Bipolar IC

Type	Ordering Code	Package
S 89	Q67000-H1694	P-DIP-14

Frequency divider with the preselectable divider ratios 50/51, 100/101, 100/102, 200/202.

Maximum input frequency is 500 MHz for divider ratios 100/102 and 200/202, or 250 MHz for divider ratios 50/51 and 100/101.

The S 89 is particularly intended as prescaler for the S 187 B.

Main application: Prescaler in dual-modulus frequency dividers.

Maximum Ratings

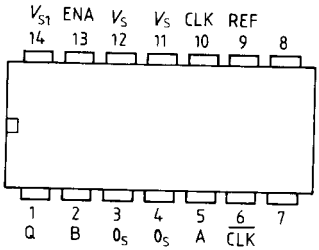
Description	Symbol	min	max	Unit
Supply voltage	V_S	−0.3	7	V
Input voltage ENA Input voltage A, B Input voltage CLK	V_I V_I V_I	−0.3 −0.3 −0.3	15 7 V_S +0.3	V V V
Output voltage Q1, output disabled	V_{Q1}	−0.3	12	V
External voltage at REF	V_I	−0.3	V_S +0.3	V
Output current at Q1 output conducting, V_{S1} open	I_{Q1}		4	mA
Junction temperature Storage temperature range Ambient temperature range	T_j T_{stg} T_A	 −55 −30	125 125 80	°C °C °C
Thermal resistance system – air	$R_{th\ SA}$		75	K/W

Function Data

Description	Symbol	Conditions	min	max	Unit
Supply voltage	V_S		4.5	5.5	V
Input frequency	f_{CLK}	ratios 50/51, 100/101		300[1]	MHz
Input frequency	f_{CLK}	ratios 100/102, 200/202		500[1]	MHz
Input frequency, sinusoidal	f_{CLK}	ratios 50/51, 100/101	20[1]		MHz
Input frequency, sinusoidal	f_{CLK}	ratios 100/102, 200/202	20[1]		MHz

Pin Configuration

(top view)



[1]) Amplitude (peak-to-peak) at CLK: 250 mV ≤ V_{CLKpp} ≤ 400 mV; V_S: 4.75 ≤ V_S ≤ 5.5 V.

Characteristics

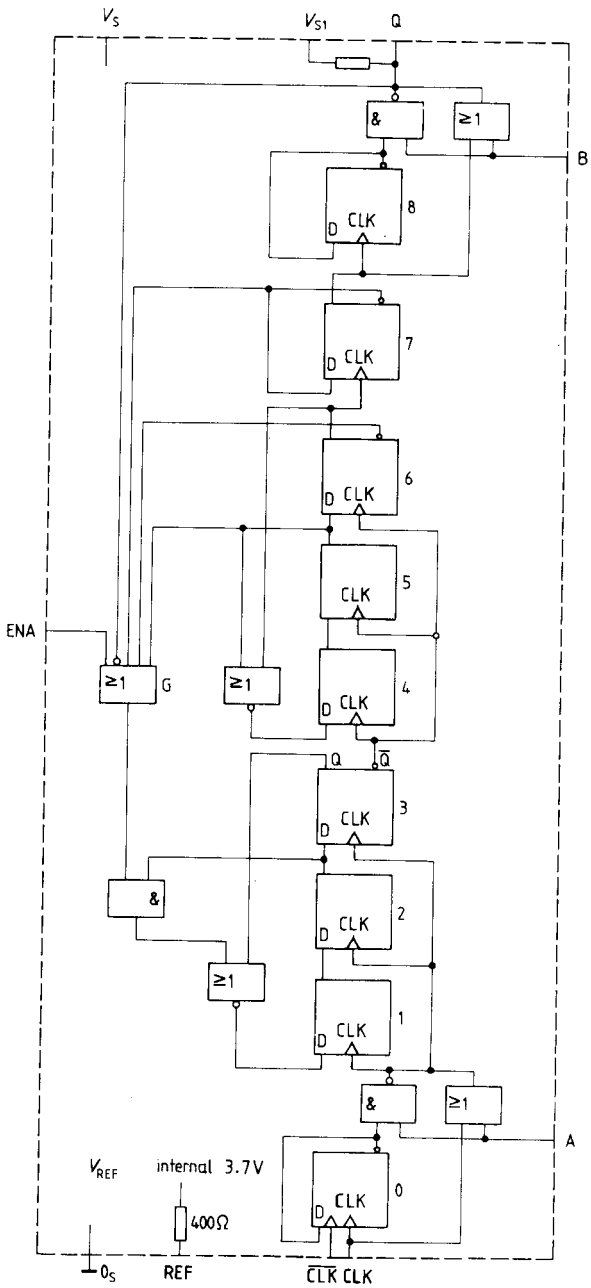
throughout the operating range
$V_S = 5$ V, $T_A = -30$ °C to +80 °C

Description	Symbol	Test conditions	min	typ	max	Unit
Supply voltage	V_S		4.75	5	5.25	V
Supply current	I_S	inputs and outputs open		55	85	mA
L input voltage at ENA	V_{IL}				1	V
H input voltage at ENA	V_{IH}	$T_A = -30$ °C	3.2			V
H input voltage at ENA	V_{IH}	$T_A = 25$ °C	3.0			V
H input voltage at ENA	V_{IH}	$T_A = 80$ °C	2.8			V
H input current at ENA	I_{IH}	$V_{ENA} = V_{ENA\,H} = f(T_A)$		0.17	0.3	mA
H input current at ENA	I_{IH}	$V_{ENA} = 9$ V		1.7	3	mA
L input voltage at A or B	V_{IL}				1.5	V
H input voltage at A or B	V_{IH}		$V_S - 0.1$		$V_S + 0.1$	V
H input current at A or B	I_{IH}	$V_{AB} = V_S$		0.5	1	mA
Threshold voltage at CLK	V_{CLK}	$V_S = 5$ V		3.7		V
Switching voltage deviation at CLK, static (CLK and REF connected)	$V_{CLK\,pp}$	$V_S = 5$ V	250		1600	mV
Switching voltage deviation at CLK at 500 MHz (CLK and REF connected)	$V_{CLK\,pp}$	$V_S = 5$ V	250		400	mV
Output voltage at Q	V_Q	$I_{Q1} = 3.2$ mA			0.5	V
	V_Q	$V_{S1} = 11.5$ V			2	V
		$I_{S1} < 100$ µA				
R between Q and V_{S1}	R_Q	$T_A = 25$ °C	2.0	2.5	3.2	kΩ

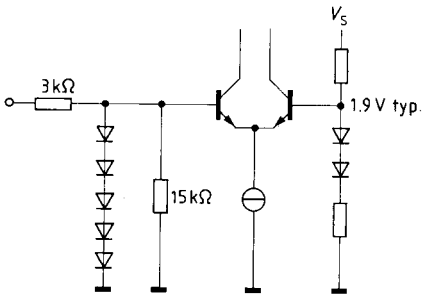
Truth Table

A	B	ENA	f_{CLK}/f_Q	Input frequency MHz min	Input frequency MHz max
H	H	H	200	40	500
H	H	L	202		
H	L	H	100		
H	L	L	102		
L	H	H	100	20	250
L	H	L	101		
L	L	H	50		
L	L	L	51		

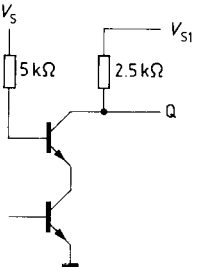
Block Diagram



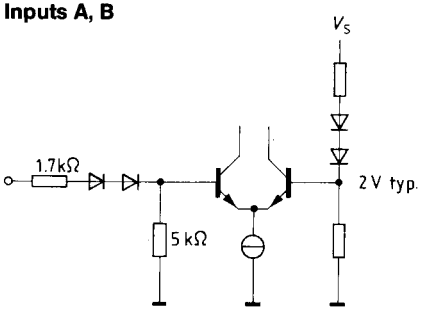
Input ENA



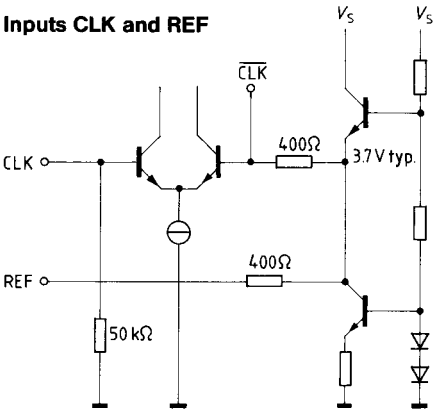
Outputs Q and V_{S1}



Inputs A, B

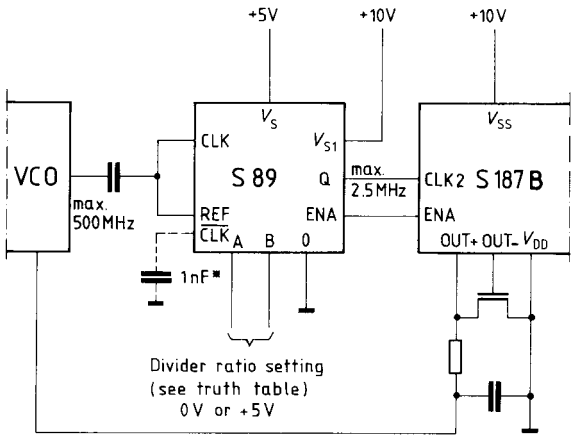


Inputs CLK and REF



Typical Application

Prescaler for PLL circuits S 187 B/C



*) Capacitor is only necessary for operation close to the maximum frequency and maximum input sensitivity