4 Megabit x 4 Dynamic RAM 5V, Fast Page

Features

4 Meg x 4 bit CMOS Dynamic
Random Access Memory

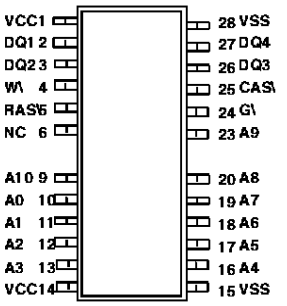
- Access Times: 60 and 70ns
- 32ms Refresh Rate
- Low Operating Power Dissipation
- Low Standby Power
- Common I/O
- All Inputs/Outputs TTL Compatible

Package Style

- 24/28 Thinpack™ Flatpack
- 24/28 Pin Flatpack

Single +5V (±10%) Supply Operation

Pin Configurations



The EDI444096C is a high performance, low power CMOS Dynamic RAM organized as 4 Megabit x 4.

During READ and WRITE cycles each bit is addressed through 22 address bits which are entered 11 at a time (AØ-A10). RAS\ is used to latch the first 11 bits and CAS\, the second 11 bits. A READ or WRITE cycle is selected with the W\ input. A logic HIGH on W\ dictates READ mode, while a logic LOW on W\ dictates WRITE mode.

During a WRITE cycle Data-in is latched by the falling edge of W\ or CAS\, whichever occurs last. If W\ goes low prior to CAS\ going LOW, the output pins remain open (HIGH-Z) until the next CAS\ cycle, regardless of the status of G\. If W\ goes LOW after data reaches the output pins, Data-out pins are activated and retain the selected cell data as long as CAS\ and G\ remain LOW, regardless of W\ or RAS\. This late W\ pulse results in a DELAYED WRITE or READ-WRITE cycle.

The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by W\ and G\. FAST PAGE MODE operations allow faster data operations, READ, WRITE or READ-MODIFY-WRITE, within a row address.

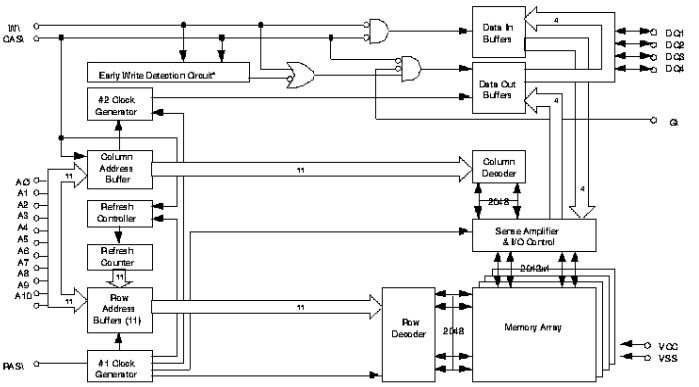
All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

Note: W\ LOW prior to CAS\ LOW, EW detection circuit output is a HIGH (EARLY WRITE). CAS\ LOW prior to W\ LOW, EW detection circuit output is a LOW (LATE WRITE).

Pin Names

AØ-A10	Address Inputs
CAS\	Column Address Strobe
RAS\	Row Address Strobe
W\	Write Control Input
G\	Output Enable
DQ1-DQ4	Data Inputs/Outputs
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Block Diagram



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-1.0V to 7.0V
Operating Temperature TA (Ambient)	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature (Ceramic)	-65°C to +150°C
Power Dissipation	1 Watt
Output Current	50 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Note 1

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.4	--	Vcc+1	V
Input Low Voltage	VIL	-1.0	–	0.8	V

Notes: 1. All voltage values are with respect to VSS.

Electrical Characteristics

(VCC = 5.0V ±10%) Note 2.

Parameter	Sym	Conditions	Min	Typ	Max	Units
Average Supply Current from VCC	ICC1	RAS\, CAS\ Cycling			110	mA
Operating (Notes 3, 4)		TRC = TWC = Min, Output Open				
Supply Current from VCC	ICC2	RAS\ = CAS\ = VIH, Outputs Open			2	mA
Standby		RAS\ = CAS\ ≥ VCC-0.2, Outputs Open			2	mA
Average Supply Current from VCC	ICC3	RAS\ Cycling, CAS\ = VIH			110	mA
Refreshing (Note 3)		TRC = Min, Outputs Open				
Average Supply Current from VCC	ICC4	RAS\ = VIL, CAS\ = Cycling			80	mA
Fast Page Mode (Notes 3, 4)		TPC = Min, Outputs Open				
Average Supply Current from VCC	ICC6	CAS\ before RAS\ Refresh Cycling			110	mA
CAS\ before RAS\ Refresh Mode (Note 3)		TRC = Min Outputs Open				
Input Current	II	0V ≤ VIN ≤ 5.5V	-2		2	µA
		All Other Input Pins = 0V				
Off-State Output Current	IOZ	Q Floating 0V ≤ V OUT ≤ 5.5V	-10		10	µA
Output High Voltage	VOH	IOH = -5mA	2.4	—	VCC	V
Output Low Voltage	VOL	IOL = 4.2mA	0	—	0.4	V

Notes: 2. Current flowing into an IC is positive, out is negative.
3. ICC1(av), ICC3(av), ICC4(av), and ICC6 are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. ICC1(av), and ICC4(av) are dependent on output loading. Specified values are obtained with the output open.

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Test Conditions	Min	Typ	Max	Unit
Address Input Capacitance	CA	VI = VSS			6	pF
Input Capacitance (D)	CD	f = 1MHz			6	pF
Input Capacitance (CAS\,W\, RAS\)	CC, CW, CR	VI = 25mVrms			7	pF
Output Capacitance (Q)	CQ	VO = VSS, f = 1MHz, VI = 25mVrms			8	pF

Input Conditions for Each Mode

The EDI444096C provides, in addition to normal Read, Write, and Read-modify-Write operations, a number of other functions, e.g. Fast Page Mode, RAS\-only Refresh, and Delayed Write. The input conditions for each are shown below.

ACT = Active
NAC= Non-active
DNC= Don't care
VLD = Valid
APD = Applied
OPN = Open

Operation	Inputs RAS\	CAS\	W\	G\	Row Address	Column Address	Input/Output D	Q
Read*	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD
Early Write*	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN
Read-Modify-Write*	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD
RAS\-only Refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN
Hidden Refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD
CAS\ before RAS\ Refresh	ACT	ACT	ACT	DNC	DNC	DNC	DNC	OPN
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN

*Fast Page Mode Identical

Switching Characteristics

(VCC=5.0V±10%) Note 5,11,12

		60ns		70ns			
Parameter	Sym	Min	Max	Min	Max	Units	Notes
Access Time from CAS\	TCAC		20		20	ns	6,7
Access Time from RAS\	TRAC		60		70	ns	6,8
Column Address Access Time	TCAA		35		35	ns	6
Access Time from CAS\ Precharge	TCPA		40		40	ns	
Access Time from G\	TOEA		20		20	ns	6
Output Low Impedance Time from CAS\ low	TCLZ	3		3		ns	9
Output Disable Time after CAS\ High	TOFF	3	20	3	20	ns	10
Output Disable Time after G\ High	TDISOE	3	20	3	20	ns	10

Notes: 5. An initial pause of 100µs is required after power-up, followed by any RAS\ only refresh or CAS\ before RAS\ refresh cycles with W\ HIGH before proper device operation is achieved. Note that RAS\ may be cycled during the initial pause. Any RAS\ only refresh or CAS\ before RAS\ refresh cycles with W\ HIGH are required after prolonged periods of RAS\ inactivity before proper device operation.

6. Measured with a load circuit equivalent to 2TTL loads and 100pF.
7. Assumes that TRCD ≥ TRCD (max).
8. Assumes that TRCD ≤TRCD(max).
9. Guaranteed, but not tested.
10. TOFF(max) defines the time at which the output achieves the high impedance state (IOUT = |±10µA|) and is not reference to VOH(min) or VOL(max).

Timing Requirements
Read, Write, Read-Modify-Write, Refresh, and Fast Page Mode Cycles

(VCC=5.0V±10%) Note 5,11,12

		60ns		70ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Refresh Cycle	TREF		32		32	ms	
RAS\ Precharge Time	TRP	50		50		ns	
RAS\ to CAS\ Delay Time	TRCD	20	50	20	50	ns	13
Delay CAS\ High to RAS\ Low	TCRP	5		5		ns	
CAS\ Precharge Time (Non Page Mode)	TCPN	10		10		ns	
Column Address Delay from RAS\ Low	TRAD	15	35	15	35	ns	14
Row Address Set Up Time	TASR	0		0		ns	
Column Address Set Up Time	TASC	0		0		ns	15
Row Address Hold Time	TRAH	10		10		ns	
Column Address Hold Time	TCAH	15		15		ns	
Transition Time	TT	3	50	3	50	ns	16

Notes: 11. The timing requirements are assumed TT = 5ns.
12. VIH(min) and VIL (max) are reference levels for measuring timing of input signals.
13. TRCD(max) is specified as a reference point only. If TRCD is less than TRCD(max), access time is TRAC. If TRCD is greater than TRCD(max), access time is defined as TCAC and TCAA as shown in note 7.
14. TRAD(max) is specified as a reference point only. If TRAD = TRAD(max), access time is assumed byTCAA for read cycle.
15. TASC(max) is specified as a reference point only of address acess time.
16. TT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

(VCC=5.0V±10%) Note 5,11,12

		60ns		70ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read Cycle Time	TRC	130		130		ns	
RAS\ Low Pulse Width	TRAS	60	100,000	70	100,000	ns	
CAS\ Low Pulse Width	TCAS	20	100,000	20	100,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	60		70		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		ns	
Read Set Up Time before CAS\ Low	TRCS	0		0		ns	
Read Hold Time after CAS\ High	TRCH	0		0		ns	17
Read Hold Time after RAS\ High	TRRH	0		0		ns	17
Column Address to RAS\ Setup	TRAL	35		35		ns	
Precharge to CAS\ Active	TRPC	0		0		ns	
Delay Time, Data to G\ Low	TDOEL	0		0		ns	
Delay Time, G\ High to Data	TOEHD	20		20		ns	

Note: 17. Either TRCH or TRRH must be satisfied for a Read Cycle

Write Cycle, Early and Delayed Write

(VCC = 5.0V±10%) Notes5,11,12

		60ns		70ns			
Parameter	Sym	Min	Max	Min	Max	Unit	Notes
Write Cycle Time	TWC	130		130		ns	
RAS\ Low Pulse Width	TRAS	60	100,000	70	100,000	ns	
CAS\ Low Pulse Width	TCAS	20	100,000	20	100,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	60		70		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		ns	
Write Setup Time before CAS\ Low	TWCS	0		0		ns	18
Write Hold Time after CAS\ Low	TWCH	15		15		ns	
CAS\ Hold Time after Write Low	TCWL	20		20		ns	
RAS\ Hold Time after Write Low	TRWL	20		20		ns	
Write Pulse Width	TWP	15		15		ns	
Data Set up Time	TDS	0		0		ns	18
Data Hold Time after CAS\ Low	TDH	15		15		ns	18
Delay Time, G\ High to Data	TOEHD	20		20		ns	
G\ Hold Time after Write Low	THWOE	20		20		ns	

Read-Write and Read-Modify - Write Cycles

(VCC = 5.0V±10%)

		60ns		70ns			
Parameter	Sym	Min	Max	Min	Max	Unit	Notes
Read-Modify-Write Cycle Time	TRWC	180		205		ns	
RAS\ Low Pulse Width	TRASRW	60	100,000	80	100,000	ns	
CAS\ Low Pulse Width	TCASRW	20	100,000	20	100,000	ns	
CAS\ Hold Time after RAS\ Low	TCSHRW	60		80		ns	
RAS\ Hold Time after CAS\ Low	TRSHRW	20		20		ns	
Read Setup time before CAS\ Low	TRCS	0		0		ns	
CAS\ Low to W\ Low Delay	TCWD	50		50		ns	18
RAS\ Low to W\ Low Delay	TRWD	95		110		ns	18
CAS\ Hold after W\ Low	TCWL	20		20		ns	
RAS\ Hold after W\ Low	TRWL	20		20		ns	
Write Pulse Width	TWP	15		15		ns	
Data Set up Time	TDS	0		0		ns	
Data Hold Time after W\ Low	TDH	15		15		ns	
Address to W\ Low Delay	TAWD	65		70		ns	18
Delay Time, G\ High to Data	TOEHD	20		20		ns	
G\ Hold Time after Write Low	THWOE	20		20		ns	

Notes 18. TWCS, TRWD, TCWD, and TAWD do not define the limits of operation, but are included as electrical characteristics only.
When TWCS ≥ TWCS(min), an early write cycle is performed, and the data output keeps the high-impedance state. When TRWD≥ TRWD(min), TCWD ≥ TCWD(min) and TAWD ≥ TAWD(min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of Q (at the access time and until CAS\ goes back to VIH) is indeterminate.

Fast Page Mode Cycle
Read, Early Write, Read-Write, Read-Modify-Write Cycle

(VCC = 5.0V±10%) Notes 5,11,12

		60ns		70ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast Page Mode Cycle Time	TPC	40		40		ns	
Fast Page Mode for R/W, R/M/W Cycle Time	TPRWC	95		95		ns	
RAS\ Low Pulse Width for Read, Write Cycle	TRASP	60	100,000	70	100,000	ns	
CAS\ Low Pulse Width for Read Cycle	TCAS	20	100,000	20	100,000	ns	
CAS\ Pulse Width (Page Mode)	TCP	10		10		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		ns	

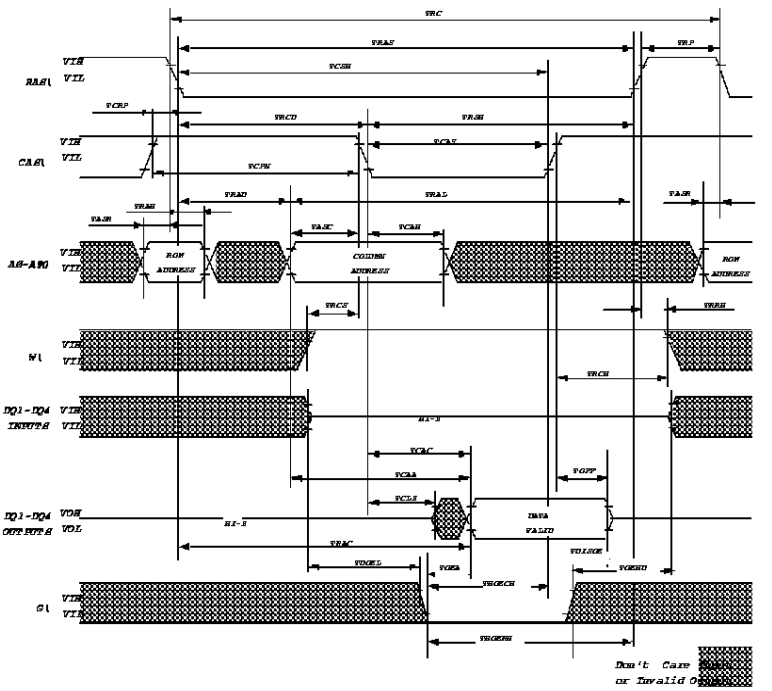
CAS\ before RAS\ Refresh Cycle

(VCC = 5.0V±10%) Notes 5,11,12

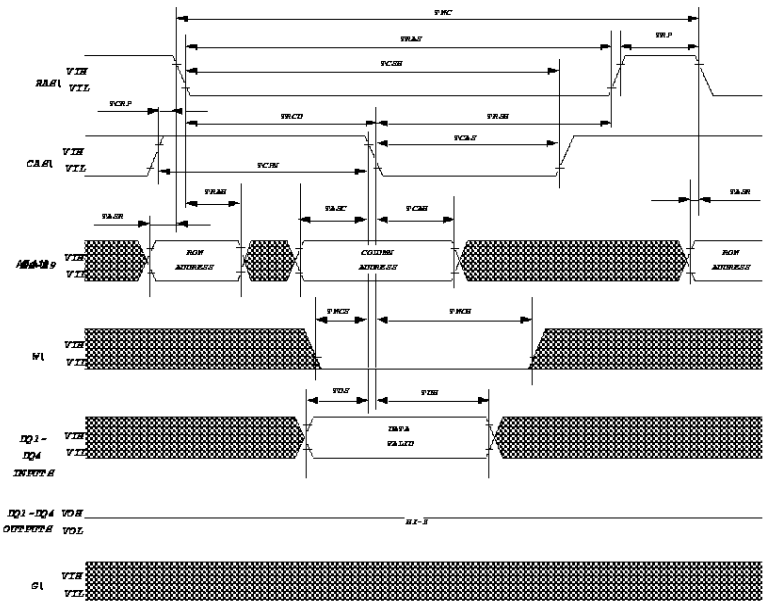
		60ns		70ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
CAS\ Setup for CAS\ before RAS\ Refresh	TCSR	5		5		ns	19
CAS\ Hold for CAS\ before RAS\ Refresh	TCHR	15		15		ns	19
Precharge to CAS\ Active	TRPC	0		0		ns	19
Write Set Up	TWRP	10		10		ns	19
Write Hold	TWRH	10		10		ns	19

Note: 19. Eight or more CAS\ before RAS\ cycles are necessary for proper operation of CAS\ before RAS\ refresh mode.

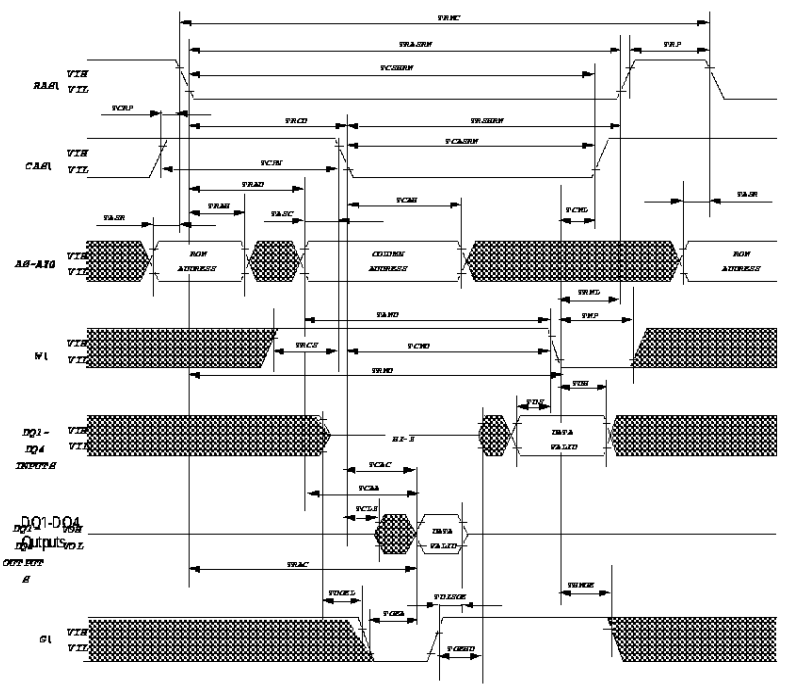
Read Cycle



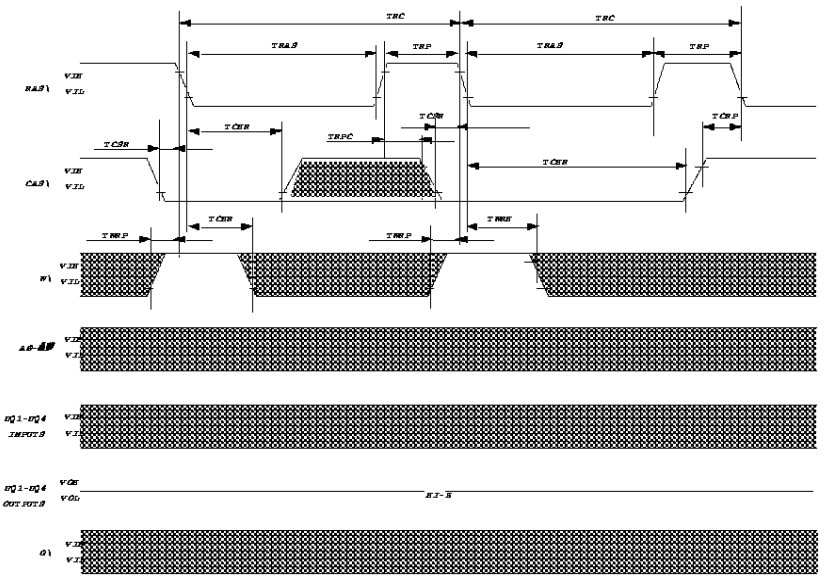
Write Cycle, Early Write



Read-Write, Read-Modify-Write and Delayed Write Cycle

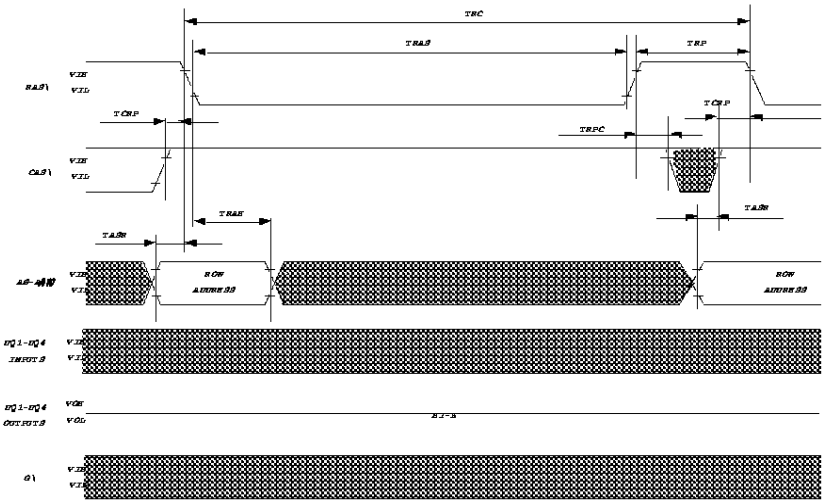


CAS\ before RAS\ Refresh Cycle



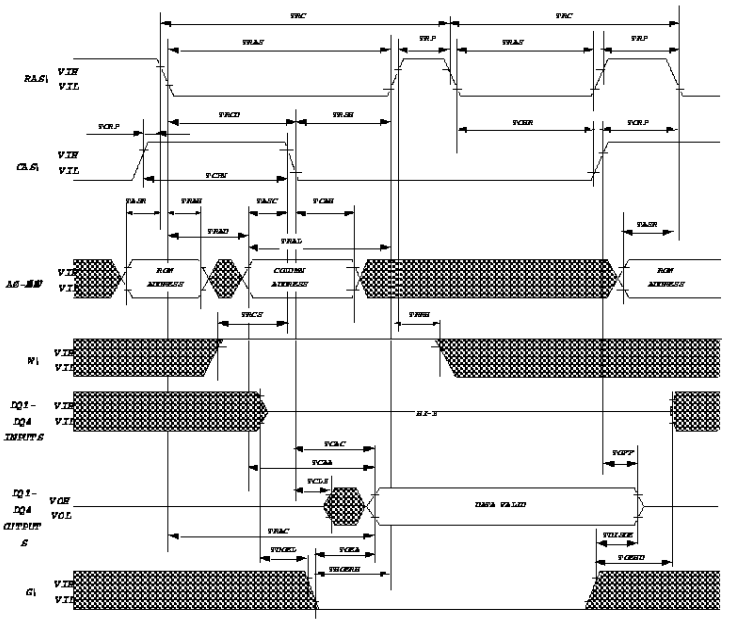
RAS\-only Refresh Cycle

Note 20

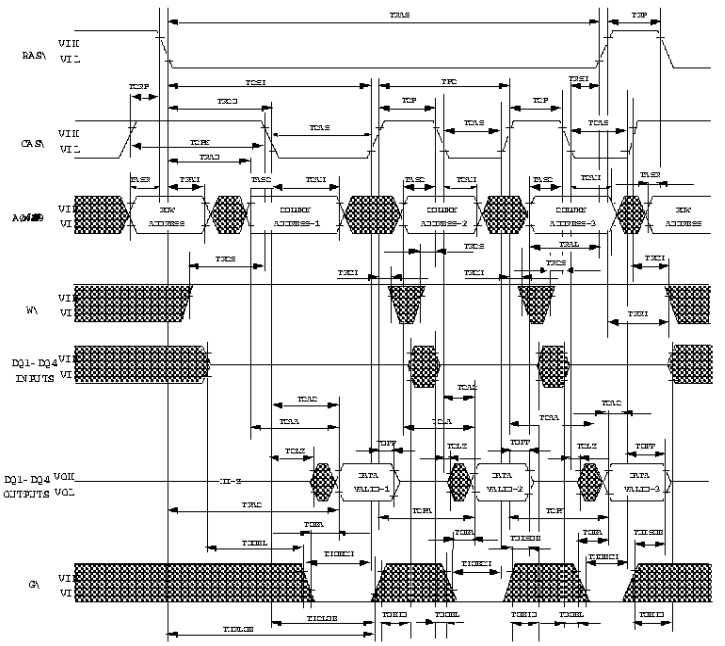


Note 20. W\ Don't Care

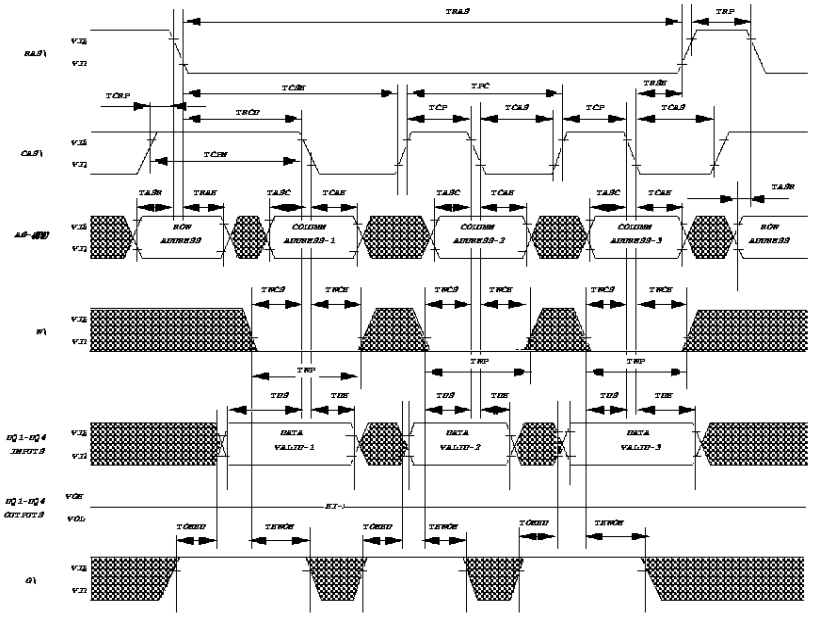
Hidden Refresh Cycle



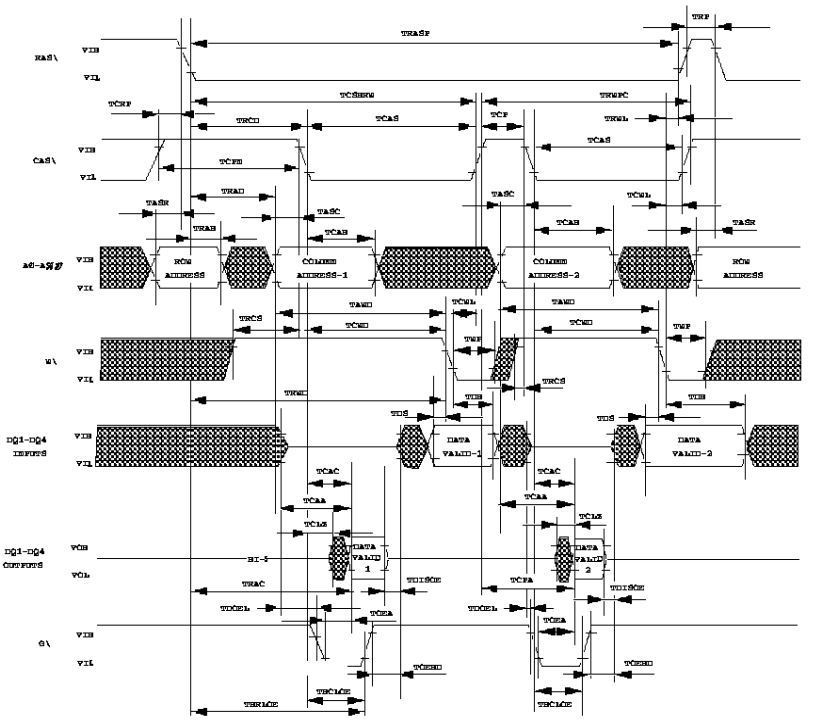
Fast-Page-Mode, Read Cycle



Fast-Page-Mode, Early Write Cycle



Fast-Page-Mode, Read-Write, Read-Modify-Write Cycle



Ordering Information

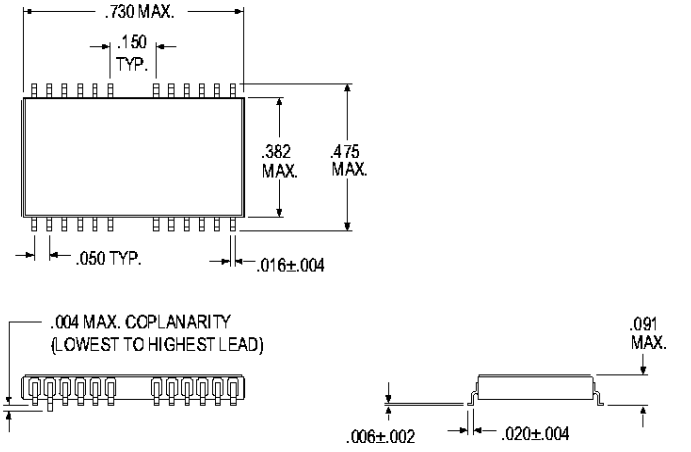
Part No.	Speed(ns)	Package No.
EDI444096C60BB	60	317
EDI444096C70BB	70	317

Part No.	Speed(ns)	Package No.
EDI444096C60FB	60	347
EDI444096C70FB	70	347

Note: For commercial, Industrial or Mil-Temp-Only grade products use C, I or M respectively to replace B or Q in the suffix of the part number, eg. EDI444096C70BB (Compliant) becomes EDI444096C70BI (Industrial).

Package Description

Package No. 317
24/28 Pin Ceramic Thinpack ™ Flatpack
Weight = 1.2 gm
Theta JC = 15°C/W
Theta JA = 38°C/W



Package No. 347
24/28 Pin Ceramic Flatpack
Weight = 1.2 gm
Theta JC = 15°C/W
Theta JA = 38°C/W