

# DATA SHEET

## **HSTL16919**

9-bit to 18-bit HSTL to LVTTL  
memory address latch with  
12 kohm pull-up resistor

Product data  
Supersedes data of 2001 Jul 19

2004 Apr 15

# 9-bit to 18-bit HSTL to LVTTTL memory address latch with 12 kohm pull-up resistor

## HSTL16919

### FEATURES

- Inputs meet JEDEC HSTL Std. JESD 8–6, and outputs meet Level III specifications
- 12 k $\Omega$  pull-up on D and  $\overline{LE}$  inputs
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.
- Latch-up testing is done to JEDEC Standard JESD78, which exceeds 100 mA.
- Packaged in 48-pin plastic thin shrink small outline package (TSSOP48)

### DESCRIPTION

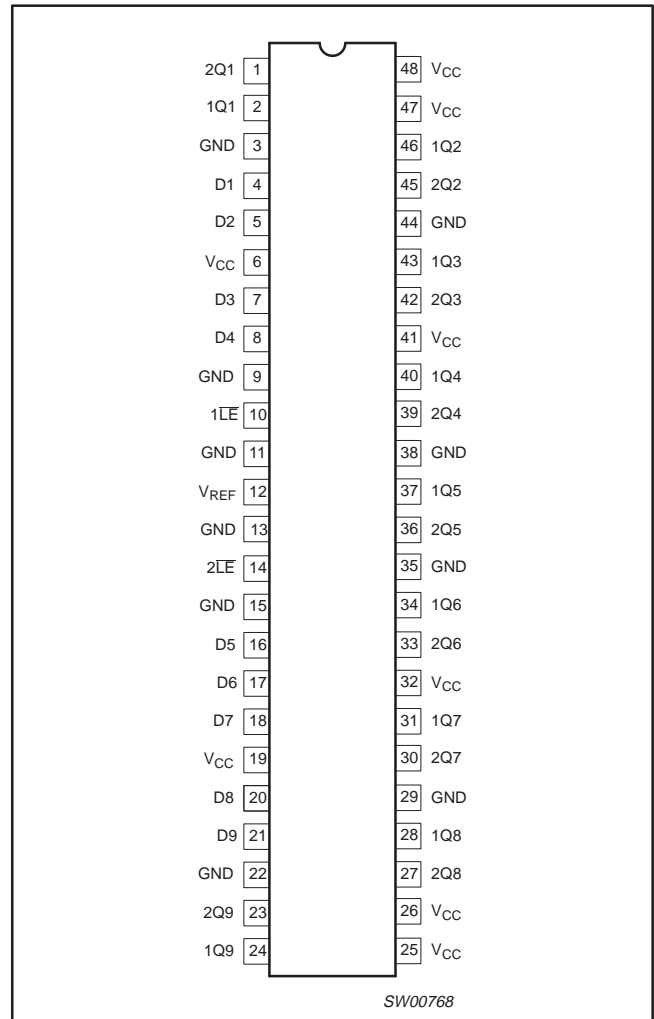
The HSTL16919 is a 9-bit to 18-bit D-type latch designed for 3.15 V to 3.45 V  $V_{CC}$  operation. The D inputs accept HSTL levels and the Q outputs provide LVTTTL levels.

The HSTL16919 is particularly suitable for driving an address bus to two banks of memory. Each bank of nine outputs is controlled with its own latch-enable ( $\overline{LE}$ ) input.

Each of the nine D inputs is tied to the inputs of two D-type latches that provide true data (Q) at the outputs. While  $\overline{LE}$  is LOW the Q outputs of the corresponding nine latches follow the D inputs. When  $\overline{LE}$  is taken HIGH, the Q outputs are latched at the levels set up at the D inputs.

The HSTL16919 is characterized for operation from 0 °C to +70 °C.

### PIN CONFIGURATION



### ORDERING INFORMATION

$T_{amb} = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$

Type number	Package		Version
	Name	Description	
HSTL16919DGG	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

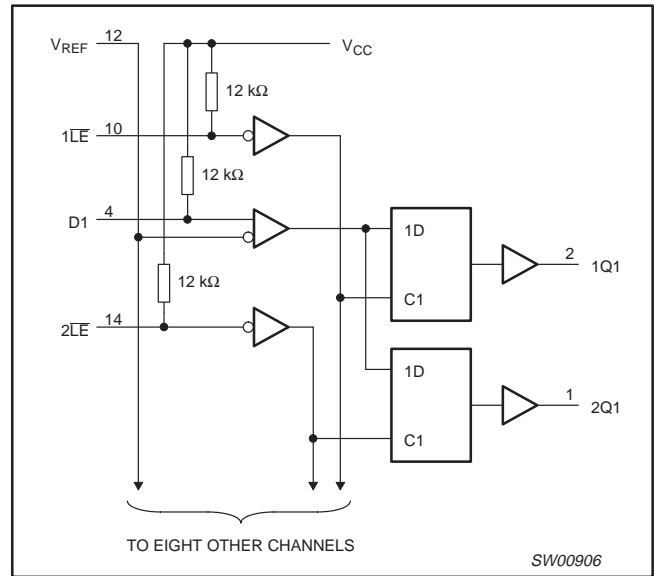
# 9-bit to 18-bit HSTL to LVTTTL memory address latch with 12 kohm pull-up resistor

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## PIN DESCRIPTION

PIN	SYMBOL	FUNCTION
4, 5, 7, 8, 16, 17, 18, 20, 21	D[1:9]	Inputs
2, 46, 43, 40, 37, 34, 31, 28, 24	1Q[1:9]	Outputs
1, 45, 42, 39, 36, 33, 30, 27, 23	2Q[1:9]	
10	1LE	Latch enable
14	2LE	
12	VREF	Reference voltage
6, 19, 25, 26, 32, 41, 47, 48	VCC	Supply voltage
3, 9, 11, 13, 15, 22, 29, 35, 38, 44	GND	Ground

## LOGIC DIAGRAM (positive logic)



## FUNCTION TABLE

INPUTS		OUTPUT Q
LE	D	
L	H	H
L	L	L
H	X	$Q_0^1$

### NOTE:

1. Output level before the indicated steady-state input conditions were established.

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## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Over operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	Supply voltage range		-0.5 to +4.6	V
$V_I$	Input voltage range <sup>2</sup>		-0.5 to $V_{CC} + 0.5$	V
$V_O$	Output voltage range <sup>2</sup>		-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0\text{ V}$	-50	mA
$I_{OK}$	Output clamp current <sup>3</sup>	$V_O < 0\text{ V}$ or $V_O > V_{CC}$	±50	mA
$I_O$	Continuous output current	$V_O = 0\text{ V}$ to $V_{CC}$	±50	mA
	Continuous current through each $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>4</sup>		89	°C/W
$T_{stg}$	Storage temperature range		-65 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- This current flows only when the output is in the HIGH state and  $V_O > V_{CC}$ .
- The package thermal impedance is calculated in accordance with JESD 51.

## RECOMMENDED OPERATING CONDITIONS<sup>1</sup>

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
$V_{CC}$	Supply voltage		3.15	—	3.45	V
$V_{REF}$	Reference voltage		0.68	0.75	0.9	V
$V_I$	Input voltage		0	—	1.5	V
$V_{IH}$	AC HIGH-level input voltage	All inputs	$V_{REF} + 200\text{ mV}$	—	—	V
$V_{IL}$	AC LOW-level input voltage	All inputs	—	—	$V_{REF} - 200\text{ mV}$	V
$V_{IH}$	DC HIGH-level input voltage	All inputs	$V_{REF} + 100\text{ mV}$	—	—	V
$V_{IL}$	DC LOW-level input voltage	All inputs	—	—	$V_{REF} - 100\text{ mV}$	V
$I_{OH}$	HIGH-level output current		—	—	-24	mA
$I_{OL}$	LOW-level output current		—	—	24	mA
$T_{amb}$	Operating free-air temperature range		0	—	+70	°C

### NOTE:

- All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

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## ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ <sup>1</sup>	Max	
$V_{IK}$		$V_{CC} = 3.15\text{ V}; I_I = -18\text{ mA}$	—	—	-1.2	V
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 3.15\text{ V}; I_{OH} = -24\text{ mA}$	2.4	—	—	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 3.15\text{ V}; I_{OL} = 24\text{ mA}$	—	—	0.5	V
$I_I$	Control inputs	$V_{CC} = 3.45\text{ V}; V_I = 0\text{ V or } 1.5\text{ V}$	—	—	-500	$\mu\text{A}$
	Data inputs	$V_{CC} = 3.45\text{ V}; V_I = 0\text{ V or } 1.5\text{ V}$	—	—	-500	$\mu\text{A}$
	$V_{REF}$	$V_{CC} = 3.45\text{ V}; V_{REF} = 0.68\text{ V or } 0.9\text{ V}$	—	—	90	$\mu\text{A}$
$I_{CC}$	Supply current	$V_{CC} = 3.45\text{ V}; V_I = 0\text{ V or } 1.5\text{ V}$	—	50	100	mA
$C_I$	Control inputs	$V_{CC} = 0\text{ V or } 3.3\text{ V}; V_I = 0\text{ V or } 3.3\text{ V}$	—	2	—	pF
	Data inputs	$V_{CC} = 0\text{ V or } 3.3\text{ V}; V_I = 0\text{ V or } 3.3\text{ V}$	—	2.5	—	pF
$C_O$	Outputs	$V_{CC} = 0\text{ V}; V_O = 0\text{ V}$	—	4	—	pF

### NOTE:

1. All typical values are at  $V_{CC} = 3.3\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$ .

## TIMING REQUIREMENTS

Over recommended operating free-air temperature range (unless otherwise noted).

SYMBOL	PARAMETER	TEST CONDITIONS	$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
			Min	Max	
$t_w$	Pulse duration	LE LOW (Figure 1)	3	—	ns
$t_{su}$	Setup time	D before $\overline{LE} \uparrow$ (Figure 2)	2	—	ns
$t_h$	Hold time	D after $\overline{LE} \uparrow$ (Figure 2)	1	—	ns
$t_{ldr}$	Data race condition time <sup>1</sup>	D after $\overline{LE} \downarrow$	—	0	ns

### NOTE:

1. This is the maximum time after  $\overline{LE}$  switches LOW that the data input can return to the latched state from the opposite state without producing a glitch on the output.

## SWITCHING CHARACTERISTICS

Over recommended operating free-air temperature range;  $V_{REF} = 0.75\text{ V}$ .

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
				Min	Max	
$t_{pd}$	Propagation delay (Figure 3)	D	Q	1.9	3.4	ns
		$\overline{LE}$	Q	1.9	4.2	ns

## SIMULTANEOUS SWITCHING CHARACTERISTICS

Over recommended operating free-air temperature range;  $V_{REF} = 0.75\text{ V}$ 

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$		UNIT
				Min	Max	
$t_{pd}$	Propagation delay; all outputs switching (Figure 3)	D	Q	1.9	4.4	ns
		$\overline{LE}$	Q	1.9	5.2	ns

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## VOLTAGE WAVEFORMS

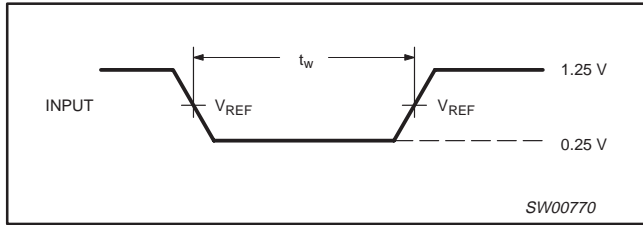
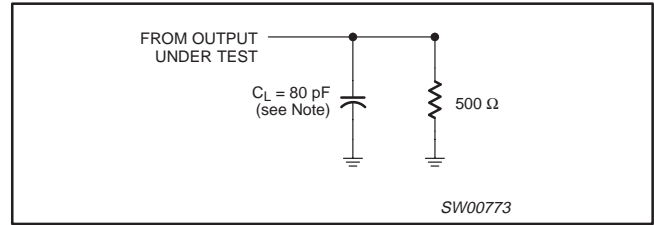


Figure 1. Pulse duration

## LOAD CIRCUIT



NOTE: C<sub>L</sub> includes probe and jig capacitance.

Figure 4. Load circuit

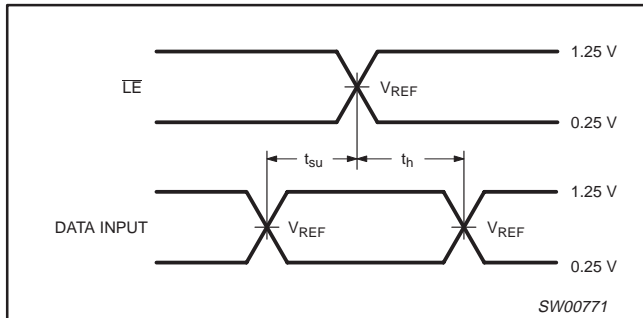


Figure 2. Setup and Hold times

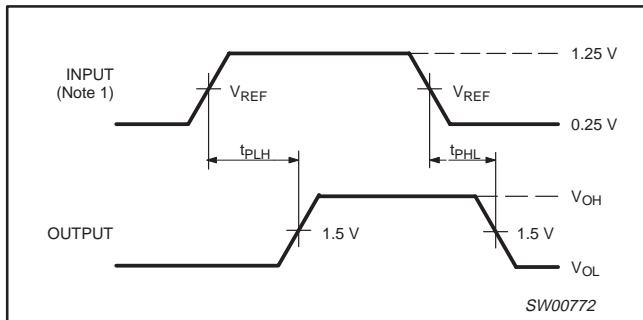


Figure 3. Propagation delay times

**NOTES:**

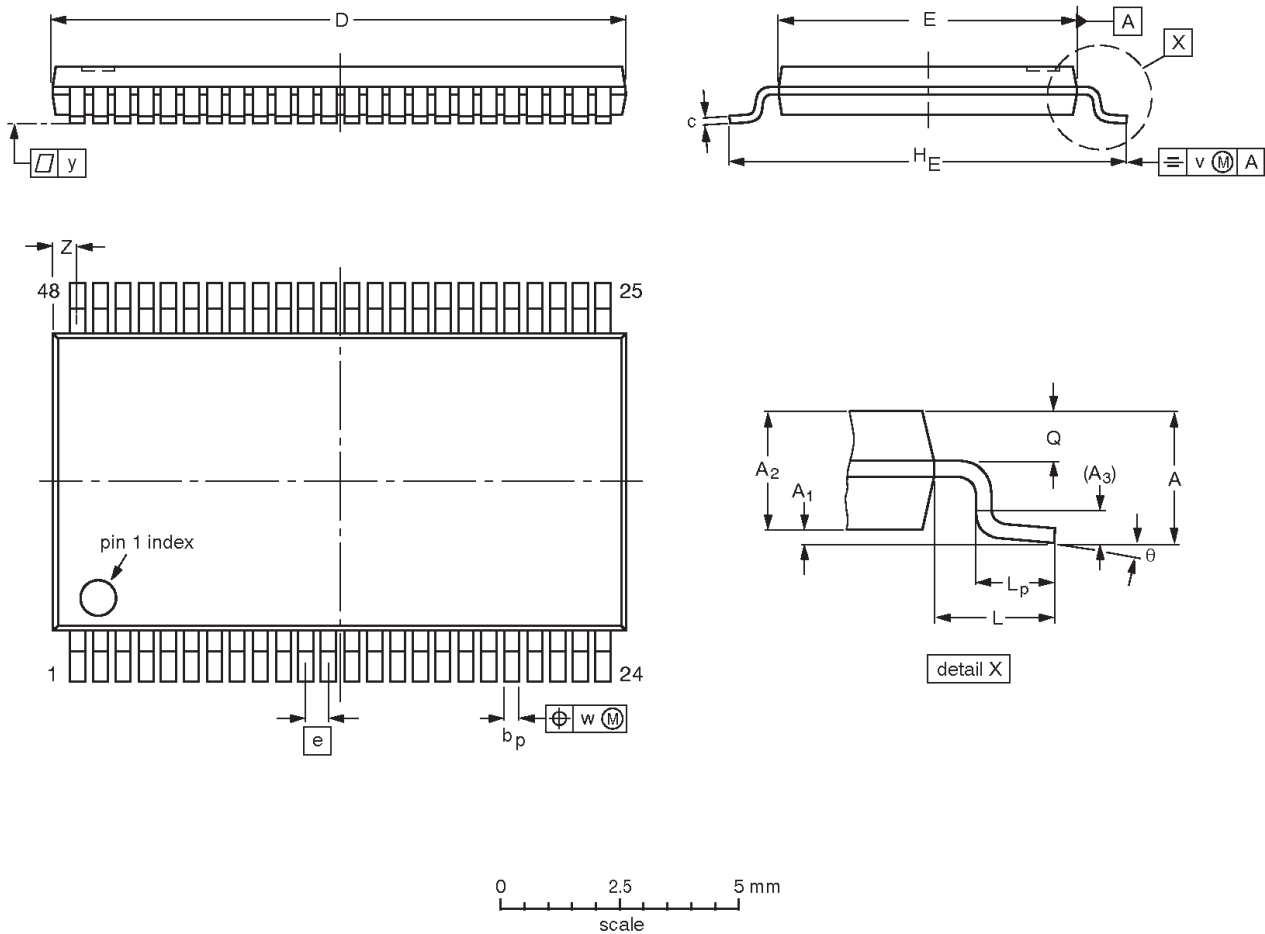
1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 1 ns, t<sub>f</sub> ≤ 1 ns.
2. The outputs are measured one at a time with one transition per measurement.
3. t<sub>PHL</sub> and t<sub>PLH</sub> are the same as t<sub>pd</sub>.

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**TSSOP48:** plastic thin shrink small outline package; 48 leads; body width 6.1 mm

**SOT362-1**



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153				-95-02-10 99-12-27

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## REVISION HISTORY

Rev	Date	Description
_2	20040415	<b>Product data (9397 750 13143). Supersedes data of 2001 Jul 19 (9397 750 08587).</b> Modifications: <ul style="list-style-type: none"> <li>Page 3: Logic diagram (positive logic) modified.</li> </ul>
_1	20010719	<b>Product data (9397 750 08587). ECN 853-2269 26745 of 19 July 2001.</b>

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Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
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For additional information please visit  
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