TFRA28J13 Superframer DS3/DS2/DS1/E1/DS0

1 Introduction

The documentation package for the TFRA28J13 Superframer DS3/DS2/DS1/E1/DS0 system chip consists of the following documents:

- The *Supermapper Family Register Description* and the *Supermapper Family System Design Guide*. These two documents are available on a password-protected website.
- The *Superframer Product Description*, and the *Superframer Hardware Design Guide* (this document). These two documents are available on the public website shown below.

If the reader displays this document using *Acrobat Reader* ®, clicking on any blue text will bring the reader to that reference point. Clicking on the back arrow (Go to previous View) in the toolbar of the *Acrobat Reader* will bring the reader back to the starting point.

To access related documents, including the documents mentioned above, please go to the following public website, or contact your Agere representative (see the last page of this document).

http://www.agere.com/enterprise_metro_access/mappers_muxes.html

This document describes the hardware interfaces to the Agere Systems Inc. TFRA28J13 Superframer device. Information relevant to the use of the device in a board design is covered. Pin descriptions, dc electrical characteristics, timing diagrams, ac timing parameters, packaging, and operating conditions are included.

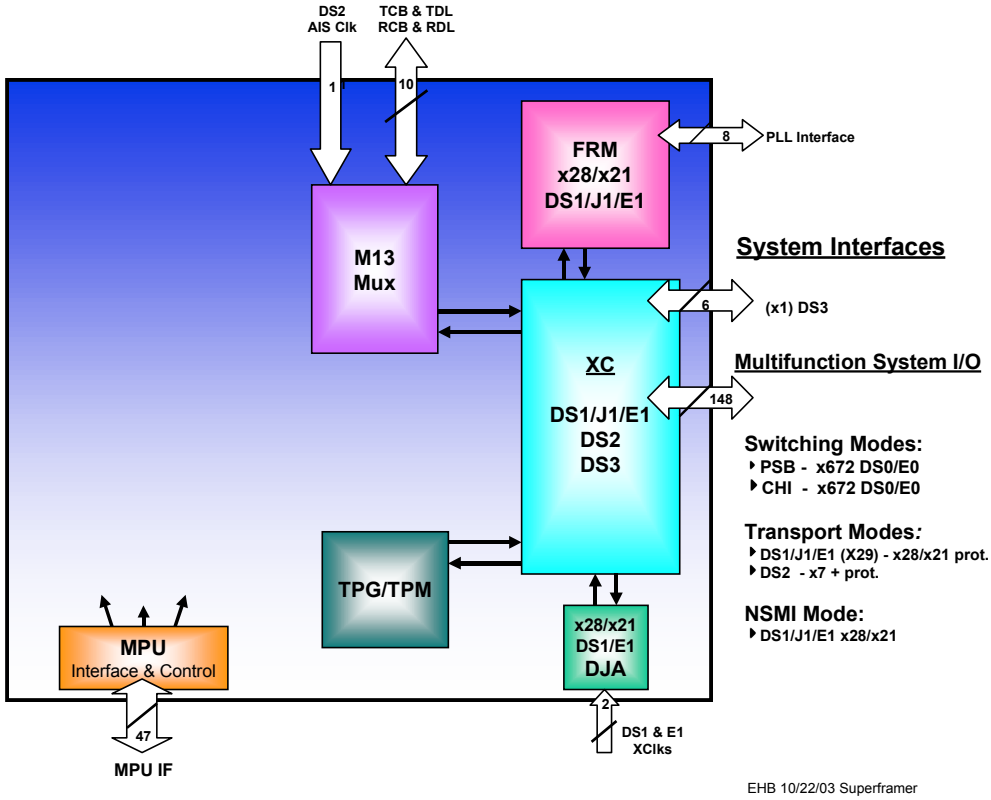

Figure 1-1. Superframer Block Diagram and High-Level Interface Definition

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2 Pin Information

2.1 456-Pin PBGA Pin Diagram

The TFRA28J13 Superframer is housed in a 456-pin plastic ball grid array. Figure 2-1 shows the ball assignment viewed from the top of the package. The pins are spaced on a 1.0 mm pitch.

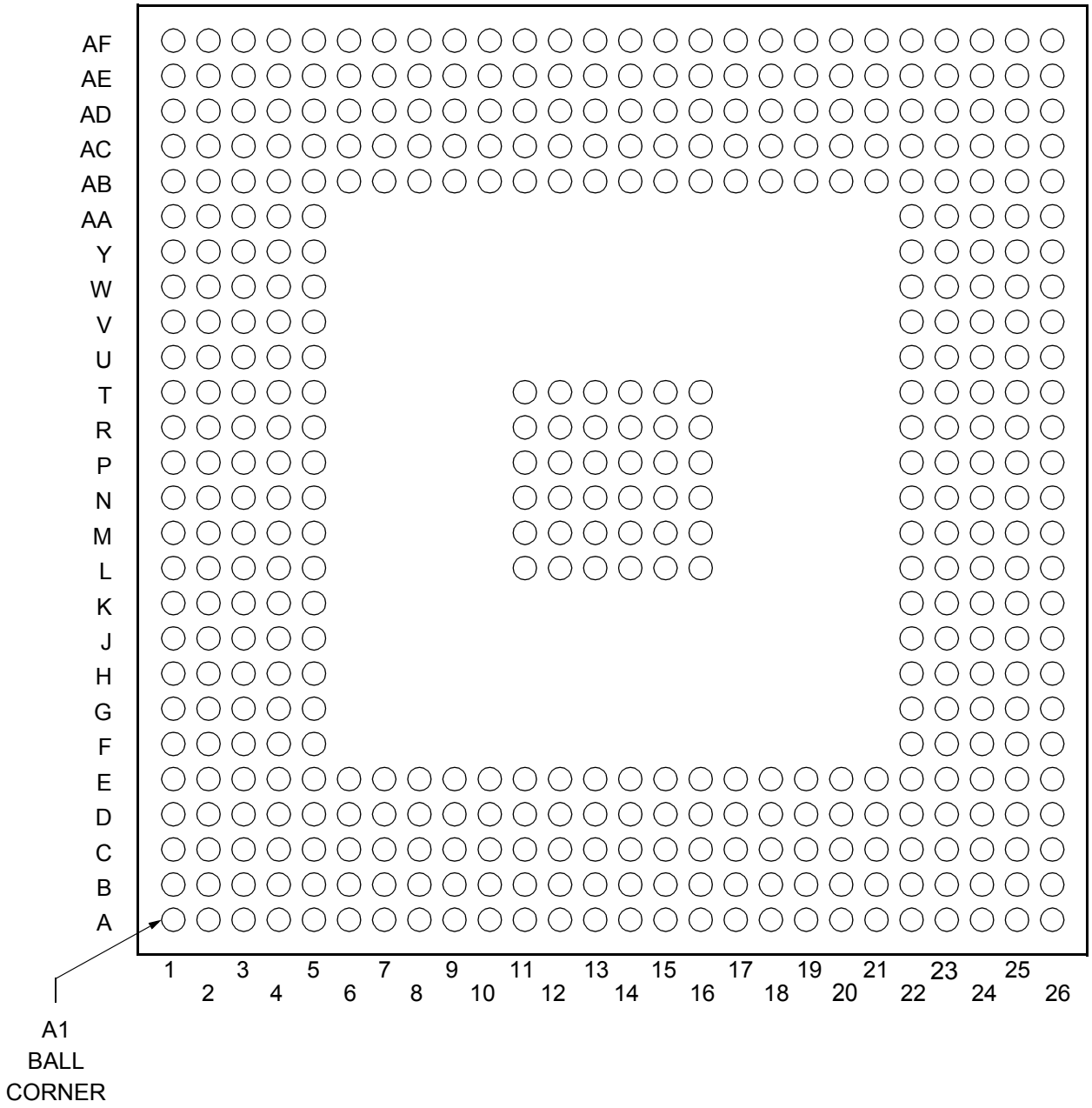

Figure 2-1. Pin Diagram of 456-Pin PBGA (Bottom View)

2.2 Pin Assignments for 456-Pin PBGA by Pin Number Order

Table 2-1. Pin/Name (cont)

Pin	Signal Name
A1	VDD
A2	VSS
A3	LINERXDATA17
A4	LINERXDATA18
A5	VDD
A6	VSS
A7	LINERXDATA21
A8	LINERXSYNC23
A9	LINERXCLK24
A10	VDD
A11	VSS
A12	LINERXDATA27
A13	LINERXSYNC29
A14	LINETXDATA1
A15	LINETXSYNC3
A16	VSS
A17	VDD
A18	LINETXCLK6
A19	LINETXDATA7
A20	LINETXSYNC9
A21	VSS
A22	VDD
A23	LINETXSYNC12
A24	LINETXSYNC13
A25	VSS
A26	VDD
B1	VSS
B2	LINERXCLK15
B3	LINERXSYNC18
B4	LINERXSYNC19
B5	LINERXSYNC20
B6	LINERXDATA20
B7	LINERXSYNC22
B8	LINERXCLK23
B9	LINERXDATA24
B10	LINERXDATA25
B11	LINERXDATA26
B12	LINERXSYNC28
B13	LINERXCLK29
B14	LINETXCLK1
B15	LINETXDATA2
B16	LINETXSYNC4
B17	LINETXSYNC5
B18	LINETXSYNC6
B19	LINETXCLK7
B20	LINETXDATA8
B21	LINETXSYNC10
B22	LINETXDATA10
B23	LINETXDATA11
B24	LINETXDATA12
B25	LINETXCLK13
B26	VSS
C1	LINERXSYNC15
C2	LINERXDATA14
C3	LINERXCLK17
C4	LINERXCLK18
C5	LINERXCLK19
C6	LINERXCLK20
C7	LINERXCLK21
C8	LINERXDATA22
C9	LINERXSYNC24
C10	LINERXCLK25
C11	LINERXCLK26
C12	LINERXCLK27
C13	LINERXDATA28
C14	LINETXSYNC2
C15	LINETXCLK3
C16	LINETXCLK4
C17	LINETXCLK5
C18	LINETXDATA6
C19	LINETXSYNC8
C20	LINETXCLK9
C21	LINETXCLK10
C22	LINETXCLK11
C23	LINETXCLK12
C24	LINETXCLK14
C25	LINETXSYNC15
C26	LINETXDATA14
D1	LINERXSYNC14
D2	LINERXDATA13
D3	LINERXCLK14
D4	VSS
D5	LINERXDATA19
D6	LINERXSYNC21
D7	LINERXCLK22
D8	LINERXDATA23
D9	LINERXSYNC25
D10	LINERXSYNC26
D11	LINERXSYNC27
D12	LINERXCLK28
D13	LINERXDATA29
D14	LINETXSYNC1
D15	LINETXCLK2
D16	LINETXDATA3
D17	LINETXDATA4
D18	LINETXDATA5
D19	LINETXSYNC7
D20	LINETXCLK8
D21	LINETXDATA9
D22	LINETXSYNC11
D23	VSS
D24	LINETXCLK15
D25	LINETXSYNC16
D26	LINETXDATA15
E1	VDD
E2	LINERXDATA12
E3	LINERXCLK13
E4	LINERXSYNC13
E5	VDD
E6	LINERXSYNC17
E7	VSS
E8	TDLDATA
E9	TDLCLK
E10	DS2AISCLK
E11	VDD
E12	TCBDATA
E13	TCBCLK
E14	TCBSYNC
E15	RCBDATA
E16	VDD
E17	RCBCLK
E18	RCBSYNC
E19	RDLCLK
E20	VSS
E21	LINETXDATA13
E22	VDD
E23	LINETXDATA16
E24	LINETXCLK16
E25	LINETXSYNC17
E26	VDD
F1	VSS
F2	LINERXSYNC12
F3	LINERXCLK12
F4	LINERXDATA11
F5	LINERXDATA15
F22	LINETXSYNC14
F23	LINETXSYNC18
F24	LINETXCLK17
F25	LINETXDATA17
F26	VSS
G1	LINERXSYNC11
G2	LINERXDATA10
G3	LINERXCLK11
G4	LINERXCLK10
G5	VSS
G22	VSS
G23	LINETXCLK19
G24	LINETXCLK18
G25	LINETXSYNC19
G26	LINETXDATA18
H1	LINERXDATA9
H2	LINERXCLK9
H3	LINERXSYNC10
H4	LINERXSYNC9
H5	LINERXDATA16
H22	RDLDATA
H23	LINETXDATA20
H24	LINETXDATA19
H25	LINETXCLK20
H26	LINETXSYNC20
J1	LINERXCLK8
J2	LINERXSYNC8
J3	LINERXDATA8
J4	LINERXDATA7
J5	LINERXCLK16
J22	DS3DATAINCLK
J23	LINETXSYNC22
J24	LINETXSYNC21
J25	LINETXDATA21
J26	LINETXCLK21
K1	VDD
K2	LINERXSYNC7
K3	LINERXCLK7
K4	LINERXDATA6
K5	LINERXSYNC16
K22	DS3NEGDATAIN
K23	LINETXSYNC23
K24	LINETXCLK22
K25	LINETXDATA22
K26	VDD
L1	VSS
L2	LINERXSYNC6
L3	LINERXCLK6
L4	LINERXDATA5
L5	VDD
L11	VSS
L12	VSS
L13	VSS

Table 2-1. Pin/Name (cont)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
L14	VSS	P15	VSS	V1	NC	AB10	NC
L15	VSS	P16	VSS	V2	NC	AB11	VDD
L16	VSS	P22	DS3NEGDATAOUT	V3	NC	AB12	VSSA_CDR
L22	VDD	P23	LINETXSYNC27	V4	NC	AB13	NC
L23	LINETXSYNC24	P24	LINETXSYNC28	V5	TDO	AB14	NC
L24	LINETXCLK23	P25	LINETXCLK27	V22	PHASEDETUP	AB15	NC
L25	LINETXDATA23	P26	LINETXDATA27	V23	DATA0	AB16	VDD
L26	VSS	R1	NC	V24	DATA3	AB17	NC
M1	LINERXSYNC5	R2	LINERXSYNC1	V25	DATA1	AB18	NC
M2	LINERXDATA4	R3	NC	V26	DATA2	AB19	RXDATAEN
M3	LINERXCLK5	R4	LINERXCLK1	W1	NC	AB20	VSS
M4	LINERXCLK4	R5	TCK	W2	NC	AB21	MODE2_PLL
M5	SCAN_MODE	R11	VSS	W3	NC	AB22	VDD
M11	VSS	R12	VSS	W4	NC	AB23	ADDR19
M12	VSS	R13	VSS	W5	TMSN	AB24	INTN
M13	VSS	R14	VSS	W22	TXDATAEN	AB25	DATA15
M14	VSS	R15	VSS	W23	DATA4	AB26	VDD
M15	VSS	R16	VSS	W24	DATA7	AC1	NC
M16	VSS	R22	DS3POSDATAOUT	W25	DATA5	AC2	NC
M22	DS3POSDATAIN	R23	LINETXCLK28	W26	DATA6	AC3	NC
M23	LINETXCLK25	R24	LINETXCLK29	Y1	NC	AC4	VSS
M24	LINETXCLK24	R25	LINETXDATA28	Y2	NC	AC5	NC
M25	LINETXSYNC25	R26	LINETXSYNC29	Y3	NC	AC6	NC
M26	LINETXDATA24	T1	VSS	Y4	NC	AC7	NC
N1	LINERXDATA3	T2	NC	Y5	VSS	AC8	NC
N2	LINERXCLK3	T3	NC	Y22	VSS	AC9	VDDA_CDR
N3	LINERXSYNC4	T4	NC	Y23	DATA8	AC10	NC
N4	LINERXSYNC3	T5	VDD	Y24	DATA11	AC11	NC
N5	SCAN_EN	T11	VSS	Y25	DATA9	AC12	NC
N11	VSS	T12	VSS	Y26	DATA10	AC13	NC
N12	VSS	T13	VSS	AA1	VSS	AC14	NC
N13	VSS	T14	VSS	AA2	NC	AC15	ETOGGLE
N14	VSS	T15	VSS	AA3	NC	AC16	TSTMUX0
N15	VSS	T16	VSS	AA4	NC	AC17	E1XCLK
N16	VSS	T22	VDD	AA5	NC	AC18	CSN
N22	DS3DATAOUTCLK	T23	LINETXDATA29	AA22	ADDR13	AC19	ADDR0
N23	LINETXDATA26	T24	RSTN	AA23	DATA12	AC20	ADDR4
N24	LINETXDATA25	T25	PMRST	AA24	DATA14	AC21	ADDR8
N25	LINETXCLK26	T26	VSS	AA25	DATA13	AC22	ADDR12
N26	LINETXSYNC26	U1	VDD	AA26	VSS	AC23	VSS
P1	LINERXSYNC2	U2	NC	AB1	VDD	AC24	ADDR17
P2	LINERXCLK2	U3	NC	AB2	NC	AC25	APS_INTN
P3	LINERXDATA1	U4	NC	AB3	NC	AC26	ADDR18
P4	LINERXDATA2	U5	TDI	AB4	NC	AD1	NC
P5	IDDQ	U22	PHASEDETDOWN	AB5	VDD	AD2	NC
P11	VSS	U23	DTN	AB6	NC	AD3	NC
P12	VSS	U24	PAR1	AB7	VSS	AD4	NC
P13	VSS	U25	PAR0	AB8	TRSTN	AD5	NC
P14	VSS	U26	VDD	AB9	IC3STATEN	AD6	NC

Table 2-1. Pin/Name (cont)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
AD7	NC	AD25	ADDR16	AE17	MPCLK	AF9	NC
AD8	NC	AD26	ADDR15	AE18	ADSN	AF10	VDD
AD9	NC	AE1	VSS	AE19	ADDR1	AF11	VSS
AD10	NC	AE2	NC	AE20	ADDR5	AF12	NC
AD11	NC	AE3	NC	AE21	ADDR9	AF13	NC
AD12	NC	AE4	NC	AE22	ADDR11	AF14	TSTPHASE
AD13	NC	AE5	NC	AE23	VDDS_PLL	AF15	TSTMODE
AD14	ECSEL	AE6	NC	AE24	MODE1_PLL	AF16	VSS
AD15	TSTSFTLD	AE7	NC	AE25	ADDR14	AF17	VDD
AD16	DS1XCLK	AE8	NC	AE26	VSS	AF18	RWN
AD17	MPMODE	AE9	NC	AF1	VDD	AF19	ADDR2
AD18	DSN	AE10	NC	AF2	VSS	AF20	ADDR6
AD19	ADDR3	AE11	NC	AF3	NC	AF21	VSS
AD20	ADDR7	AE12	NC	AF4	NC	AF22	VDD
AD21	ADDR10	AE13	NC	AF5	VDD	AF23	VSSA_PLL
AD22	VDDD_PLL	AE14	BYPASS	AF6	VSS	AF24	MODE0_PLL
AD23	VSSS_PLL	AE15	EXDNUP	AF7	NC	AF25	VSS
AD24	CLKIN_PLL	AE16	TSTMUX1	AF8	NC	AF26	VDD

2.3 Pin Assignments for 456-Pin PBGA by Signal Name

Table 2-2. Pin Assignments for 456-Pin PBGA by Signal Name

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
ADDR0	AC19	NC	AB13	ECSEL	AD14	LINERXCLK24	A9
ADDR1	AE19	NC	AE11	ETOGGLE	AC15	LINERXCLK25	C10
ADDR2	AF19	DATA0	V23	EXDNUP	AE15	LINERXCLK26	C11
ADDR3	AD19	DATA1	V25	IC3STATEN	AB9	LINERXCLK27	C12
ADDR4	AC20	DATA2	V26	IDDQ	P5	LINERXCLK28	D12
ADDR5	AE20	DATA3	V24	INTN	AB24	LINERXCLK29	B13
ADDR6	AF20	DATA4	W23	LINERXCLK1	R4	LINERXDATA1	P3
ADDR7	AD20	DATA5	W25	LINERXCLK2	P2	LINERXDATA2	P4
ADDR8	AC21	DATA6	W26	LINERXCLK3	N2	LINERXDATA3	N1
ADDR9	AE21	DATA7	W24	LINERXCLK4	M4	LINERXDATA4	M2
ADDR10	AD21	DATA8	Y23	LINERXCLK5	M3	LINERXDATA5	L4
ADDR11	AE22	DATA9	Y25	LINERXCLK6	L3	LINERXDATA6	K4
ADDR12	AC22	DATA10	Y26	LINERXCLK7	K3	LINERXDATA7	J4
ADDR13	AA22	DATA11	Y24	LINERXCLK8	J1	LINERXDATA8	J3
ADDR14	AE25	DATA12	AA23	LINERXCLK9	H2	LINERXDATA9	H1
ADDR15	AD26	DATA13	AA25	LINERXCLK10	G4	LINERXDATA10	G2
ADDR16	AD25	DATA14	AA24	LINERXCLK11	G3	LINERXDATA11	F4
ADDR17	AC24	DATA15	AB25	LINERXCLK12	F3	LINERXDATA12	E2
ADDR18	AC26	DS1XCLK	AD16	LINERXCLK13	E3	LINERXDATA13	D2
ADDR19	AB23	DS2AISCLK	E10	LINERXCLK14	D3	LINERXDATA14	C2
ADSN	AE18	DS3DATAINCLK	J22	LINERXCLK15	B2	LINERXDATA15	F5
APS_INTN	AC25	DS3DATAOUTCLK	N22	LINERXCLK16	J5	LINERXDATA16	H5
NC	AC6	DS3NEGDATAIN	K22	LINERXCLK17	C3	LINERXDATA17	A3
NC	AE6	DS3NEGDATAOUT	P22	LINERXCLK18	C4	LINERXDATA18	A4
NC	AD6	DS3POSDATAIN	M22	LINERXCLK19	C5	LINERXDATA19	D5
BYPASS	AE14	DS3POSDATAOUT	R22	LINERXCLK20	C6	LINERXDATA20	B6
CLKIN_PLL	AD24	DSN	AD18	LINERXCLK21	C7	LINERXDATA21	A7
CSN	AC18	DTN	U23	LINERXCLK22	D7	LINERXDATA22	C8
NC	AB10	E1XCLK	AC17	LINERXCLK23	B8	LINERXDATA23	D8

Table 2-2. Pin Assignments for 456-Pin PBGA by Signal Name (cont)

Signal Name	Pin
LINERXDATA24	B9
LINERXDATA25	B10
LINERXDATA26	B11
LINERXDATA27	A12
LINERXDATA28	C13
LINERXDATA29	D13
LINERXSYNC1	R2
LINERXSYNC2	P1
LINERXSYNC3	N4
LINERXSYNC4	N3
LINERXSYNC5	M1
LINERXSYNC6	L2
LINERXSYNC7	K2
LINERXSYNC8	J2
LINERXSYNC9	H4
LINERXSYNC10	H3
LINERXSYNC11	G1
LINERXSYNC12	F2
LINERXSYNC13	E4
LINERXSYNC14	D1
LINERXSYNC15	C1
LINERXSYNC16	K5
LINERXSYNC17	E6
LINERXSYNC18	B3
LINERXSYNC19	B4
LINERXSYNC20	B5
LINERXSYNC21	D6
LINERXSYNC22	B7
LINERXSYNC23	A8
LINERXSYNC24	C9
LINERXSYNC25	D9
LINERXSYNC26	D10
LINERXSYNC27	D11
LINERXSYNC28	B12
LINERXSYNC29	A13
LINETXCLK1	B14
LINETXCLK2	D15
LINETXCLK3	C15
LINETXCLK4	C16
LINETXCLK5	C17
LINETXCLK6	A18

Signal Name	Pin
LINETXCLK7	B19
LINETXCLK8	D20
LINETXCLK9	C20
LINETXCLK10	C21
LINETXCLK11	C22
LINETXCLK12	C23
LINETXCLK13	B25
LINETXCLK14	C24
LINETXCLK15	D24
LINETXCLK16	E24
LINETXCLK17	F24
LINETXCLK18	G24
LINETXCLK19	G23
LINETXCLK20	H25
LINETXCLK21	J26
LINETXCLK22	K24
LINETXCLK23	L24
LINETXCLK24	M24
LINETXCLK25	M23
LINETXCLK26	N25
LINETXCLK27	P25
LINETXCLK28	R23
LINETXCLK29	R24
LINETXDATA1	A14
LINETXDATA2	B15
LINETXDATA3	D16
LINETXDATA4	D17
LINETXDATA5	D18
LINETXDATA6	C18
LINETXDATA7	A19
LINETXDATA8	B20
LINETXDATA9	D21
LINETXDATA10	B22
LINETXDATA11	B23
LINETXDATA12	B24
LINETXDATA13	E21
LINETXDATA14	C26
LINETXDATA15	D26
LINETXDATA16	E23
LINETXDATA17	F25
LINETXDATA18	G26

Signal Name	Pin
LINETXDATA19	H24
LINETXDATA20	H23
LINETXDATA21	J25
LINETXDATA22	K25
LINETXDATA23	L25
LINETXDATA24	M26
LINETXDATA25	N24
LINETXDATA26	N23
LINETXDATA27	P26
LINETXDATA28	R25
LINETXDATA29	T23
LINETXSYNC1	D14
LINETXSYNC2	C14
LINETXSYNC3	A15
LINETXSYNC4	B16
LINETXSYNC5	B17
LINETXSYNC6	B18
LINETXSYNC7	D19
LINETXSYNC8	C19
LINETXSYNC9	A20
LINETXSYNC10	B21
LINETXSYNC11	D22
LINETXSYNC12	A23
LINETXSYNC13	A24
LINETXSYNC14	F22
LINETXSYNC15	C25
LINETXSYNC16	D25
LINETXSYNC17	E25
LINETXSYNC18	F23
LINETXSYNC19	G25
LINETXSYNC20	H26
LINETXSYNC21	J24
LINETXSYNC22	J23
LINETXSYNC23	K23
LINETXSYNC24	L23
LINETXSYNC25	M25
LINETXSYNC26	N26
LINETXSYNC27	P23
LINETXSYNC28	P24
LINETXSYNC29	R26
NC	AC13

Signal Name	Pin
NC	AB15
NC	AC14
NC	AB17
NC	AB14
NC	AB18
NC	AE5
MODE0_PLL	AF24
MODE1_PLL	AE24
MODE2_PLL	AB21
MPCLK	AE17
MPMODE	AD17
PAR0	U25
PAR1	U24
PHASEDETDOWN	U22
PHASEDETUP	V22
PMRST	T25
RCBCLK	E17
RCBDATA	E15
RCBSYNC	E18
RDLCLK	E19
RDLDATA	H22
NC	AC11
NC	AD12
NC	AF12
NC	AE12
NC	AD8
NC	AC7
NC	AE7
NC	AF7
NC	AD7
NC	AC2
NC	V4
NC	U3
NC	U2
NC	U4
NC	T3
NC	T2
NC	T4
NC	R3
NC	R1
NC	V3

Table 2-2. Pin Assignments for 456-Pin PBGA by Signal Name (cont)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
NC	V2	NC	AA3	VDD	AB11	VSS	N12
NC	V1	NC	AB2	VDD	AB16	VSS	N13
NC	AC1	NC	AD2	VDD	AB22	VSS	N14
NC	W4	NC	AB3	VDD	AB26	VSS	N15
NC	AE3	TMSN	W5	VDD	AF1	VSS	N16
NC	AD4	NC	AE4	VDD	AF5	VSS	P11
NC	AF4	NC	AD5	VDD	AF10	VSS	P12
NC	AD11	NC	AC5	VDD	AF17	VSS	P13
NC	AC10	NC	AD13	VDD	AF22	VSS	P14
NC	AE10	NC	AC12	VDD	AF26	VSS	P15
NC	AD10	NC	AE13	VDDA_CDR	AC9	VSS	P16
RSTN	T24	NC	AF13	VDDD_PLL	AD22	VSS	R11
NC	AD1	TRSTN	AB8	VDDS_PLL	AE23	VSS	R12
NC	AD3	TSTMODE	AF15	VSS	A2	VSS	R13
NC	AA5	TSTMUX0	AC16	VSS	A6	VSS	R14
RWN	AF18	TSTMUX1	AE16	VSS	A11	VSS	R15
RXDATAEN	AB19	TSTPHASE	AF14	VSS	A16	VSS	R16
SCAN_EN	N5	TSTSFTLD	AD15	VSS	A21	VSS	T1
SCAN_MODE	M5	NC	AB6	VSS	A25	VSS	T11
TCBCLK	E13	NC	AE2	VSS	B1	VSS	T12
TCBDATA	E12	NC	AF3	VSS	B26	VSS	T13
TCBSYNC	E14	TXDATAEN	W22	VSS	D4	VSS	T14
TCK	R5	VDD	A1	VSS	D23	VSS	T15
TDI	U5	VDD	A5	VSS	E7	VSS	T16
TDLCLK	E9	VDD	A10	VSS	E20	VSS	T26
TDLDATA	E8	VDD	A17	VSS	F1	VSS	Y5
TDO	V5	VDD	A22	VSS	F26	VSS	Y22
NC	AE8	VDD	A26	VSS	G5	VSS	AA1
NC	AF8	VDD	E1	VSS	G22	VSS	AA26
NC	AE9	VDD	E5	VSS	L1	VSS	AB7
NC	AF9	VDD	E11	VSS	L11	VSS	AB20
NC	AD9	VDD	E16	VSS	L12	VSS	AC4
NC	AC8	VDD	E22	VSS	L13	VSS	AC23
NC	AC3	VDD	E26	VSS	L14	VSS	AE1
NC	AA2	VDD	K1	VSS	L15	VSS	AE26
NC	AA4	VDD	K26	VSS	L16	VSS	AF2
NC	Y3	VDD	L5	VSS	L26	VSS	AF6
NC	Y1	VDD	L22	VSS	M11	VSS	AF11
NC	Y2	VDD	T5	VSS	M12	VSS	AF16
NC	Y4	VDD	T22	VSS	M13	VSS	AF21
NC	W3	VDD	U1	VSS	M14	VSS	AF25
NC	W1	VDD	U26	VSS	M15	VSSA_CDR	AB12
NC	W2	VDD	AB1	VSS	M16	VSSA_PLL	AF23
NC	AB4	VDD	AB5	VSS	N11	VSSS_PLL	AD23

2.3.1 DS3 Port

If a DS3 output is required in a Superframer application and the DS3 signal has been recovered (demapped) from an STS-1, then it is necessary to smooth the DS3 recovered clock. The DS3 clock extracted from the STS-1 clock will have considerable jitter introduced when the SONET overhead is removed and pointer adjustments are made. A phase-locked loop is recommended for this purpose. The Superframer contains a phase comparator that can be used in conjunction with an external low-pass filter and voltage-controlled crystal oscillator to implement the PLL.

Table 2-3. DS3 Port

Pin	Symbol	Type	I/O	Description
V22	PHASEDETUP	LVCMOS	O	**Phase Detector Up.** Phase error signal out to external filter and VCXO. This output will generate an error signal when the VCXO output is slower than the reference signal.
U22	PHASEDETDOWN	LVCMOS	O	**Phase Detector Down.** Phase error signal out to external filter and VCXO. This output will generate an error signal when the VCXO output is faster that the reference signal.
R22	DS3POSDATAOUT	LVCMOS	O	**Positive Data Output.** Serial DS3 positive data out to LIU when the DS3 output port is operating in dual-rail mode. Nonreturn-to-zero DS3 data output when the DS3 output is operating in single-ended mode.
P22	DS3NEGDATAOUT	LVCMOS	O	**Negative Data Output.** Serial DS3 negative data output to LIU when the DS3 port is operating in dual-rail mode. In single-rail mode, this output is not used and may be left unconnected.
N22	DS3DATAOUTCLK	LVCMOS	I Pull-down	**DS3 Data Out Clock.** 44.736 MHz DS3 clock input. If the Superframer is being used to map DS3 data to and from STS-1, then this clock should be supplied by the external VCXO that is associated with the DS3 clock recovery PLL. In other DS3 modes (e.g., M13), this input will be supplied by an external crystal oscillator.
M22	DS3POSDATAIN	LVCMOS	I Pull-down	**Positive Data Input.** If the DS3 port is configured in dual-rail mode, then this input is serial positive data from an external DS3 LIU. If the DS3 port is configured in single-rail mode, then this input is serial nonreturn-to-zero data from the external LIU.
K22	DS3NEGDATAIN	LVCMOS	I Pull-down	**Negative Data In.** In dual-rail mode, this is negative data from an external DS3 LIU. In single-rail mode, it may be connected to the bipolar violation output of the external DS3 LIU, left unconnected, or tied to ground.
J22	DS3DATAINCLK	LVCMOS	I Pull-down	**DS3 Data In Clock.** This is a 44.736 MHz clock input from the clock recovery in the external DS3 LIU.

Table 2-4. DS3 Port C-Bit and Datalink Access

Pin	Symbol	Type	I/O	Description
E14	TCBSYNC	LVCMOS	O	**Transmit C-Bit Sync.** In the C-bit parity mode, 10 C-bits may optionally be input for multiplexing into the transmit DS3 frame through the TCBDATA input. The TCBSYNC output is low, except during the rising edge of TCBCLK that is used to input C2.
E13	TCBCLK	LVCMOS	O	**Transmit C-Bit Clock.** A gapped clock (nominally 93.983 kHz) for accepting selected C-bits on input M13_CBDATA.
E12	TCBDATA	LVCMOS	I Pull-down	**Transmit C-Bit Data.** In the C-bit parity mode, the network requirements bit (C2) and the unused C-bits (C4, C5, C6, C16, C17, C18, C19, C20, and C21) may optionally be input for multiplexing into the transmit DS3 frame through this input.
E9	TDLCLK	LVCMOS	O	**Transmit Data Link Clock.** A gapped clock (nominally 28.195 kHz) for accepting path maintenance data link C-bits on input TDLDATA.
E8	TDLDATA	LVCMOS	I Pull-down	**Transmit Data Link Data.** The path maintenance data link C-bits (C13, C14, and C15) may optionally be input for multiplexing into the transmit DS3 frame through this input.

Table 2-5. M13 Multiplexer/Demultiplexer Receive Section

Pin	Symbol	Type	I/O	Description
E18	RCBSYNC	LVCMOS	O	**Receive C-Bit Sync.** Ten C-bits are output on RCBDATA after they are demultiplexed from the received DS3 signal. The RCBSYNC output is low, except during the rising edge of RCBDATA that is used to output C2.
E17	RCBCLK	LVCMOS	O	**Receive C-Bit Clock.** A gapped clock (nominally 93.983 kHz) for outputting selected C-bits on RCBDATA.
E15	RCBDATA	LVCMOS	O	**Receive C-Bit Data.** The received network requirements bit (C2) and the received unused C-bits (C4, C5, C6, C16, C17, C18, C19, C20, and C21) are output after they are demultiplexed from the received DS3 signal.
E19	RDLCLK	LVCMOS	O	**Receive Data Link Clock.** A gapped clock (nominally 28.195 kHz) for outputting path maintenance data link C-bits on RDLDATA.
H22	RDLDATA	LVCMOS	O	**Receive Data Link Data.** The received path maintenance data link C-bits (C13, C14, and C15) that are demultiplexed from the received DS3 signal.

Reference clocks, used internally in the jitter attenuation and AIS generation processes, are defined. Note that these are typically supplied by free-running crystal oscillators.

Table 2-6. Reference Clocks

Pin	Symbol	Type	I/O	Description
AC17	E1XCLK	LVCMOS	I Pull-down	**E1 X Clock.** This clock signal is used by the E1 test pattern generator (i.e., to generate E1 AIS (all 1s), as a reference to the E1 DJA, and as a clock source for the E1 test pattern generator and test pattern monitor. This input may be provided by a 2.048 MHz, a 32.768 MHz, or a 65.536 MHz ± 50 ppm free-running crystal oscillator, or clocking chip. For the E1 DJA, an input of 32.768 MHz or 65.536 MHz must be used. **Note:** If this clock is used as the master clock for the framer and is provisioned in register 0x00012, bits SMPR_FRM_CLK_SEL[2:0], then this clock must be greater than the total aggregate speed of the links (plus some cushion, i.e., if all 21 links are used, then this clock must be >= 49.408 MHz).
AD16	DS1XCLK	LVCMOS	I Pull-down	**DS1 X Clock**. This clock signal is used for three purposes: to generate DS1 AIS (all 1s), as a reference to the DS1 DJA, and as a clock source for the DS1 test pattern generator and test pattern monitor. This input may be provided by a 1.544 MHz, a 24.704 MHz, or a 49.408 MHz ± 32 ppm free-running crystal oscillator, or clocking chip. For the DS1 DJA, an input of 24.704 MHz or 49.408 MHz must be used. **Note:** If this clock is used as the master clock for the framer and is provisioned in register 0x00012, bits SMPR_FRM_CLK_SEL[2:0], then this clock must be greater than the total aggregate speed of the links (plus some cushion, i.e., if all 28 links are used, then this clock must be >= 49.408 MHz).
E10	DS2AISCLK	LVCMOS	I Pull-down	**DS2 AIS Clock.** See separate DS2/E2 application note for use in DS2 mode. **VC11 AIS Clock**. A 1.664 MHz clock input. In the VT mapper mode, this clock is used to generate VC11 AIS. The clock is used when VC11 is sent from the LINETXDATA[30:1] outputs. The 1.664 MHz clock is for a VC11 payload. There are 27 bytes per VT1.5 in each STS-1 frame, excluding the VT overhead (1 byte), 26 bytes/125 µs = 1.664 Mbits/s. (VC11 rate is 1.728 Mbits/s.) If used, this input can be provided by a free-running crystal oscillator, or a clocking chip.

Table 2-7. Multifunction System Interface

Pin	Symbol	Type	I/O	Description
C13, A12, B11, B10, B9, D8, C8, A7, B6, D5, A4, A3, H5, F5, C2, D2, E2, F4, G2, H1, J3, J4, K4, L4, M2, N1, P4, P3	LINERXDATA[28:1]	LVCMOS	I Pull-down	**Line Receive Data [28:1].** Configurable inputs to the internal cross connect. The use depends on the application. Generally, these inputs are used for the received positive-rail or single-rail DS1/E1 line data input. If operating in dual-rail mode, the negative rail will be expected on LINERXSYNC[28:1]. Using dual-rail mode implies that the internal B8ZS or HDB3 decoders are enabled, and line code violations can be detected and counted inside the Superframer. These data inputs may be assigned, using the cross connect block, to the DS1 or E1 inputs on the VT mapper, M13 or DS1/E1 framers. It is also possible to use the inputs for DS2 data, in which case they may be assigned to the M23 multiplexer inputs.
D13	LINERXDATA29	LVCMOS	I Pull-down	**Receive Data 29.** Configurable input to the internal cross connect. May be used as an additional line receive data input, for a protection channel. Other possible uses are as follows: Global transmit line clock input. Externally supplied 1.544 MHz or 2.048 MHz low jitter clock phase-locked to the TDM system clock. Used for transmit line clock on the DS1/E1 framer. This is not normally used because the DS1/E1 framer has a PLL that can generate a 1.544 MHz/2.048 MHz clock from the TDM system clock (CHI clock). This applies in PSB and CHI modes. Receive data input. If NSMI mode is used, this will be a 51.84 Mbits/s serial data input.
D12, C12, C11, C10, A9, B8, D7, C7, C6, C5, C4, C3, J5, B2, D3, E3, F3, G3, G4, H2, J1, K3, L3, M3, M4, N2, P2, R4	LINERXCLK[28:1]	LVCMOS	I/O Pull-down	**Receive Clock [28:1].** Configurable inputs/outputs to the internal cross connect. Typically a line clock associated with the corresponding LINERXDATA input. It can therefore be running at DS1, E1, or DS2 rate. The cross connect is used to assign these inputs to the VT mapper, M13, or DS1/E1 framer.
B13	LINERXCLK29	LVCMOS	I/O Pull-down	**Receive Clock 29.** May be used as additional receive clock input for a DS1/E1 protection channel. Also has special use as a master clock. In CHI mode, it is the receive clock input (2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz). In PSB mode, it is the receive clock input (19.44 MHz). In NSMI mode, it is the receive clock output (51.84 MHz).

Table 2-7. Multifunction System Interface (cont)

Pin	Symbol	Type	I/O	Description
B12, D11, D10, D9, C9, A8, B7, D6, B5, B4, B3, E6, K5, C1, D1, E4, F2, G1, H3, H4, J2, K2, L2, M1, N3, N4, P1, R2	LINERXSYNC[28:1]	LVCMOS	I	**Line Receive Synchronous[28:1].** Multifunction input. Channel assignment may be configured through the internal cross connect. Can be used as the negative rail of a DS1/E1 signal in conjunction with LINERXDATA[28:1], when operating in dual-rail mode. In CHI mode, these inputs are used for receive TDM highways that may run at 2.048, 4.096, or 8.192 Mbits/s. In parallel system bus mode, the receive system data bus inputs are assigned to LINERXSYNC 16:1. The PSB is a 16-bit wide bus that operates at 19.44 MHz.
A13	LINERXSYNC29	LVCMOS	I/O	**Line Receive Synchronous 29.** Multifunction input. Channel assignment may be configured through the internal cross connect. Can be used as the negative rail of a DS1/E1 signal in conjunction with LINERXDATA 29, when operating in dual-rail mode. In CHI and PSB modes, this input is used as the receive system frame synchronization input. In NSMI mode, it is the receive frame sync output.
R25, P26, N23, N24, M26, L25, K25, J25, H23, H24, G26, F25, E23, D26, C26, E21, B24, B23, B22, D21, B20, A19, C18, D18, D17, D16, B15, A14	LINETXDATA[28:1]	LVCMOS	I/O	**Line Transmit Data [28:1]** Configurable outputs from the internal cross connect. Used for transmit positive-rail or single-rail DS1/E1 line data outputs. May be connected to the DS1/E1 outputs from the VT mapper, M13 MUX, or DS1/E1 framer line outputs. May also be used as DS2 outputs.
T23	LINETXDATA29	LVCMOS	O	**Line Transmit Data 29.** Configurable output from the internal cross connect. An extra DS1 or E1 transmit port that may be used for protection or as a timing reference output.
R23, P25, N25, M23, M24, L24, K24, J26, H25, G23, G24, F24, E24, D24, C24, B25, C23, C22, C21, C20, D20, B19, A18, C17, C16, C15, D15, B14	LINETXCLK[28:1]	LVCMOS	I/O	**Line Transmit Clock [28:1].** Configurable outputs from the internal cross connect. Can be used as the clock signals for LINETXDATA[28:1] in DS1, E1, and DS2 modes.
R24	LINETXCLK29	LVCMOS	I/O	**Line Transmit Clock 29.** Configurable output to the internal cross connect for the protection or timing reference channel. Also used as the transmit global system clock input for CHI (2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz), PSB (19.44 MHz), and NSMI (51.84 MHz) modes.

Table 2-7. Multifunction System Interface (cont)

Pin	Symbol	Type	I/O	Description
P24, P23, N26, M25, L23, K23, J23, J24, H26, G25, F23, E25, D25, C25, F22, A24, A23, D22, B21, A20, C19, D19, B18, B17, B16, A15, C14, D14	LINETXSYNC[28:1]	LVCMOS	I/O	**Line Transmit Synchronous [28:1].** Configurable inputs/outputs to the internal cross connect. An output when used as the negative rail of a DS1 or E1 output port operating in dual-rail mode. In CHI mode, these pins may be used as output TDM highways. In PSB mode, bits 16:1 are used for the transmit data bus, and bits 28:17 are not used. These pins may also be used as DS2 I/O to/from the M12 block as follows: 7:1—Tx data out. 14:8—Tx clock in. 21:16—Rx data in. 28:22—Rx clock in.
R26	LINETXSYNC29	LVCMOS	I/O	**Line Transmit Synchronous 29.** Configurable input/output to the internal cross connect. An output when used as the negative rail of a DS1 or E1 output port operating in dual-rail mode. In CHI and PSB modes, it is used as the transmit system frame synchronization input. In NSMI mode, it is the transmit system frame sync output.
AB19	RXDATAEN	LVCMOS	O	**NSMI Receive Enable.** Receive data enable for NSMI mode.
W22	TXDATAEN	LVCMOS	O	**NMSI Transmit Enable.** Transmit data enable for NSMI mode.

2.3.2 Framer PLL

The DS1/E1 framer has a phase-locked loop that may be used to generate a transmit line clock at 1.544 MHz or 2.048 MHz. The reference signal for this PLL may be chosen from a number of possible sources, all typically synchronized to the system clock (CHI transmit/receive clock, for example). In order to ensure reliable performance, this PLL has its own isolated power pins. The PLL also has a number of test control pins that are used for factory testing only.

The PLL is active when framer bit FRM_PLL_BYPAS = 0. When FRM_PLL_BYPAS = 1, the PLL is bypassed and an external clock at the system interface is used as the line clock. An example would be when the framers are programmed for a CHI interface at 2.048 MHz and the frames are programmed for E1, the PLL may be bypassed and the CHI system clock may be used as the line clock.

Table 2-8. Framer PLL

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>I/O</th><th>Description</th></tr>
<tr><td>AD24</td><td>CLKIN_PLL</td><td>LVCMOS</td><td>I
Pull-down</td><td>Clock In PLL. Phase locked-loop reference clock input. Frequency should be consistent with the MODE_PLL pins in the PLL Mode1 table below. A 1.544 MHz/2.048 MHz clock for DS1/E1 transmit outputs is generated synchronous to this clock.</td></tr>
<tr><td>AB21, AE24, AF24</td><td>MODE[2:0]_PLL</td><td>LVCMOS</td><td>I
Pull-down</td><td>PLL Mode 1. PLL control input 1. The PLL mode inputs should be hardwired to the logic levels shown in the table below, depending on the frequency of the reference supplied to CLKIN_PLL.
<table>
<tr><th>Mode[2:0]</th><th>CLKIN_PLL</th><th>Mode[2:0]</th><th>CLKIN_PLL</th></tr>
<tr><td>000</td><td>Reserved</td><td>100</td><td>16.384 MHz</td></tr>
<tr><td>001</td><td>51.84 MHz</td><td>101</td><td>8.192 MHz</td></tr>
<tr><td>010</td><td>26.62 MHz</td><td>110</td><td>4.096 MHz</td></tr>
<tr><td>011</td><td>19.44 MHz</td><td>111</td><td>2.048 MHz</td></tr>
</table></td></tr>
</table>

Table 2-9. Microprocessor Interfaces

Pin	Symbol	Type	I/O	Description
AE17	MPCLK	LVCMOS	I	**Processor Clock.** This is the synchronous microprocessor clock (when MPMODE = 1). The maximum clock frequency is 60 MHz. This clock is required to properly sample address, data, and control signals from the microprocessor in both asynchronous and synchronous modes of operation. This clock must be within the range of 16 MHz—60 MHz.
AD17	MPMODE	LVCMOS	I	**Control Port Mode.** If the microprocessor interface is synchronous, MPMODE should be high. If the microprocessor interface is asynchronous, MPMODE should be set to 0.
AC18	CSN	LVCMOS	I Pull-up	**Chip Select.** Active-low chip select. For synchronous mode, it should be stable beyond a certain setup time before the rising clock edge when ADSN is active. For asynchronous mode, it should be stable before DSN is asserted.
AE18	ADSN	LVCMOS	I	**Address Strobe.** Active-low address strobe that is a 1 MPCLK cycle wide pulse for synchronous mode and active for the entire read/write cycle for asynchronous mode. Address bus signals, ADDR[19:0], are transparently latched into Superframer when ADSN is low. The address bus should remain valid for the duration of ADSN.
AF18	RWN	LVCMOS	I	**Read/Write Cycle Selection.** RWN is set high for a read operation, or set low for write operation.
AD18	DSN	LVCMOS	I	**Data Strobe.** DSN is not used for synchronous mode. For asynchronous mode, write operation DSN becomes active after data is stable. For read operation, it is similar to ADSN.
AB23, AC26, AC24, AD25, AD26, AE25, AA22, AC22, AE22, AD21, AE21, AC21, AD20, AF20, AE20, AC20, AD19, AF19, AE19, AC19	ADDR[19:0]	LVCMOS	I	**Address [19:0].** ADDR19 is the most significant and ADDR0 the least significant bit for addressing all the internal Superframer registers during CPU access cycles. **Note:** The Superframer is little endian; the least significant byte is stored in the lowest address and the most significant byte is stored in the highest address. Care must be exercised in connection to microprocessors that use big-endian byte ordering.
AB25, AA24, AA25, AA23, Y24, Y26, Y25, Y23, W24, W26, W25, W23, V24, V26, V25, V23	DATA[15:0]	LVCMOS	I/O	**Data [15:0].** Data bus for all transfers between the CPU and the internal Superframer registers. The pins are inputs during write cycles and outputs during read cycles. DATA15 is the MSB, and DATA0 is the LSB.
U24, U25	PAR[1:0]	LVCMOS	I/O	**CPU Port Parity [1:0].** Byte-wide parity bits for data. PAR[1] is the parity for DATA[15:8], and PAR[0] is the parity for DATA[7:0].

Table 2-9. Microprocessor Interfaces (cont)

Pin	Symbol	Type	I/O	Description
U23	DTN	LVCMOS	O Open Drain	**Data Transfer Acknowledge.** In synchronous CPU mode, DTN goes low at the fourth cycle for write or the fifth cycle for read, resulting in a fixed two wait-states for writes and three wait-states for reads. In asynchronous CPU mode, after qualification of ADSN and DSN by the MPCLK clock, DTN goes low for two MPCLK clock cycles for writes and three MPCLK clock cycles for reads. DTN goes high with the rising edge of ASDN.
AB24	INTN	LVCMOS	O Open Drain	**Interrupt.** Superframer interrupt request, active-low.This is an open-drain output and should be connected to an external pull-up resistor.
AC25	APS_INTN	LVCMOS	O Open Drain	**APS Interrupt.** Automatic protection switch interrupt request, active-low. This an open-drain output and should be connected to an external pull-up resistor.

Table 2-10. General-Purpose Interface

Pin	Symbol	Type	I/O	Description
T24	RSTN	LVCMOS	I Pull-up	**Reset.** Global reset, active-low. Initializes all internal registers to their default state.
T25	PMRST	LVCMOS	I/O Pull-down	**Performance Monitor Reset.** May be configured as an input and then used to directly reset all the counters associated with DS1/E1 performance monitoring. If an internal PM reset is used, PMRST is configured as an output that indicates when a PM reset occurred.
R5	TCK	LVCMOS	I	**Test Clock.** This signal provides timing for the boundary scan and TAP controller. This signal should be static, except during boundary-scan testing.
P5	IDDQ	LVCMOS	I Pull-up	**Do Not Connect.**
U5	TDI	LVCMOS	I Pull-up	**Test Data In.** Data input for the boundary scan; sampled on the rising edge of TCK.
W5	TMSN	LVCMOS	I Pull-up	**Test Mode Select (Active-Low).** Controls boundary-scan test operations. TMSN is sampled on the rising edge of TCK.
AB8	TRSTN	LVCMOS	I Pull-down	**Test Reset (Active-Low).** This signal is an asynchronous reset for the TAP controller.
V5	TDO	LVCMOS	O	**Test Data Out.** Updated on the falling edge of TCK. The TDO output is high impedance, except when scanning out test data.
AB9	IC3STATEN	LVCMOS	I Pull-up	**Global Output Enable.** All output and bidirectional buffers will be high impedance when this input is low. Normally pulled high internally.

2.3.3 Test Pins

These pins are for factory test purposes only and must be connected properly. They are used to establish special configurations for testing, inserting test data, etc. For normal operation, they should be left unconnected; each is equipped with a pull-up or pull-down to the inactive (normal operation) state.

Table 2-11. Test Pins

Pin	Symbol	Type	I/O	Description
N5	SCAN_EN	LVCMOS	I Pull-down	**Test Only.** Scan enable (active-high).
M5	SCAN_MODE	LVCMOS	I Pull-down	**Test Only.** Serial scan input for testing (active-high).
AE14	BYPASS	LVCMOS	I Pull-down	**Test Only.** Enables functional bypassing of the clock synthesis with a test clock (active-high).
AF14	TSTPHASE	LVCMOS	I Pull-down	**Test Only.** Controls bypass of 32 PLL-generated phases with 32 low-speed phases, generated by test logic (active-high).
AD14	ECSEL	LVCMOS	I Pull-down	**Test Only.** Enables external test control of 155 MHz clock phase selection through ETOGGLE and EXDNUP inputs (active-high).
AC15	ETOGGLE	LVCMOS	I Pull-down	**Test Only.** Moves 155 MHz clock selection one phase per positive pulse > 20 ns. Active + pulse.
AE15	EXDNUP	LVCMOS	I Pull-down	**Test Only.** Direction of phase changes. 0 = down. 1 = up.
AF15	TSTMODE	LVCMOS	I Pull-down	**Test Only.** Enables test mode.
AD15	TSTSFTLD	LVCMOS	I Pull-down	**Test Only.** Enables test mode shift register.
AE16, AC16	TSTMUX[1:0]	LVCMOS	O	**Test Only.** Test mode output.

Table 2-12. Analog Power and Ground Signals

Pin	Symbol	Type	Name/Description
AC9	V_{DDA_CDR}	—	**CDR Power.** 3.3 V power supply for the internal CDR. Good engineering practice needs to be applied to minimize noise on this pin.
AB12	V_{SSA_CDR}	—	**CDR Ground.** Isolated ground for the internal CDR.
AE23	V_{DDS_PLL}	—	**Analog V_{DD} for PLL.** 3.3 V power supply for the framer's PLL. Good engineering practice needs to be applied.
AF23	V_{SSA_PLL}	—	**Analog PLL Ground.** Analog ground for PLL.
AD22	V_{DDD_PLL}	—	**Digital PLL Power.** Digital 3.3 V for PLL. Good engineering practice needs to be applied to minimize noise on this pin.
AD23	V_{SSS_PLL}	—	**Digital Ground for PLL.** Digital ground for PLL. Good engineering practice needs to be applied.

3 Pin Assignment Matrix

Table 3-1. Pin Matrix

	A	B	C	D	E	F	G	H	J
1	VDD	VSS	LINERXSYNC15	LINERXSYNC14	VDD	VSS	LINERXSYNC11	LINERXDATA9	LINERXCLK8
2	VSS	LINERXCLK15	LINERXDATA14	LINERXDATA13	LINERXDATA12	LINERXSYNC12	LINERXDATA10	LINERXCLK9	LINERXSYNC8
3	LINERXDATA17	LINERXSYNC18	LINERXCLK17	LINERXCLK14	LINERXCLK13	LINERXCLK12	LINERXCLK11	LINERXSYNC10	LINERXDATA8
4	LINERXDATA18	LINERXSYNC19	LINERXCLK18	VSS	LINERXSYNC13	LINERXDATA11	LINERXCLK10	LINERXSYNC9	LINERXDATA7
5	VDD	LINERXSYNC20	LINERXCLK19	LINERXDATA19	VDD	LINERXDATA15	VSS	LINERXDATA16	LINERXCLK16
6	VSS	LINERXDATA20	LINERXCLK20	LINERXSYNC21	LINERXSYNC17	—	—	—	—
7	LINERXDATA21	LINERXSYNC22	LINERXCLK21	LINERXCLK22	VSS	—	—	—	—
8	LINERXSYNC23	LINERXCLK23	LINERXDATA22	LINERXDATA23	TDLDATA	—	—	—	—
9	LINERXCLK24	LINERXDATA24	LINERXSYNC24	LINERXSYNC25	TDLCLK	—	—	—	—
10	VDD	LINERXDATA25	LINERXCLK25	LINERXSYNC26	DS2AISCLK	—	—	—	—
11	VSS	LINERXDATA26	LINERXCLK26	LINERXSYNC27	VDD	—	—	—	—
12	LINERXDATA27	LINERXSYNC28	LINERXCLK27	LINERXCLK28	TCBDATA	—	—	—	—
13	LINERXSYNC29	LINERXCLK29	LINERXDATA28	LINERXDATA29	TCBCLK	—	—	—	—
14	LINETXDATA1	LINETXCLK1	LINETXSYNC2	LINETXSYNC1	TCBSYNC	—	—	—	—
15	LINETXSYNC3	LINETXDATA2	LINETXCLK3	LINETXCLK2	RCBDATA	—	—	—	—
16	VSS	LINETXSYNC4	LINETXCLK4	LINETXDATA3	VDD	—	—	—	—
17	VDD	LINETXSYNC5	LINETXCLK5	LINETXDATA4	RCBCLK	—	—	—	—
18	LINETXCLK6	LINETXSYNC6	LINETXDATA6	LINETXDATA5	RCBSYNC	—	—	—	—
19	LINETXDATA7	LINETXCLK7	LINETXSYNC8	LINETXSYNC7	RDLCLK	—	—	—	—
20	LINETXSYNC9	LINETXDATA8	LINETXCLK9	LINETXCLK8	VSS	—	—	—	—
21	VSS	LINETXSYNC10	LINETXCLK10	LINETXDATA9	LINETXDATA13	—	—	—	—
22	VDD	LINETXDATA10	LINETXCLK11	LINETXSYNC11	VDD	LINETXSYNC14	VSS	RDLDATA	DS3DATAINCLK
23	LINETXSYNC12	LINETXDATA11	LINETXCLK12	VSS	LINETXDATA16	LINETXSYNC18	LINETXCLK19	LINETXDATA20	LINETXSYNC22
24	LINETXSYNC13	LINETXDATA12	LINETXCLK14	LINETXCLK15	LINETXCLK16	LINETXCLK17	LINETXCLK18	LINETXDATA19	LINETXSYNC21
25	VSS	LINETXCLK13	LINETXSYNC15	LINETXSYNC16	LINETXSYNC17	LINETXDATA17	LINETXSYNC19	LINETXCLK20	LINETXDATA21
26	VDD	VSS	LINETXDATA14	LINETXDATA15	VDD	VSS	LINETXDATA18	LINETXSYNC20	LINETXCLK21

Table 3-1. Pin Matrix (continued)

	K	L	M	N	P	R	T	U	V
1	VDD	VSS	LINERXSYNC5	LINERXDATA3	LINERXSYNC2	NC	VSS	VDD	NC
2	LINERXSYNC7	LINERXSYNC6	LINERXDATA4	LINERXCLK3	LINERXCLK2	LINERXSYNC1	NC	NC	NC
3	LINERXCLK7	LINERXCLK6	LINERXCLK5	LINERXSYNC4	LINERXDATA1	NC	NC	NC	NC
4	LINERXDATA6	LINERXDATA5	LINERXCLK4	LINERXSYNC3	LINERXDATA2	LINERXCLK1	NC	NC	NC
5	LINERXSYNC16	VDD	SCAN_MODE	SCAN_EN	IDDQ	TCK	VDD	TDI	TDO
6	—	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	—	—	—
11	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
12	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
13	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
14	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
15	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
16	—	VSS	VSS	VSS	VSS	VSS	VSS	—	—
17	—	—	—	—	—	—	—	—	—
18	—	—	—	—	—	—	—	—	—
19	—	—	—	—	—	—	—	—	—
20	—	—	—	—	—	—	—	—	—
21	—	—	—	—	—	—	—	—	—
22	DS3NEGDATAIN	VDD	DS3POSDATAIN	DS3DATAOUTCLK	DS3NEGDATAOUT	DS3POSDATAOUT	VDD	PHASEDETDOWN	PHASEDETUP
23	LINETXSYNC23	LINETXSYNC24	LINETXCLK25	LINETXDATA26	LINETXSYNC27	LINETXCLK28	LINETXDATA29	DTN	DATA0
24	LINETXCLK22	LINETXCLK23	LINETXCLK24	LINETXDATA25	LINETXSYNC28	LINETXCLK29	RSTN	PAR1	DATA3
25	LINETXDATA22	LINETXDATA23	LINETXSYNC25	LINETXCLK26	LINETXCLK27	LINETXDATA28	PMRST	PAR0	DATA1
26	VDD	VSS	LINETXDATA24	LINETXSYNC26	LINETXDATA27	LINETXSYNC29	VSS	VDD	DATA2

Table 3-1. Pin Matrix (continued)

	W	Y	AA	AB	AC	AD	AE	AF
1	NC	NC	VSS	VDD	NC	NC	VSS	VDD
2	NC	NC	NC	NC	NC	NC	NC	VSS
3	NC	NC	NC	NC	NC	NC	NC	NC
4	NC	NC	NC	NC	VSS	NC	NC	NC
5	TMSN	VSS	NC	VDD	NC	NC	NC	VDD
6	—	—	—	NC	NC	NC	NC	VSS
7	—	—	—	VSS	NC	NC	NC	NC
8	—	—	—	TRSTN	NC	NC	NC	NC
9	—	—	—	IC3STATEN	VDDA_CDR	NC	NC	NC
10	—	—	—	NC	NC	NC	NC	VDD
11	—	—	—	VDD	NC	NC	NC	VSS
12	—	—	—	VSSA_CDR	NC	NC	NC	NC
13	—	—	—	NC	NC	NC	NC	NC
14	—	—	—	NC	NC	ECSEL	BYPASS	TSTPHASE
15	—	—	—	NC	ETOGGLE	TSTSFTLD	EXDNUP	TSTMODE
16	—	—	—	VDD	TSTMUX0	DS1XCLK	TSTMUX1	VSS
17	—	—	—	NC	E1XCLK	MPMODE	MPCLK	VDD
18	—	—	—	NC	CSN	DSN	ADSN	RWN
19	—	—	—	RXDATAEN	ADDR0	ADDR3	ADDR1	ADDR2
20	—	—	—	VSS	ADDR4	ADDR7	ADDR5	ADDR6
21	—	—	—	MODE2_PLL	ADDR8	ADDR10	ADDR9	VSS
22	TXDATAEN	VSS	ADDR13	VDD	ADDR12	VDDD_PLL	ADDR11	VDD
23	DATA4	DATA8	DATA12	ADDR19	VSS	VSSS_PLL	VDDS_PLL	VSSA_PLL
24	DATA7	DATA11	DATA14	INTN	ADDR17	CLKIN_PLL	MODE1_PLL	MODE0_PLL
25	DATA5	DATA9	DATA13	DATA15	APS_INTN	ADDR16	ADDR14	VSS
26	DATA6	DATA10	VSS	VDD	ADDR18	ADDR15	VSS	VDD

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 4-1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
dc Supply Voltage Range	V_{DD}	–0.5	4.6	V
Storage Temperature Range	Tstg	–65	125	°C
Maximum Voltage (digital input pins)	—	—	5.25	V
Minimum Voltage (digital input pins)	—	–0.3	—	V

4.2 Thermal Parameters (Definitions and Values)

System and circuit board level performance depends not only on device electrical characteristics, but also on device thermal characteristics. The thermal characteristics frequently determine the limits of circuit board or system performance, and they can be a major cost adder or cost avoidance factor. When the die temperature is kept below 125 °C, temperature activated failure mechanisms are minimized. The thermal parameters that Agere provides for its packages help the chip and system designer choose the best package for their applications, including allowing the system designer to thermally design and integrate their systems.

It should be noted that all the parameters listed below are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

Θ_{JA}—Junction to Air Thermal Resistance

Θ_{JA} is a number used to express the thermal performance of a part under JEDEC standard natural convection conditions. Θ_{JA} is calculated using the following formula:

$\Theta_{JA} = (T_J – T_{amb})/P$; where P = power

Θ_{JMA}—Junction to Moving Air Thermal Resistance

Θ_{JMA} is effectively identical to Θ_{JA} but represents performance of a part mounted on a JEDEC four layer board inside a wind tunnel with forced air convection. Θ_{JMA} is reported at airflows of 200 lft./min and 500 lft./min, which roughly correspond to 1 m/s and 2.5 m/s (respectively). Θ_{JMA} is calculated using the following formula:

$\Theta_{JMA} = (T_J – T_{amb})/P$

Θ_{JC}—Junction to Case Thermal Resistance

Θ_{JC} is the thermal resistance from junction to the top of the case. This number is determined by forcing nearly 100% of the heat generated in the die out the top of the package by lowering the top case temperature. This is done by placing the top of the package in contact with a copper slug kept at room temperature using a liquid refrigeration unit. Θ_{JC} is calculated using the following formula:

$\Theta_{JC} = (T_J – T_C)/P$

Θ_{JB}—Junction to Board Thermal Resistance

Θ_{JB} is the thermal resistance from junction to board. This number is determined by forcing the heat generated in the die out of the package through the leads or balls by lowering the board temperature and insulating the package top. This is done using a special fixture, which keeps the board in contact with a water chilled copper slug around the perimeter of the package while insulating the package top. Θ_{JB} is calculated using the following formula:

$\Theta_{JB} = (T_J - T_B)/P$

Ψ_{JT}

Ψ_{JT} correlates the junction temperature to the case temperature. It is generally used by the customer to infer the junction temperature while the part is operating in their system. It is not considered a true thermal resistance. Ψ_{JT} is calculated using the following formula:

$\Psi_{JT} = (T_J - T_C)/P$

Table 4-2. Thermal Parameter Values

Parameter	Temperature °C/Watt
Θ_{JA}	15.1
Θ_{JMA} (1 m/s)	11.8
Θ_{JMA} (2.5 m/s)	10.3
Θ_{JC}	4.2
Θ_{JB}	10.1
Ψ_{JT}	1.0

4.3 Reliability

Product reliability can be calculated as the probability that the product will perform under normal operating conditions for a set period of time. Factors influencing the reliability of a product cover a range of variables, including design and manufacturing. The failure rate of a product is given as the number of units failing per unit time. This failure rate is known as FIT, which is as follows:

1 FIT = 1 Failure/1x10e^9 hours.

Another unit used for failure rate is known as MTBF, which is 1/FIT. Many assumptions are made when calculating the failure rate for a product, such as the average junction temperature and activation energy. The assumptions made for calculating FIT and MTBF are shown in Table 4-3.

Table 4-3. Reliability Data

Junction Temperature	FIT (Per 10e^9 Device Hours	MTBF	Activation Energy
55 °C	34	2.9e^7 hours	.7eV

4.4 Handling Precautions

Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

Table 4-4. Handling Precaution

Device	Minimum HBM Threshold	Minimum CDM Threshold	
		Corner	Noncorner
TFRA28J13	2000 V	500 V	500 V

4.5 Operating Conditions

The following tables list the voltages required for proper operation of the TFRA28J13 device, along with their tolerances.

Table 4-5. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power	V_{DD}	3.14	3.3	3.47	V
Ground	V_{SS}	—	0.0	—	V
Ambient Operating Temperature Range	T_A	–40	—	85	°C

* Internal reference voltage is used if SMPR_LVDS_REF_SEL = 1, or else external voltage is used.

4.5.1 Power Consumption

Table 4-6. Power Consumption

Parameter	Typical Power*	Unit
V_{DD} = 3.5 V, T_A = 25 °C	3.185	W
V_{DD} = 3.3 V, T_A = 25 °C	2.772	W
V_{DD} = 3.0 V, T_A = 25 °C	2.190	W

* When measuring power consumption of the Superframer, the following blocks are powered on: TMUX, SPEMPR, VTMPR, DJA, FRAMER. MPCLK = 25 MHz.

4.6 Logic Interface Characteristics

Table 4-7. Logic Interface Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Current:					
Low	I_{OL}	—	—	4.0	mA
High	I_{OH}	—	—	4.0	mA
Output Voltage:					
Low	V_{OL}	—	V_{SS}	0.5	V
High	V_{OH}	—	V_{DD} – 0.5	3.465	V
Input Capacitance	C_I	—	—	1.5	pF
Input Leakage	I_L	—	—	1.0	µA
Input Voltage, High	V_{IH}	—	V_{DD} – 1.0	5.25	V
Input Voltage, Low	V_{IL}	—	V_{SS}	1.0	V

The input specification for the remaining (nonbalanced) inputs are specified in Figure 4-1.

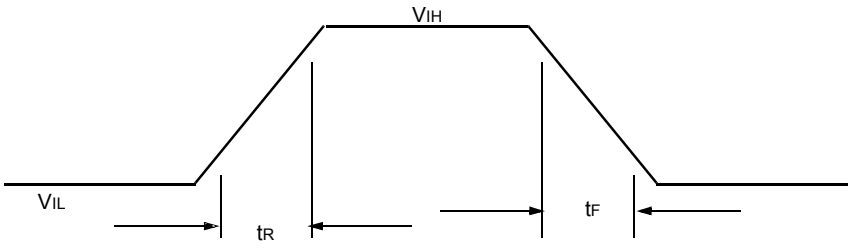

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Figure 4-1. Single-Ended Input Specification

4.7 DS3 Timing

Table 4-8. DS3 Input Clock Specifications

Symbol	Parameter	Signal Name	Min	Max	Unit
F_{CK}	Clock Frequency	DS3DATAINCLK DS3DATAOUTCLK	—	44.736 ± 50 ppm	MHz
t_{CK}	Clock Period	DS3DATAINCLK DS3DATAOUTCLK	—	22.353	ns
t_{CLKHI}	Clock Pulse High Time	DS3DATAINCLK DS3DATAOUTCLK	6 6	16 12	ns ns
t_R	Rise Time	DS3DATAINCLK DS3DATAOUTCLK	0	2	ns
t_F	Fall Time	DS3DATAINCLK DS3DATAOUTCLK	0	2	ns

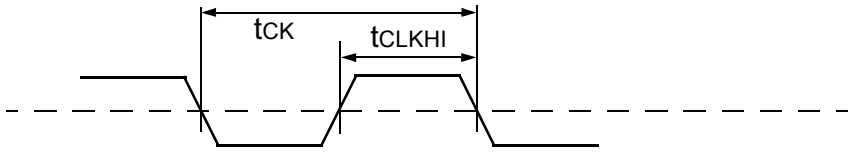

Figure 4-2. DS3DATAOUTCLK Timing

Table 4-9. Input Timing Specifications

Input Name	Reference CLK	Min Setup Time (ts)	Min Hold Time (t_H)	Unit
DS3POSDATAIN	DS3DATAINCLK ↑↓*	4	0	ns
DS3NEGDATAIN	DS3DATAINCLK ↑↓*	4	0	ns

* Register 0x100A1, bit 0, M13_RDS3_EDGE. Register 0x30019, bit 5, SPE_TDS3CLK_EDGE.

Table 4-10. Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay t_{PD}		Unit
			Min	Max	
DS3POSDATAOUT	DS3DATAOUTCLK ↑	C_L = 15 pF	2	6.5	ns
DS3NEGDATAOUT	DS3DATAOUTCLK ↑	C_L = 15 pF	2	6.5	ns

4.8 M13 Timing

Table 4-11. M13 Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
F_{CK}	Clock Frequency	TCBCLK	—	93.983 gapped	—	kHz
		TDLCLK	—	28.195 gapped	—	kHz
		E1XCLK	2.048	32.768	65.536	MHz
		DS1XCLK	1.544	24.704	49.408	MHz
		DS2AISCLK	—	6.312	—	MHz
		RCBCLK	—	93.983	—	kHz
		RDLCLK	—	28.195	—	kHz
t_{CLKHI}	Clock Pulse High Time	TCBCLK	212.19	223.53	250.77	ns
		TDLCLK	212.19	223.53	250.77	ns
		RCBCLK	212.19	223.53	250.77	ns
		RDLCLK	212.19	223.53	250.77	ns
t_R	Rise Time	TCBCLK	0	—	3	ns
		TDLCLK	0	—	3	ns
		E1XCLK	0	—	3	ns
		DS1XCLK	0	—	3	ns
		DS2AISCLK	0	—	3	ns
		RCBCLK	0	—	3	ns
		RDLCLK	0	—	3	ns
t_F	Fall Time	TCBCLK	0	—	3	ns
		TDLCLK	0	—	3	ns
		E1XCLK	0	—	3	ns
		DS1XCLK	0	—	3	ns
		DS2AISCLK	0	—	3	ns
		RCBCLK	0	—	3	ns
		RDLCLK	0	—	3	ns

Table 4-12. Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (t_H)		Unit
		Min	Max	Min	Max	
TCBDATA	TCBCLK ↑	50	—	0	—	ns
TDLDATA	TDLCLK ↑	50	—	0	—	ns

Table 4-13. Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay t_{PD}		Unit
			Min	Max	
TCBSYNC	TCBCLK ↑	C_L = 15 pF	0.5	10	ns
RCBSYNC	RCBCLK ↑	C_L = 15 pF	0.5	10	ns
RCBDATA	RCBCLK ↑	C_L = 15 pF	0.5	10	ns
RDLDATA	RDLCLK ↑	C_L = 15 pF	2	10	ns

4.9 Concentration Highway (CHI) Timing

Table 4-14 and Table 4-15 with Figure 4-3 and Figure 4-4, respectively, illustrate the detailed CHI timing for clock, data, and frame synchronization.

Table 4-14. CHI Transmit Timing Characteristics

Symbol	Parameter	Min	Max	Unit
F_{CK}	Clock Frequency*	2.048	16.384	MHz
t_{CK}	Clock Period	488.2	61.04	ns
t_R	Clock Rise Time	0	3	ns
t_F	Clock Fall Time	0	3	ns
t_S†	Frame Sync Setup Time	35	—	ns
t_H†	Frame Sync Hold Time	0	—	ns
t_{PD}†	Clock to CHI Data Delay	—	25	ns

* Fck can be either 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz.
† tS, tH, and tPD,⇒ LINETXCLK29 ↑↓ (Register 0x80050, bit 4, FRM_TFSCKE).

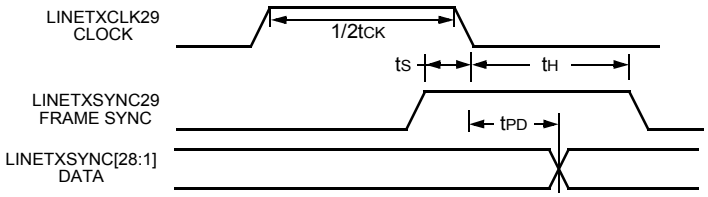

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Figure 4-3. CHI Transmit I/O Timing

Table 4-15. CHI Receive Timing Characteristics

Symbol	Parameter	Min	Max	Unit
F_{CK}	Clock Frequency*	2.048	16.384	MHz
t_{CK}	Clock Period	488.2	61.04	ns
t_R	Clock Rise Time	0	3	ns
t_F	Clock Fall Time	0	3	ns
t_{SSYNC}†	Frame Sync Setup Time	30	—	ns
t_{HSYNC}†	Frame Sync Hold Time	3.4	—	ns
t_{SDATA}†	CHI Data Setup Time	25	—	ns
t_{HDATA}†	CHI Data Hold Time	0	—	ns

* FCK can be either 2.048 MHz, 4.096 MHz, 8.192 MHz, or 16.384 MHz.
† LINERXSYNC29 ↑↓ (Register 0x80150, bit 13, FRM_RFSCKE).

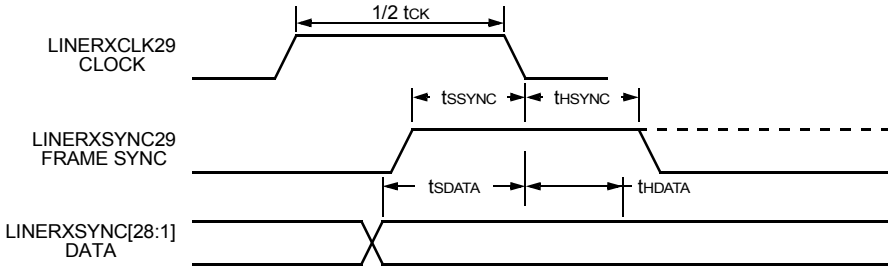

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Figure 4-4. CHI Receive I/O Timing

4.10 Parallel System Bus Timing

Table 4-16 and Table 4-17 with Figure 4-5 and Figure 4-6, respectively, show the transmit and receive timing. In the transmit direction (to the system interface), the frame sync is sampled and the data is clocked out on the rising edge of the clock. In the receive direction (from the switch), the data and frame sync are sampled on the rising edge of the clock.

Table 4-16. PSB Interface Transmit Timing Characteristics

Symbol	Parameter	Min	Max	Unit
FCK	Clock Frequency	19.44	19.44	MHz
tCK	Clock Period	51.44	51.44	ns
tR	Clock Rise Time	0	3	ns
tF	Clock Fall Time	0	3	ns
tS*	Frame Sync Setup Time	8	—	ns
tH*	Frame Sync Hold Time	0	—	ns
tPD*	Clock to PSB Out Delay	3	10	ns

* LINETXCLK29 ↑↓ (Register 0x80050, bit 4, FRM_TFSCKE).

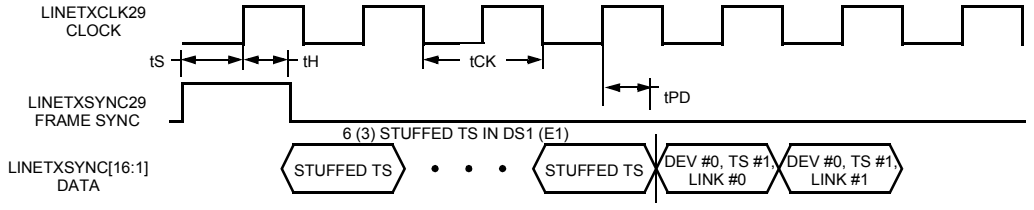


Figure 4-5. Parallel System Bus Interface Transmit I/O Timing

Table 4-17. PSB Interface Receive Timing Characteristics

Symbol	Parameter	Min	Max	Unit
FCK	Clock Frequency	19.44	19.44	MHz
tCK	Clock Period	51.44	51.44	ns
tR	Clock Rise Time	0	3	ns
tF	Clock Fall Time	0	3	ns
tSSYNC*	Frame Sync Setup Time	8	—	ns
tHSYNC*	Frame Sync Hold Time	0	—	ns
tSDATA*	PSB to Clock Setup Time	8	—	ns
tHDATA*	PSB Hold Time from Clock	2.8	—	ns

* LINERXCLK29 ↑↓ (Register 0x80150, bit 13, FRM_RFSCKE).

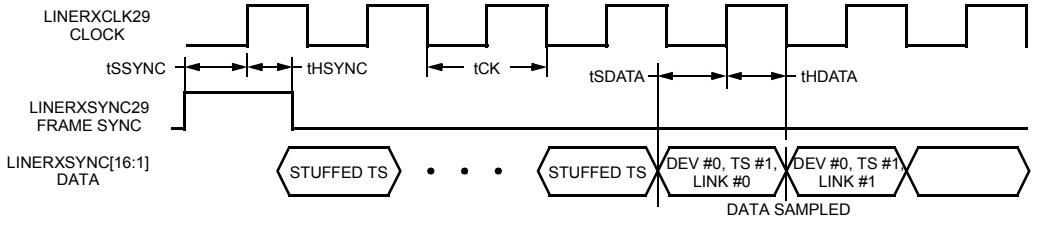


Figure 4-6. Parallel System Bus Interface Receive I/O Timing

4.11 NSMI Timing (6-Pin) (to/from Framer)

Table 4-18. NSMI Input/Output Clock Specifications

Symbol	Parameter	Signal Name	I/O	Min	Nom	Max	Unit
F_{CK}	Clock Frequency	LINETXCLK29 LINERXCLK29	Output Input	–50 ppm –50 ppm	51.84 51.84	50 ppm 50 ppm	MHz MHz
$t_{CK} = 1/F_{CK}$	Clock Period	LINETXCLK29 LINERXCLK29	Output Input	— —	19.29 19.29	— —	ns ns
t_{CKHI}	Clock Pulse High Time	LINETXCLK29 LINERXCLK29	Output Input	6 6	— —	12 12	ns ns
t_R	Rise Time	LINETXCLK29 LINERXCLK29	Output Input	— —	— —	3 3	ns ns
t_F	Fall Time	LINETXCLK29 LINERXCLK29	Output Input	— —	— —	3 3	ns ns

Table 4-19. Input Timing Specifications

Input Name	Reference CLK	Setup Time (t_S)		Hold Time (t_H)		Unit
		Min	Max	Min	Max	
LINERXDATA29	LINERXCLK29 ↑	3	—	0	—	ns
LINERXSYNC29	LINERXCLK29 ↑	3	—	0.5	—	ns

Table 4-20. Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay t_{PD}		Unit
			Min	Max	
LINETXDATA29	LINETXCLK29 ↑	C_L = 15 pF	0.1	3.0	ns
LINETXSYNC29	LINETXCLK29 ↑	C_L = 15 pF	0.1	5.0	ns

4.12 NSMI Timing (7-Pin) (to/from Framer)

Table 4-21. NSMI Output Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
FCK	Clock Frequency	LINETXCLK29 LINERXCLK29 RXDATAEN	–50 ppm –50 ppm –50 ppm	51.84/44.736 51.84/44.736 51.84/44.736	50 ppm 50 ppm 50 ppm	MHz MHz MHz
$t_{CK} = 1/F_{CK}$	Clock Period	LINETXCLK29 LINERXCLK29 RXDATAEN	— — —	19.29/22.35 19.29/22.35 19.29/22.35	— — —	ns ns ns
t_{CKHI}	Clock Pulse High Time	LINETXCLK29 LINERXCLK29 RXDATAEN	6 6 —	1/2 tck 1/2 tck 1/2 tck	— — —	ns ns ns
t_R	Rise Time	LINETXCLK29 LINERXCLK29 RXDATAEN	0 0 0	— — —	3 3 3	ns ns ns
t_F	Fall Time	LINETXCLK29 LINERXCLK29 RXDATAEN	0 0 0	— — —	3 3 3	ns ns ns

Table 4-22. NSMI Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (t_H)		Unit
		Min	Max	Min	Max	
LINERXDATA29	LINERXCLK29 ↑	3.0	—	0	—	ns
LINERXSYNC29	LINERXCLK29 ↑	3.0	—	0.5	—	ns

Table 4-23. NSMI Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay t_{PD}		Unit
			Min	Max	
LINETXDATA29	LINETXCLK29 ↑	C_L = 15 pF	0.1	3.0	ns
LINETXSYNC29	LINETXCLK29 ↑	C_L = 15 pF	0.1	5.0	ns
TXDATAEN	LINETXCLK29 ↑	C_L = 15 pF	–0.6	0.2	ns

4.13 CHI Interface Timing

Table 4-24. CHI Interface Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
F_{CK}	Clock Frequency	LINERXDATA29	–130 ppm	1.544 or 2.048	130 ppm	MHz
		LINERXCLK29	–50 ppm	2.048 or 4.096 or 8.192 or 16.384	50 ppm	MHz
		LINETXCLK29	–50 ppm	2.048 or 4.096 or 8.192 or 16.384	50 ppm	MHz
$t_{CK} = 1/F_{CK}$	Clock Period	LINERXDATA29 LINERXCLK29 LINETXCLK29	—	647.67 or 488.28 488.28, or 244.14 or 122.07, or 61.04 488.28, or 244.14 or 122.07, or 61.04	—	ns ns ns ns ns
t_{CKHI}	Clock Pulse High Time	LINERXDATA29, LINERXCLK29 LINETXCLK29	—	1/2 tck	—	ns
t_R	Rise Time	LINERXDATA29, LINERXCLK29 LINETXCLK29	0	—	3	ns
t_F	Fall Time	LINERXDATA29, LINERXCLK29 LINETXCLK29	0	—	3	ns

Table 4-25. CHI Interface Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (t_H)		Unit
		Min	Max	Min	Max	
LINERXSYNC[28:1]	LINERXCLK[28:1] ↑↓	25	—	0	—	ns
LINERXSYNC29	LINERXCLK29 ↑↓	30	—	3.4	—	ns
LINETXSYNC29	LINETXCLK29 ↑↓	35	—	1.6	—	ns

Table 4-26. CHI Interface Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay t_{PD}		Unit
			Min	Max	
LINETXSYNC[28:1]	LINETXCLK29 ↑↓	C_L = 15 pF	—	25	ns

4.14 PSB Interface Timing

Table 4-27. PSB Interface Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
FCK	Clock Frequency	LINERXDATA29 LINERXCLK29 LINETXCLK29	–130 ppm –50 ppm –50 ppm –50 ppm	1.544 or 2.048 19.44 19.44	130 ppm 50 ppm 50 ppm 50 ppm	MHz MHz MHz MHz
tCK = 1/FCK	Clock Period	LINERXDATA29 LINERXCLK29 LINETXCLK29	—	647.67 or 488.28 51.44 51.44	—	ns ns ns ns
tCKHI	Clock Pulse High Time	LINERXDATA29 LINERXCLK29 LINETXCLK29	—	1/2 tck 1/2 tck 1/2 tck 1/2 tck	—	ns ns ns ns
tR	Rise Time	LINERXDATA29 LINERXCLK29 LINETXCLK29	0 0 0 0	— — — —	3 3 3 3	ns ns ns ns
tF	Fall Time	LINERXDATA29 LINERXCLK29 LINETXCLK29	0 0 0 0	— — — —	3 3 3 3	ns ns ns ns

Table 4-28. PSB Interface Input Timing Specifications

Input Name	Reference CLK	Setup Time (tS)		Hold Time (tH)		Unit
		Min	Max	Min	Max	
LINERXSYNC[16:1]	LINERXCLK29 ↑↓	8	—	2.8	—	ns
LINERXSYNC29	LINERXCLK29 ↑↓	8	—	0	—	ns
LINETXSYNC29	LINETXCLK29 ↑↓	8	—	0	—	ns

Table 4-29. PSB Interface Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay tPD		Unit
			Min	Max	
LINETXSYNC[16:1]	LINETXCLK29 ↑↓	CL = 15 pF	3	10	ns

4.15 Framer DS1/E1 Interface Timing

Table 4-30. Framer DS1/E1 Interface Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
F_{CK}	Clock Frequency	LINERXCLK[29:1] LINETXCLK[29:1]	–130 ppm –50 ppm –130 ppm –50 ppm	1.544 or 2.048 1.544 or 2.048	130 ppm 50 ppm 130 ppm 50 ppm	MHz MHz MHz MHz
$t_{CK} = 1/F_{CK}$	Clock Period	LINERXCLK[29:1] LINETXCLK[29:1]	—	647.67 or 488.28 647.67 or 488.28	—	ns ns ns ns
t_{CKHI}	Clock Pulse High Time	LINERXCLK[29:1] LINETXCLK[29:1]	—	1/2 tck 1/2 tck	—	ns ns
t_R	Rise Time	LINERXCLK[29:1] LINETXCLK[29:1]	0 0	— —	3 3	ns ns
t_F	Fall Time	LINERXCLK[29:1] LINETXCLK[29:1]	0 0	— —	3 3	ns ns

Table 4-31. Framer DS1/E1 Interface Input Timing Specifications

Input Name	Reference CLK	Setup Time (t_S)		Hold Time (t_H)		Unit
		Min	Max	Min	Max	
LINERXDATA[29:1]	LINERXCLK[29:1] ↑↓	12.0	—	9.0	—	ns
LINERXSYNC[29:1]	LINERXCLK[29:1] ↑↓	12.0	—	9.0	—	ns

Table 4-32. Framer DS1/E1 Interface Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay t_{PD}		Unit
			Min	Max	
LINETXDATA[29:1]	LINETXCLK[29:1] ↑↓	C_L = 15 pF	0.5	10	ns
LINETXSYNC[29:1]	LINETXCLK[29:1] ↑↓	C_L = 15 pF	0.5	11	ns

4.16 DJA DS1/E1 Interface Timing

Table 4-33. DJA DS1/E1 Interface Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
F_{CK}	Clock Frequency	LINERXCLK[29:1] LINETXCLK[29:1]	–130 ppm –50 ppm –130 ppm –50 ppm	1.544 or 2.048 1.544 or 2.048	130 ppm 50 ppm 130 ppm 50 ppm	MHz MHz MHz MHz
$t_{CK} = 1/F_{CK}$	Clock Period	LINERXCLK[29:1] LINETXCLK[29:1]	—	647.67 or 488.28 647.67 or 488.28	—	ns ns ns ns
t_{CKHI}	Clock Pulse High Time	LINERXCLK[29:1] LINETXCLK[29:1]	—	1/2 tck 1/2 tck	—	ns ns
t_R	Rise Time	LINERXCLK[29:1] LINETXCLK[29:1]	0 0	— —	3 3	ns ns
t_F	Fall Time	LINERXCLK[29:1] LINETXCLK[29:1]	0 0	— —	3 3	ns ns

Table 4-34. DJA DS1/E1 Interface Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (t_H)		Unit
		Min	Max	Min	Max	
LINERXDATA[29:1]	LINERXCLK[29:1] ↑↓	NA	—	NA	—	ns

Table 4-35. DJA DS1/E1 Interface Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay t_{PD}		Unit
			Min	Max	
LINETXDATA[29:1]	LINETXCLK[29:1] ↑↓	C_L = 15 pF	–4.0	4.0	ns

4.17 M13 DS1/E1 Interface Timing

Table 4-36. M13 DS1/E1 Interface Clock Specifications

Symbol	Parameter	Signal Name	Min	Nom	Max	Unit
F_{CK}	Clock Frequency	LINERXCLK[29:1] LINETXCLK[29:1]	–130 ppm –50 ppm –130 ppm –50 ppm	1.544 or 2.048 1.544 or 2.048	130 ppm 50 ppm 130 ppm 50 ppm	MHz MHz MHz MHz
$t_{CK} = 1/F_{CK}$	Clock Period	LINERXCLK[29:1] LINETXCLK[29:1]	—	647.67 or 488.28 647.67 or 488.28	—	ns ns ns ns
t_{CKHI}	Clock Pulse High Time	LINERXCLK[29:1] LINETXCLK[29:1]	—	1/2 tck 1/2 tck	—	ns ns
t_R	Rise Time	LINERXCLK[29:1] LINETXCLK[29:1]	0 0	— —	3 3	ns ns
t_F	Fall Time	LINERXCLK[29:1] LINETXCLK[29:1]	0 0	— —	3 3	ns ns

Table 4-37. M13 DS1/E1 Interface Input Timing Specifications

Input Name	Reference CLK	Setup Time (ts)		Hold Time (t_H)		Unit
		Min	Max	Min	Max	
LINERXDATA[29:1]	LINERXCLK[29:1] ↑↓	12.0	—	8.0	—	ns

Table 4-38. M13 DS1/E1 Interface Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay t_{PD}		Unit
			Min	Max	
LINETXDATA[29:1]	LINETXCLK[29:1] ↑↓	C_L = 15 pF	–5.0	2.0	ns

4.18 Microprocessor Interface Timing

4.18.1 Synchronous Mode

The synchronous microprocessor interface mode is selected when MPMODE (pin AD17) = 1.

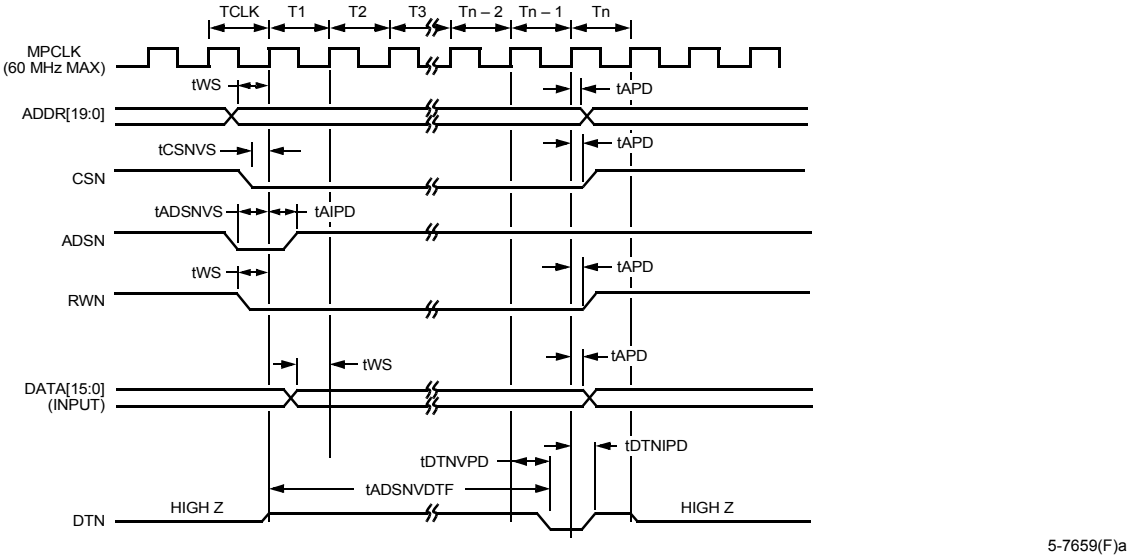


Figure 4-7. Microprocessor Interface Synchronous Write Cycle (MPMODE (Pin AD17) = 1)

MPCLK 16 MHz minimum to 60* MHz maximum frequency.

ADDR [19:0] The address will be available throughout the entire cycle.

DATA[15:0] Data will be available during cycle T1.

RWN (Input) The read (H) write (L) signal is always high except during a write cycle.

CSN (Input) Chip select is an active-low signal.

DTN (Output) Data transfer acknowledge is active-low for one clock and then driven high before entering a high-impedance state. (This is done with an I/O pad using the input as feedback to qualify the 3-state term.) DTN will become 3-stated when CSN is high. Typically, DTN is active 4 or 5 MPCLK cycles after ADSN is low.

ADSN (Input) Address strobe is active-low. ADSN must be 1 MPCLK clock period wide.

* If DTN is used, then the maximum frequency for MPCLK is determined by the processor's setup specification for DTN. For example, a 9 ns setup time would limit MPCLK to 40 MHz for reliable DTN detection.

Table 4-39. Microprocessor Interface Synchronous Write Cycle Specifications

Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Max)	Unit
t_{CLK}	MPCLK 16 MHz Min—60 MHz Max Frequency	—	—	—	ns
t_{WS}	ADDR, RWN, DATA (write) Valid to MPCLK	3.5	0	—	ns
t_{APD}	MPCLK to ADDR, RWN, DATA, CSN (write) Invalid	—	5	—	ns
t_{CSNVS}	CSN Valid to MPCLK	3.5	0	—	ns
t_{ADSNVS}	ADSN Valid to MPCLK	5.5	0	—	ns
t_{AIPD}	MPCLK to ADSN Invalid	—	5	—	ns
t_{DTNVPD}	MPCLK to DTN Valid	—	—	16	ns
t_{DTNIPD}	MPCLK to DTN Invalid	—	—	16	ns
$t_{ADSNVDTF}$	ADSN Valid to DTN Fall	—	—	1000	ns

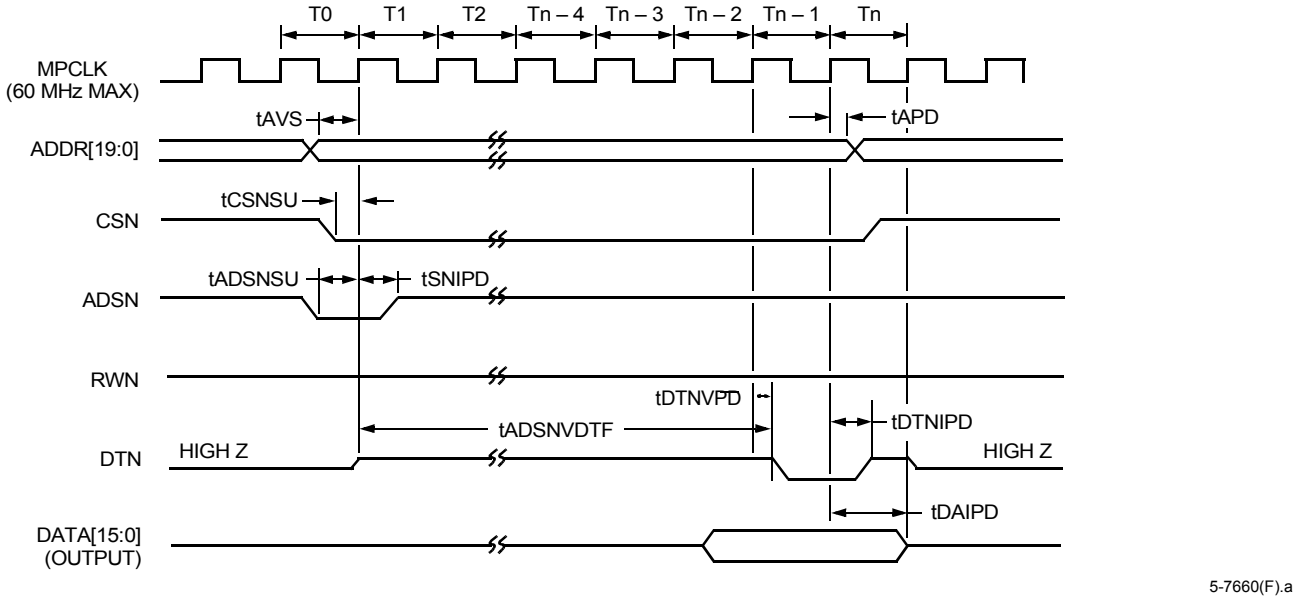


Figure 4-8. Microprocessor Interface Synchronous Read Cycle (MPMODE (Pin AD17) = 1)

MPCLK 16 MHz minimum to 60* MHz maximum frequency.

ADDR [19:0] The address will be available throughout the entire cycle, and must be stable before ADSN turns high.

DATA [15:0] Read data is stable in Tn – 1.

RWN (Input) The read (H) write (L) signal is always high during the read cycle.

CSN (Input) Chip select is an active-low signal.

DTN (Output) Data transfer acknowledge on the host bus interface is initiated on T6. This signal is active for one clock and then driven high before entering a high-impedance state. (This is done with an I/O pad using the input as feedback to qualify the 3-state term.) Fall will become 3-stated when CS is high. Typically, DTN is active 4 or 5 MPCLK cycles after ADSN is low.

ADSN (Input) Address strobe is active-low. ADSN must be one MPCLK clock period wide.

* If DTN is used, then the maximum frequency for MPCLK is determined by the processor's setup specification for DTN. For example, a 9 ns setup time would limit MPCLK to 40 MHz for reliable DTN detection.

Table 4-40. Microprocessor Interface Synchronous Read Cycle Specifications

Symbol	Parameter	Setup (Min)	Hold (Min)	Delay (Min)	Delay (Max)	Unit
T_{CLK}	MPCLK 16 MHz Min—60 MHz Max Frequency	—	—	—	—	ns
t_{AVS}	ADDR Valid to MPCLK	3.5	0	—	—	ns
t_{APD}	MPCLK to ADDR Invalid	—	5	—	—	ns
t_{CSNSU}	CSN Active to MPCLK	3.5	0	—	—	ns
t_{ADSNSU}	ADSN Valid to MPCLK	5.5	0	—	—	ns
t_{SNIPD}	MPCLK to ADSN Inactive	—	5	—	—	ns
t_{DVPD}	MPCLK to DTN Valid	—	—	4	16	ns
t_{DIPD}	MPCLK to DTN Invalid	—	—	4	16	ns
t_{DAIPD}	MPCLK to DATA 3-state	—	—	—	10	ns
$t_{ADSNVDTF}$	ADSN Valid to DTN Fall	—	—	—	1000	ns

4.18.2 Asynchronous Mode

The asynchronous microprocessor interface mode is selected when MPMODE (pin AC18) = 0. Interface timing for the asynchronous mode write cycle is given in Figure 4-9 and in Table 4-41, and for the read cycle in Figure 4-10 and in Table 4-42.

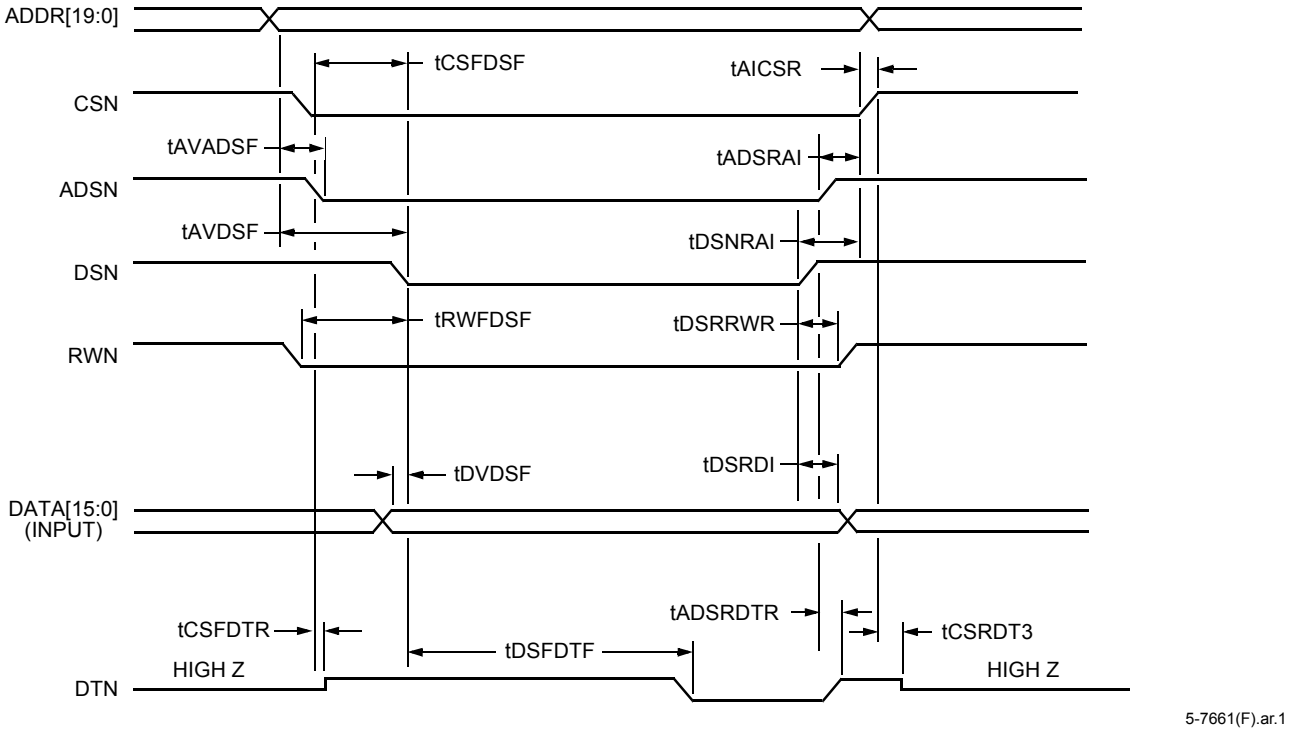


Figure 4-9. Microprocessor Interface Asynchronous Write Cycle Description (MPMODE (Pin AC18) = 0)

ADDR [19:0] Address is asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle.

DATA [15:0] Write data is asynchronously passed from the host bus to the internal bus. Data will be available throughout the entire cycle.

RWN (Input) The read (H) write (L) signal is always high except during a write cycle.

CSN (Input) Chip select is an active-low signal.

DTN (Output) Data transfer acknowledge (active-low). DTN is driven asynchronously based on the arrival of CSN. DTN is driven high until the internal transaction is done. DTN is driven high again when either ADSN or DSN is deasserted. DTN will become 3-stated when CSN is high.

ADSN (Input) Address strobe is active-low. ADSN must be a minimum of one MPCLK clock period wide.

DSN (Input) Data strobe is active-low.

Table 4-41. Microprocessor Interface Asynchronous Write Cycle Specifications

Symbol	Parameter	Typical Interval	Max Interval	Unit
t_{CSFDSF}	CSN Fall to DSN Fall	0	—	ns
t_{AICSR}	ADDR Invalid to CSN Rise	0	—	ns
t_{AVADSF}	ADDR Valid to ADSN Fall	0	—	ns
t_{ADSRAI}	ADSN Rise to ADDR Invalid	0	—	ns
t_{AVDSF}	ADDR Valid to DSN Fall	0	—	ns
t_{DSNRAI}	DSN Rise to ADDR Invalid	0	—	ns
t_{RWFDSF}	RWN Fall to DSN Fall	0	—	ns
t_{DSRRWR}	DSN Rise to RWN Rise	0	—	ns
t_{DVDSF}	DATA Valid to DSN Fall	0	—	ns
t_{DSRDI}	DSN Rise to DATA Invalid	0	—	ns
t_{CSFDTR}	CSN Fall to DTN Rise	20	—	ns
t_{DSFDTF}	DSN Fall to DTN Fall	120	1000	ns
$t_{ADSRDTR}$	ADSN Rise to DTN Rise	20	—	ns
t_{CSRDT3}	CSN Rise to DTN 3-state	10	—	ns

Note: Specifications are valid for 50 MHz MPCLK with MPMODE = 0. Address strobe (ADSN) and chip select (CSN) may be connected and driven from the same source. In this configuration, the setup and hold times for ADSN must be satisfied.

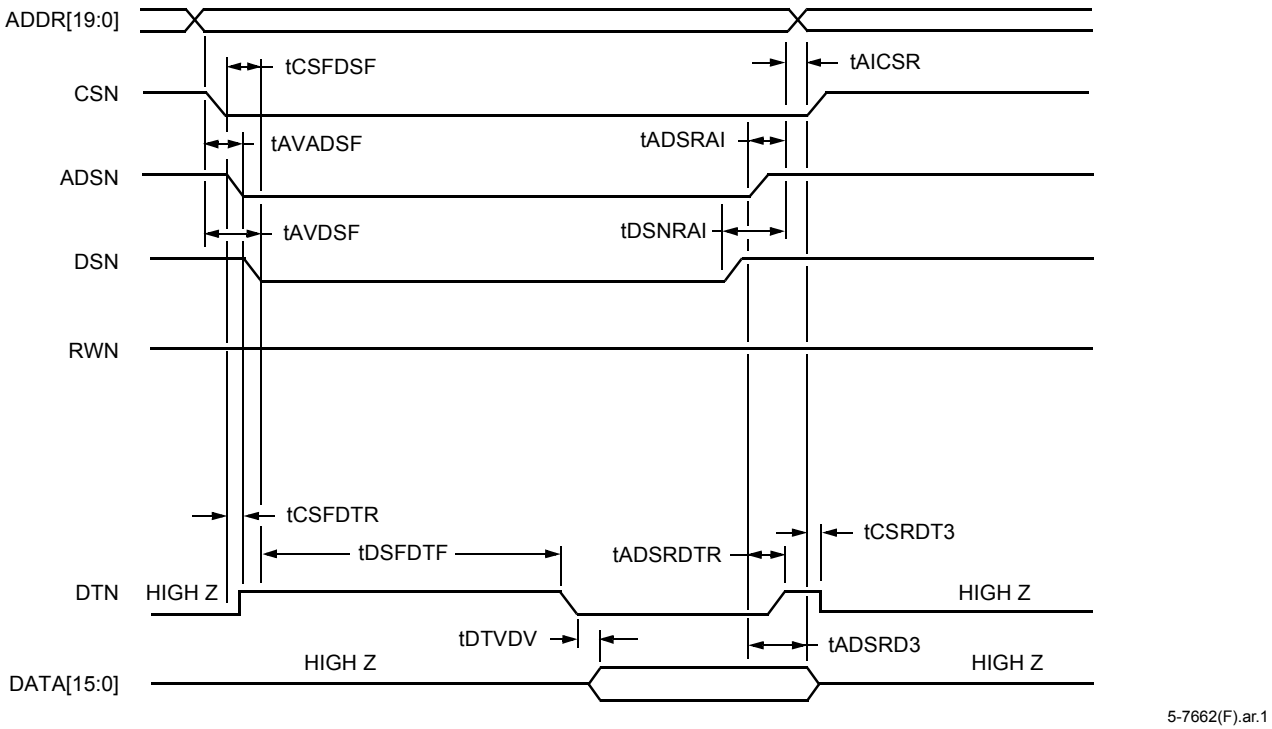


Figure 4-10. Microprocessor Interface Asynchronous Read Cycle (MPMODE (Pin AC18) = 0)

ADDR [19:0] Address is asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle.

DATA [15:0] Read data on the internal bus is only valid for one clock cycle; therefore, a latch is necessary to meet the correct timing on the host bus.

RWN (Input) The read (H) write (L) signal is always high during a read cycle.

CSN (Input) Chip select is an active-low signal.

DTN (Output) Data transfer acknowledge (active-low). DTN is driven asynchronously based on the arrival of CSN, DSN, and ADSN. DTN is driven high while the internal bus transaction is in progress. There is no need to provide synchronization to outgoing signals in this mode. DTN is driven high and then placed in a high-impedance state when either ADSN or DSN is deasserted. DTN will become 3-stated when CSN is high.

ADSN (Input) Address strobe is active-low.

DSN (Input) Data strobe is active-low.

Table 4-42. Microprocessor Interface Asynchronous Read Cycle Specifications

Symbol	Parameter	Typical Interval	Max Interval	Unit
t_{CSFDSF}	CSN Fall to DSN Fall	0[1]	—	ns
t_{AICSR}	ADDR Invalid to CSN Rise	0	—	ns
t_{AVADSF}	ADDR Valid to ADSN Fall	0	60[2]	ns
t_{ADSRAI}	ADSN Rise to ADDR Invalid	0	—	ns
t_{AVDSF}	ADDR Valid to DSN Fall	0	—	ns
t_{DSNRAI}	DSN Rise to ADDR Invalid	0	—	ns
t_{CSFDTR}	CSN Fall to DTN Rise	20	—	ns
t_{DSFDTF}	DSN Fall to DTN Fall	100	1000 [3, 4]	ns
$t_{ADSRDTR}$	ADSN Rise to DTN Rise	20[5]	—	ns
t_{CSRDT3}	CSN Rise to DTN 3-state	10	—	ns
t_{DTVDV}	DTN Valid to DATA Valid	0[6]	—	ns
t_{ADSRD3}	ADSN Rise to DATA 3-state	20	—	ns

1. DSN can be asserted up to 20 ns (1 clk at 50 MHz) previous to CSN.
2. ADDR can be asserted up to 60 ns (3 clk at 50 MHz) into cycle from ASDN.
3. DTN fall is variable depending on the block selected for access.
4. Leading edges of ADSN and DSN determine the Fall edge of DTN.
5. Rising edge of ADSN determines the rising edge of DTN.
6. Data toggle 20 ns (1 clk at 50 MHz) previous to CSN.

Note: Specifications are valid for 50 MHz MPCLK with MPMODE = 0. Address strobe (ADSN) and chip select (CSN) may be connected and driven from the same source. In this configuration, the setup and hold times for ADSN must be satisfied.

4.19 General-Purpose Interface Timing

Table 4-43. Input Timing Specifications

Input Name	Reference CLK	Min Setup Time (t_S)	Min Hold Time (t_H)	Unit
JTAG Signals				
TDI	TCLK ↑	15.0	2.0	ns
TMSN	TCLK ↑	15.0	2.0	ns
TRSTN	NA	ASYNC	ASYNC	—
SCAN_EN	NA	ASYNC	ASYNC	—
SCAN_MODE	NA	ASYNC	ASYNC	—
Miscellaneous Signals				
RSTN	NA	ASYNC	ASYNC	—
PMRST	NA	ASYNC	ASYNC	—
IC3STATEN	NA	ASYNC	ASYNC	—
IDDQ	NA	ASYNC	ASYNC	—

Table 4-44. Output Timing Specifications

Output Name	Reference CLK	Test Conditions	Propagation Delay* (t_{PD})		Unit
			Min	Max	
Transmit Signals					
TDO	TLCK ↓	C_L = 25 pF	3.0	20.0	ns
Miscellaneous Signals					
PMRST	NA	—	ASYNC	ASYNC	—

* Propagation delay skew, tPLH – tPHL, is ±200 ps.

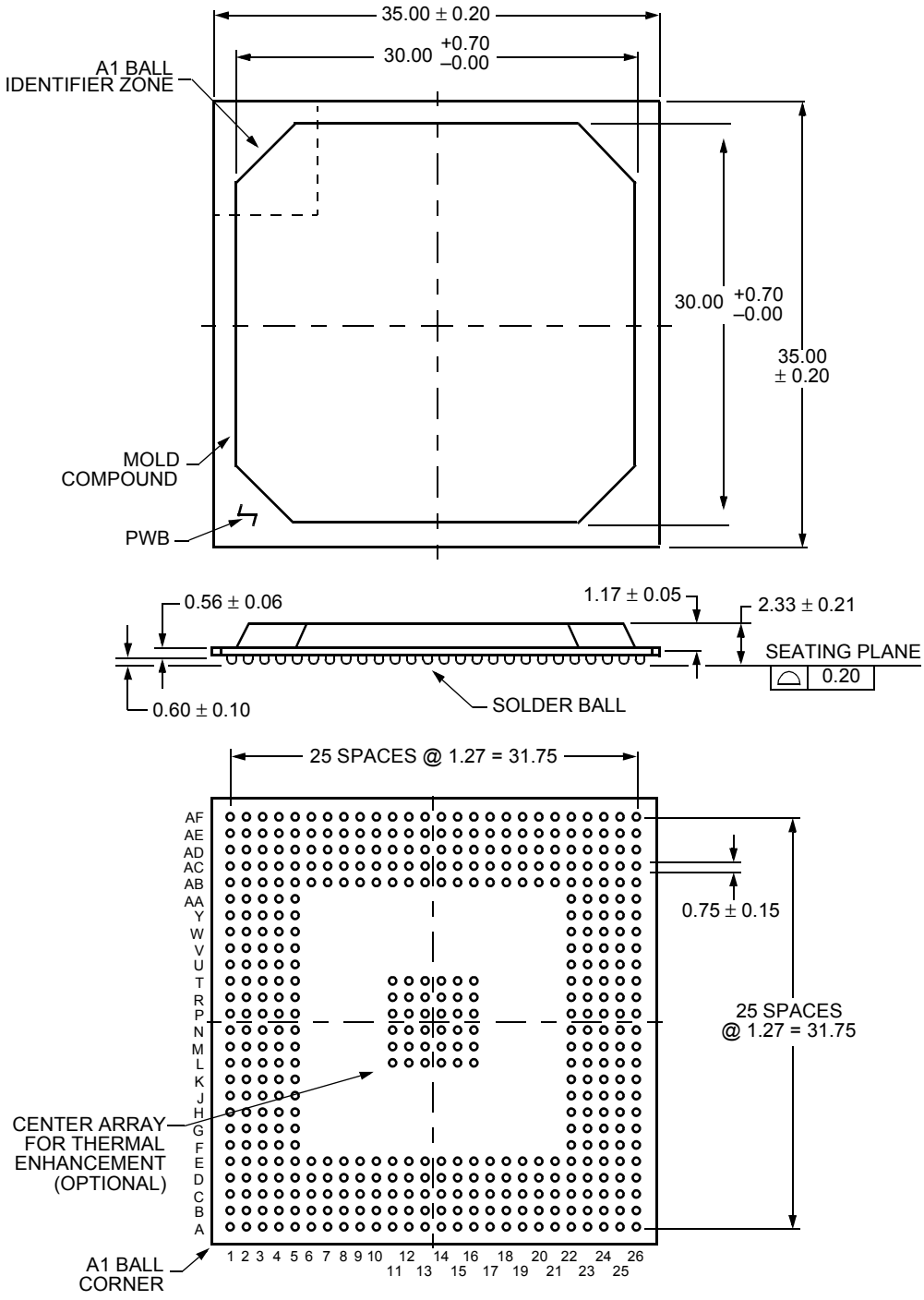
5 Ordering Information

Device Code	Package	Temperature	Comcode
TFRA28J133BAL-1-DB	456-pin PBGA	–40 °C to +85 °C	1090573560

6 Outline Diagram

6.1 456-Pin PBGA

Dimensions are in millimeters.



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