N-Channel JFET Low Noise Amplifier

calogic CORPORATION

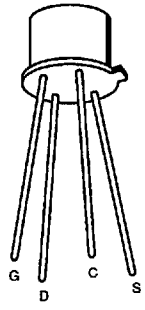
2N4867 – 2N4869 / 2N4867A – 2N4869A

T-27-25

FEATURES

- **Low Noise Voltage**
- **Low Leakage**
- **High Gain**

PIN CONFIGURATION



5005

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage ..... -40V
Gate Current 50mA
Storage Temperature Range ..... -65°C to +200°C
Operating Temperature Range ..... -55°C to +200°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 300mW
Derate above 25°C ..... 1.7mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
2N4867	Hermetic TO-72	-55°C to +200°C
2N4867A	Hermetic TO-72	-55°C to +200°C
X2N4867	Sorted Chips in Carriers	-55°C to +200°C
2N4868	Hermetic TO-72	-55°C to +200°C
2N4868A	Hermetic TO-72	-55°C to +200°C
X2N4868	Sorted Chips in Carriers	-55°C to +200°C
2N4869	Hermetic TO-72	-55°C to +200°C
2N4869A	Hermetic TO-72	-55°C to +200°C
X2N4869	Sorted Chips in Carriers	-55°C to +200°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER		2N4867 2N4867A MIN	2N4867 2N4867A MAX	2N4868 2N4868A MIN	2N4868 2N4868A MAX	2N4869 2N4869A MIN	2N4869 2N4869A MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current			-0.25		-0.25		-0.25	nA	V_{GS} = -30V, V_{DS} = 0	
				-0.25		-0.25		-0.25	µA		T_A = 150°C
BV_{GSS}	Gate-Source Breakdown Voltage		-40		-40		-40		V	I_G = -1µA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-0.7	-2	-1	-3	-1.8	-5		V_{DS} = 20V, I_D = 1µA	
I_{DSS}	Saturation Drain Current (Note 1)		0.4	1.2	1	3	2.5	7.5	mA	V_{DS} = 20V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)		700	2000	1000	3000	1300	4000	µs	V_{DS} = 20V, V_{GS} = 0	f = 1kHz
g_{os}	Common-Source Output Conductance			1.5		4		10			
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 2)			5		5		5	pF		f = 1MHz
C_{iss}	Common-Source Input Capacitance (Note 2)			25		25		25			
$\bar{e}_n$	Short Circuit Equivalent Input Noise Voltage (Note 2)			20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10V V_{GS} = 0	f = 10Hz
				10		10		10			f = 1kHz
		A devices		10		10		10			f = 10Hz
		A devices		5		5		5			f = 1kHz
NF	Spot Noise Figure (Note 2)			1		1		1	dB	V_{DS} = 10V, V_{GS} = 0 R_{gen} = 20K, (2N4867 Series) R_{gen} = 5K, (2N4867A Series)	f = 1kHz

NOTES: 1. Pulse test duration = 2ms.
2. For design reference only, not 100% tested.