Preliminary

Am79C02/A

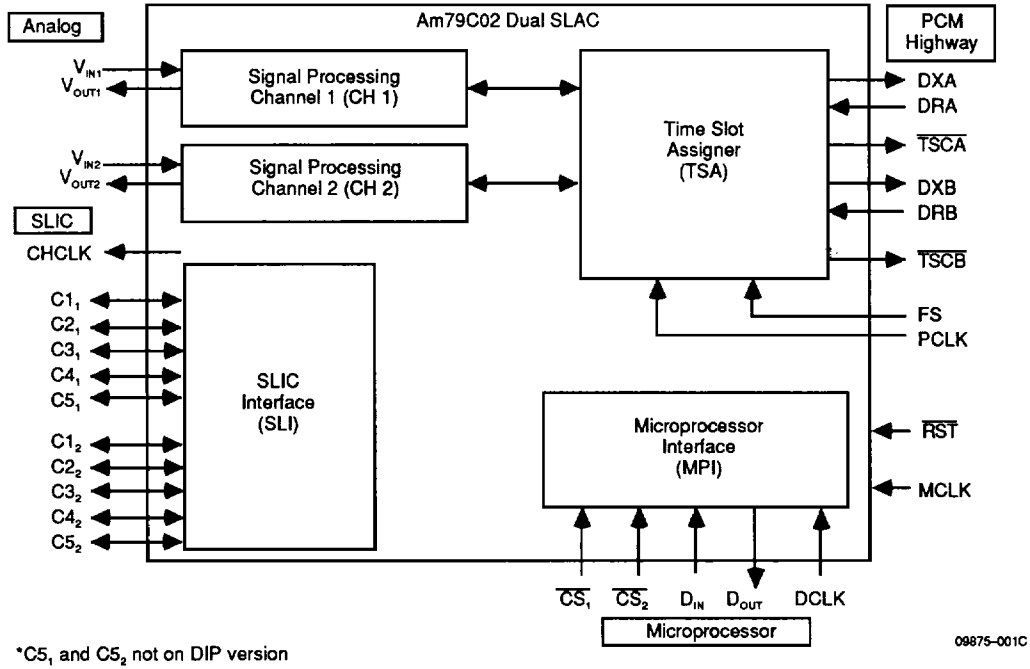
Dual Subscriber Line Audio-Processing Circuit (DSLAC™)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Software programmable:**
  - –SLIC impedance
  - –Trans-hybrid balance
  - –Transmit and Receive gains
  - –Equalization
  - –Digital I/O pins
  - –Time Slot Assigner
- **Adapt and freeze or fixed trans-hybrid balance filter (Am79C02 and Am79C02A)**
- **Continuously adapting trans-hybrid balance filter (Am79C02A only)**
- **A-law or μ-law coding**
- **Dual PCM ports**
  - –Up to 8.192 MHz (128 channels per port) through the PCM interface
- **2.048 MHz or 4.096 MHz master clock**
- **Direct Transformer Drive**
- **Built-in test modes**
- **Low power CMOS**
- **Mixed mode (analog and digital) impedance scaling**
- **Performance characteristics guaranteed over 12 dB gain range**

BLOCK DIAGRAM



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*$C5_1$ and $C5_2$ not on DIP version

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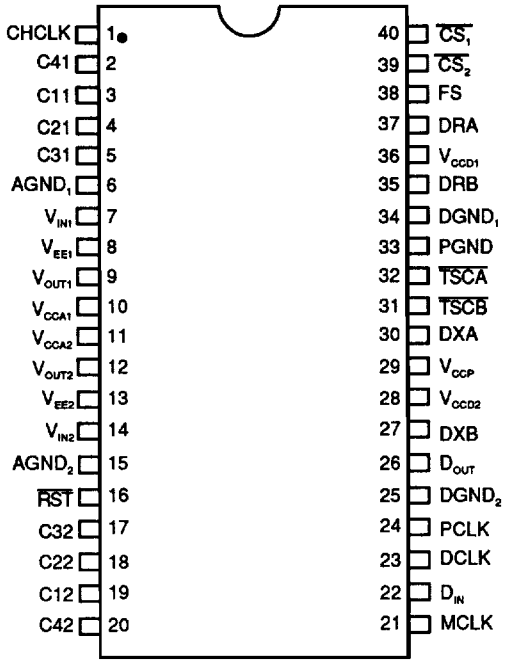
GENERAL DESCRIPTION

The Am79C02/A Dual Subscriber Line Audio-Processing Circuit (DSLAC) integrates the key functions of an analog linecard into one programmable, high-performance dual CODEC-filter device. The DSLAC is based on the proven design of the reliable Am7901A Subscriber Line Audio-Processing Circuit (SLAC™). The advanced architecture of the DSLAC implements two independent channels and employs digital filters to allow software control of transmission, thus providing a cost-effective solution for the four-wire-to-PCM section of a linecard.

Advanced CMOS technology makes the Am79C02/A DSLAC an economical device that has both the functionality and the low power consumption needed by linecard designers to maximize linecard density at minimum cost. When used with two SLICs, the DSLAC provides a complete, software-configurable solution to the BORSCHT function.

CONNECTION DIAGRAMS
Top View

40-Pin DIP



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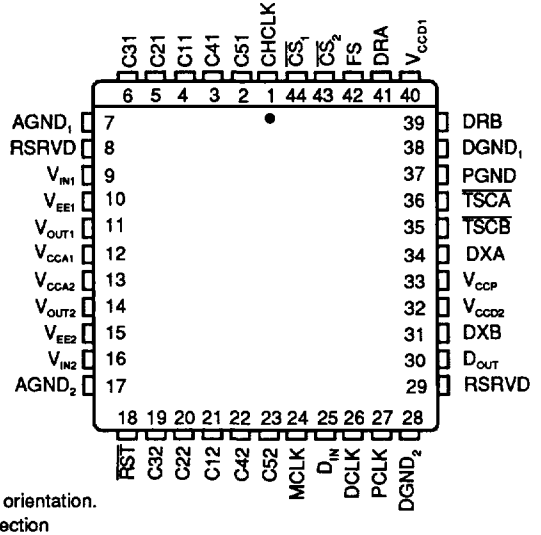
44-Pin PLCC



Notes: 1. Pin 1 is marked for orientation.
2. RSRVD = No connection

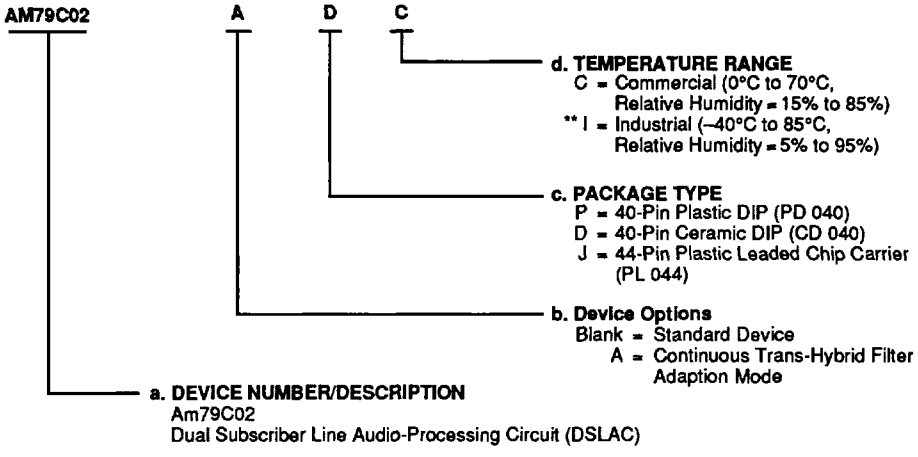
09875-003C

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range



Valid Combinations			
AM79C02	ADC	APC	AJC
	ADI	API	AJI
	DC	PC	JC
	DI	PI	JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

**The performance specifications contained in this Data Sheet are valid for the commercial temperature range device only. The specifications for the industrial temperature range device will be released after full characterization.

PIN DESCRIPTION

C11–C51, C12–C52
SLIC Input/Outputs (Input/Output)

The five SLIC control lines per channel are TTL compatible and bidirectional. They can be used to monitor or control the operation of a SLIC or any other device associated with the subscriber line. Lines C11–C51 are associated with Channel 1, and lines C12–C52 are associated with Channel 2. The C51 and C52 lines are only available on the 44-pin PLCC version of the DSLAC.

CHCLK
SLIC Clock (Output)

This output provides a 256-kHz, 50-duty cycle, TTL-compatible clock for use by two SLICs. The CHCLK frequency is synchronous to MCLK but the phase relationship to MCLK is random. CHCLK is capable of driving two TTL inputs.

$\overline{CS_1}$, $\overline{CS_2}$
Chip Selects (Input, Active LOW)

The Chip Select inputs enable the device to read or write control data. $\overline{CS_1}$ is for the Channel 1 microprocessor interface, and $\overline{CS_2}$ is for the Channel 2 microprocessor interface.

DCLK
Data Clock (Input)

The Data Clock input shifts data either into or out of the Microprocessor Interface of the DSLAC. The maximum clock rate is 4.096 MHz.

D_{IN}
Data Input (Input)

Control data is serially written into the DSLAC via the D_{IN} pin with the most significant bit first. The Data Clock determines the data rate. D_{IN} and D_{OUT} may be strapped together to reduce the number of connections to the microprocessor.

D_{OUT}
Data Output (Output)

Control data is serially read out of the DSLAC via the D_{OUT} pin with the most significant bit first. The Data Clock determines the data rate. D_{OUT} is high impedance except when data is being transmitted from the DSLAC under control of $\overline{CS_1}$ or $\overline{CS_2}$. D_{IN} and D_{OUT} may be strapped together to reduce the number of connections to the microprocessor.

DRA, DRB
PCM Inputs (Input)

The Receive PCM data for Channels 1 and 2 is serially received on either the DRA or the DRB port with port selection under user program control. Eight bits are received with the most significant bit first. Data for each channel is received in 8-bit bursts every 125 µs at the PCLK rate.

DXA, DXB
PCM Outputs (Output)

The Transmit PCM data from Channels 1 and 2 is sent serially through either the DXA or DXB port with port selection under user program control. Eight bits are transmitted with the most significant bit first. The output is available every 125 µs and the data is shifted out in 8-bit bursts at the PCLK rate. DXA and DXB are high impedance between bursts and while the device is in the Inactive mode.

FS
Frame Sync (Input)

The Frame Sync pulse is an 8-kHz signal that identifies the beginning of a frame. The DSLAC references individual time slots with respect to this input, which must be synchronized to PCLK.

MCLK
Master Clock (Input)

The Master Clock must be a 2.048-MHz or 4.096-MHz clock input for use by the digital signal processor. MCLK may be asynchronous to PCLK.

PCLK
PCM Clock (Input)

The PCM clock determines the rate at which PCM data is serially shifted into or out of the PCM ports. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 128 kHz. The PCLK clock may be asynchronous to MCLK.

$\overline{RST}$
Reset (Input, Active LOW)

A TTL LOW signal on this input resets the DSLAC to its default state.

$\overline{TSCA}$, $\overline{TSCB}$
Time Slot Control (Output, Open Drain, Active LOW)

The Time Slot Control outputs are open drain (requiring *pull-up resistors) and are normally inactive (high impedance).* $\overline{TSCA}$ is active (LOW) when PCM data is present on the DXA output and $\overline{TSCB}$ is active (LOW) when PCM data is present on the DXB output.

V_{IN1}, V_{IN2}
Analog Inputs (Input)

The analog input is applied to the transmit path of the DSLAC. The signal is sampled, digitally processed and encoded for the PCM output. V_{IN1} is the input for Channel 1 *and* V_{IN2} *is the input for Channel 2.*

V_{OUT1}, V_{OUT2}
Analog Outputs (Output)

The received PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin. V_{OUT1} is the output from Channel 1 and V_{OUT2} is the output for Channel 2. These outputs can directly drive a transformer SLIC.

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$AGND_1$	Analog Ground—Channel 1
$AGND_2$	Analog Ground—Channel 2
$DGND_1$	Digital Ground 1
$DGND_2$	Digital Ground 2
PGND	PCM I/O Ground
V_{CCA1}	+5 V Analog Power Supply—Channel 1
V_{CCA2}	+5 V Analog Power Supply—Channel 2
V_{CCD1}	+5 V Digital Power Supply. Internally connected to substrate on the IC
V_{CCD2}	+5 V Digital Power Supply. Internally connected to substrate on the IC
V_{CCP}	+5 V PCM I/O Power Supply. Internally connected to substrate on the IC
V_{EE1}	–5 V Power Supply—Channel 1
V_{EE2}	–5 V Power Supply—Channel 2

The many separate power supply inputs are intended to provide for good power supply decoupling techniques. Note that all of the +5 volt inputs should be connected to the same source, all of the ground inputs should be connected to the same source, and both of the –5 volt inputs should be connected to the same source.

FUNCTIONAL DESCRIPTION

The DSLAC performs the CODEC and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the trans-hybrid balancing function, permit adjustment of the two-wire termination impedance, and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive trans-hybrid balancing is also included. All programmable digital filter coefficients can be calculated using the AmSLAC-II software. The PCM codes can be either 8-bit companded A-law or μ-law. The PCM data is read or written to the PCM highway in user-programmable time slots at rates of 128 kHz to 8.192 MHz. The output hold time can be adjusted for compatibility with other devices which can be connected to the PCM highway.

The independent channels allow the DSLAC to function as two SLACs. All of the digital filtering is performed in digital signal processors operating from either a 2.048-MHz or 4.096-MHz external clock. The A/D, D/A, and signal processing is separate for each channel and each channel has its own chip select ($\overline{CS_1}$ and $\overline{CS_2}$) to allow separate programming. The dual channel DSLAC is available in a 40-pin DIP or a 44-pin PLCC, with the PLCC version having one extra SLIC I/O line per channel.

The following documentation describes the operation of a single channel of the DSLAC. The description is valid for either Channels 1 or 2. V_{IN} in this data sheet refers to either V_{IN1} or V_{IN2}, V_{OUT} refers to either V_{OUT1} or V_{OUT2}, and $\overline{CS}$ refers to either $\overline{CS_1}$ or $\overline{CS_2}$.

Operational Modes

Active Mode

Each channel of the DSLAC can operate in either the active (operational) or inactive (standby) mode. In the active mode, the DSLAC is able to transmit and receive PCM and analog information. This is the normal operating mode when a telephone call is in progress. The Activate command, Microprocessor Interface (MPI) Command #5, puts the device into this state. Bringing the DSLAC into the active mode is only possible through the MPI.

Inactive Mode

The DSLAC is forced into the inactive (standby) mode by a hardware or software reset, or is programmed into this mode by the Inactivate command (Command #1). No transmission or reception of PCM data takes place, but the circuits which contain programmed information retain their data. Power is switched off from all non-essential circuitry, though the MPI remains active to receive new commands. The analog output is tied to ground through approximately 3 kohm resistors. Upon initial application of power, the DSLAC is forced into the inactive mode.

Reset State

An active LOW, hardware Reset pin ($\overline{RST}$) is available on the DSLAC which resets the device to the following default state:

1. A-law is selected.
2. B, X, R and Z filters are disabled and AISN gain is zero.
3. Transmit (GX & AX) and receive (GR & AR) gains are set to unity.
4. SLIC input/output direction is set to the input mode.
5. Normal conditions are selected (see Command #4).
6. The B-filter adaptive mode is turned off.
7. Both channels are placed in the Inactive (standby) mode.
8. Transmit and receive time and clock slots are set to zero.
9. DXA/DRA ports are selected for Channel 1.
10. DXB/DRB ports are selected for Channel 2.
11. MCLK is selected to be 4.096 MHz.

Reset states 1 to 7 are identical to those of the software reset (Command #2), but the hardware reset applies to both channels simultaneously. When power is initially applied to the DSLAC or when $\overline{RST}$ is asserted, the following sequence of actions is necessary to ensure correct operation of the DSLAC:

1. Select MCLK frequency (Command # 6).
2. Software reset (Command # 2).
3. Program filter coefficients and all other required parameters.

Upon initial application of power, a minimum of 1 msec is needed before $\overline{CS_1}$ or $\overline{CS_2}$ may go LOW and an MPI command initiated. If the power supply (V_{CCD1} or V_{CCD2}) falls below approximately 2.0 volts, the device is software-reset and will require complete reprogramming with the above sequence. Bit 7 of the SLIC Direction Register will read back as a logical 1 to indicate that a power interruption has been detected. This bit is cleared when a software reset command is sent to the DSLAC. The $\overline{RST}$ pin may be tied to +5 volts if it is not needed in the system.

Signal Processing

Overview of Digital Filters

Several of the blocks in the signal processing section are user programmable. These allow the user to optimize the performance of the DSLAC for the system. Figure 1 shows DSLAC signal processing and indicates the blocks that can be programmed.

The advantages of digital filters are:
–High reliability
–No drift with time or temperature
–Unit-to-unit repeatability
–Superior transmission performance

Two-Wire Impedance Matching

Two feedback paths on the DSLAC modify the effective two-wire input impedance of the SLIC by providing programmable feedback from V_{IN} to V_{OUT}. The Analog Impedance Scaling Network (AISN) is a programmable analog gain of –0.9375 to +0.9375 from V_{IN} to V_{OUT}. The Z filter is a programmable digital filter, also connecting V_{IN} to V_{OUT}.

Distortion Correction and Equalization

The DSLAC contains programmable filters in the receive (R) and transmit (X) directions that may be programmed for line equalization and to correct any attenuation distortion caused by the Z filter.

Trans-Hybrid Balancing

The DSLAC programmable B filter provides trans-hybrid balance. The filter has a single-pole IIR section (B-IIR) and an eight-tap FIR section (B-FIR), both operating at 16 kHz. The DSLAC has an optional adaptive mode for the B filter which may be used to achieve optimum performance. The Echo Path Gain (EPG) and Error Level Threshold (ELT) registers contain values which determine the adaptive mode performance.

Gain Adjustment

The DSLAC transmit path has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB, located immediately before the A/D converter. Gain block GX is a digital gain that is programmable from 0 dB to 12 dB with a minimum step size of .1 dB if the gain setting is below +10 dB, and a minimum step size of .3 dB for gain settings above +10 dB (0 dBm0 is defined as 1.55 VRMS at V_{IN}). The filters provide a net gain in the range of 0 dB to 18 dB.

The DSLAC receive path has two programmable loss blocks. Loss block GR is a digital loss that is programmable from 0 dB to 12 dB with a worst case step size of 0.1 dB (0 dBm0 is defined as 1.55 VRMS at V_{OUT}). Loss block AR is an analog loss of 0 dB or 6.02 dB, located immediately after the D/A converter. This provides a net loss in the range of 0 dB to 18 dB.

Transmit Signal Processing

In the transmit path, the analog input signal is A/D converted, filtered, companded (A- or μ-law), and made available for output to the PCM highway. The signal processor contains an ALU, RAM, ROM, and control logic to implement the filter sections. The B, X, and GX blocks are user-programmable digital filter sections with coefficients stored in the coefficient RAM while AX is an analog amplifier which can be programmed for 0 dB or 6.02 dB gain. The filters may be made transparent when not required in a system.

The decimator reduces the high input sampling rate to 16 kHz for input to the B, GX, and X filters. The X filter is a 6-tap FIR section which is part of the frequency response correction network. The B filter operates on samples from the receive signal path in order to provide trans-hybrid balancing in the loop. The high-pass filter rejects low frequencies such as 50 or 60 Hz and may be disabled.

Transmit PCM Interface

The transmit PCM interface receives an 8-bit compressed code from the digital A/μ-law compressor. The transmit PCM interface logic (Figure 2) controls the transmission of the data onto the PCM highway through the output port selection circuitry and the time and clock slot control block.

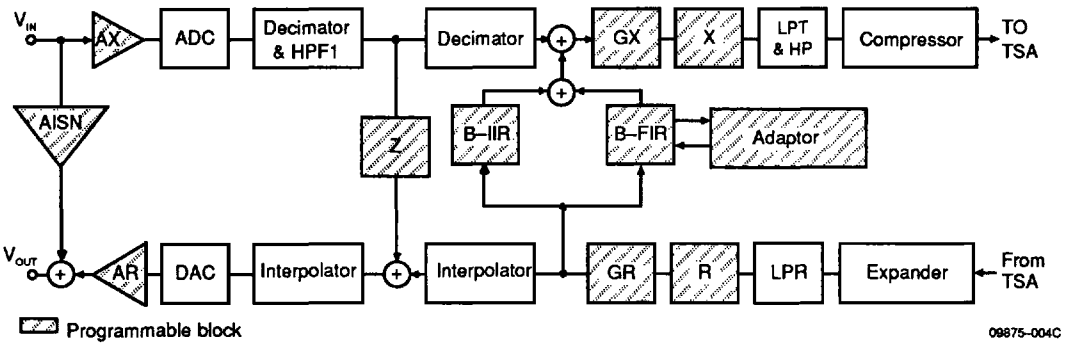

Figure 1. DSLAC Signal Processing

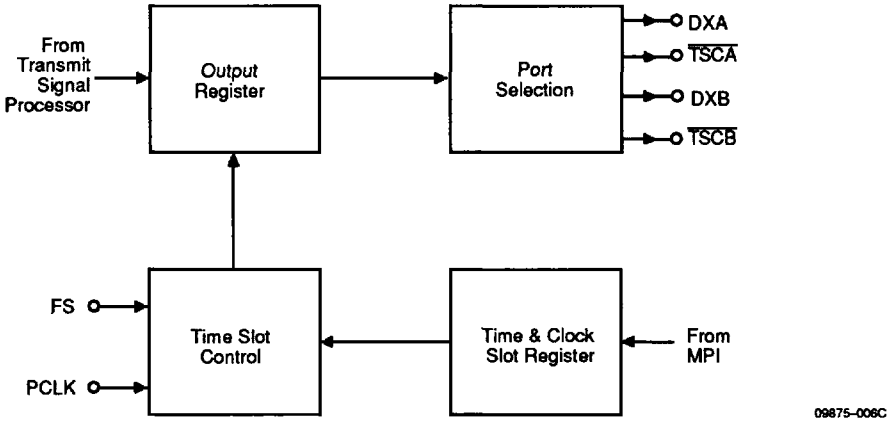

Figure 2. Transmit PCM Interface

The frame sync (FS) pulse identifies the beginning of a transmit frame and all channels (time slots) are referenced to it. The logic contains user-programmable Transmit Time Slot and Transmit Clock Slot registers.

The Time Slot register is 7 bits wide and allows up to 128 8-bit channels (using a PCLK of 8.192 MHz) in each frame. This feature allows any clock frequency between 128 kHz and 8.192 MHz (2 to 128 channels) in a system. The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 PCLK periods to eliminate any clock skew in the system. The data is transmitted in bytes with the most significant bit first.

The PCM data may be user-programmed for output onto either the DXA or DXB port. Correspondingly, either $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$ is LOW during transmission. An extra delay (PCM delay) in the timing of the DXA and DXB signals may be programmed to allow timing compatibility with other devices on the PCM highway.

Receive Signal Processing

In the receive path, the digital signal is expanded, filtered, converted to analog, and passed to the V_{OUT} pin. The signal processor contains an ALU, RAM, ROM, and Control logic to implement the filter sections. The Z, R, and GR blocks are user-programmable filter sections with their coefficients stored in the coefficient RAM while AR is an analog amplifier which can be programmed for a 0-dB or 6.02-dB loss. The filters may be made transparent when not required in a system.

The low-pass filter band limits the signal. The R filter is a 6-tap FIR section operating at a 16-kHz sampling rate and is part of the frequency response correction network. The analog impedance scaling network (AISN) is a user-programmable gain block providing feedback from V_{IN} to V_{OUT} to emulate different ZSLIC impedances from a single external ZSLIC impedance. The Z filter provides feedback from the transmit signal path to the receive path and is used to modify the effective input impedance to the system. The interpolator increases the sampling rate prior to D/A conversion.

Receive PCM Interface

The receive PCM interface logic (Figure 3) controls the reception of data bytes from the PCM highway, transfers the data to the A/μ-law expansion logic, and then passes the data to the receive path of the signal processor. The frame sync (FS) pulse identifies the beginning of a receive frame, and all channels (time slots) are referenced to it.

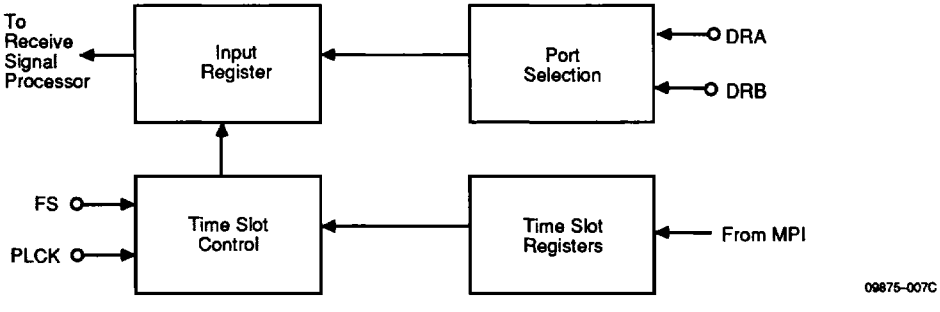

Figure 3. Receive PCM Interface

The logic contains user-programmable Receive Time Slot and Receive Clock Slot registers. The Time Slot register is 7 bits wide and allows up to 128 8-bit channels (using a PCLK of 8.192 MHz) in each frame. This feature allows any clock frequency between 128 kHz and 8.192 MHz (2 to 128 channels) in a system. The Clock Slot register is 3 bits wide and may be programmed to offset the time slot assignment by 0 to 7 PCLK periods to eliminate any clock skews in the system. The PCM data may be user-programmed for input from either the DRA or DRB port.

Analog Impedance Scaling Network (AISN)

The AISN is incorporated in the DSLAC to scale the value of the external Z_{SLIC} impedance. Scaling this external impedance with the AISN (along with the Z filter) allows matching of many different line conditions using a single impedance value. Line cards may be designed for many different specifications without any hardware changes.

The AISN is a programmable gain that is connected across the DSLAC input from V_{IN} to V_{OUT}. The gain can be varied from –0.9375 to +0.9375 in 31 steps of 0.0625. The AISN gain is given by the following equation:

$$h_{AISN} = 0.0625\,[(A \bullet 2^4 + B \bullet 2^3 + C \bullet 2^2 + D \bullet 2^1 + E \bullet 2^0) - 16]$$

where A, B, C, D, and E = 1 or 0.

The AISN gain is used to determine the input impedance of the DSLAC when terminated by Z_{SLIC} as shown in Figure 4.

The DSLAC input impedance is approximately given by:

$$Z_{IN} = \frac{1 - G_{44}\, h_{AISN}}{1 - G_{440}\, h_{AISN}} Z_{SL},$$

where G_{440} (defined as $G_{24} G_{42} + G_{44}$) is the echo gain into an open circuit and G_{44} is the echo gain into a short circuit.

There are two special cases to the formula for h_{AISN}. A value of ABCDE = "00000" will specify a gain of 0 (or cut-off), and a value of ABCDE = "10000" is a special case where the AISN circuitry is disabled and the V_{OUT} pad is connected internally to V_{IN} with a gain of 0 dB. This allows a digital-to-digital loopback mode wherein a digital PCM input signal is completely processed through the receive section all the way to the V_{OUT} pin, then connected internally to V_{IN} where it is processed through the transmit section and output as digital PCM data.

Speech Coding

The A/D and D/A conversion follows either the A-law or the μ-law as they are defined in CCITT rec. G.711. A- or μ-law operation is programmed using MPI Command #19. Alternate bit inversion is performed as part of the A-law coding.

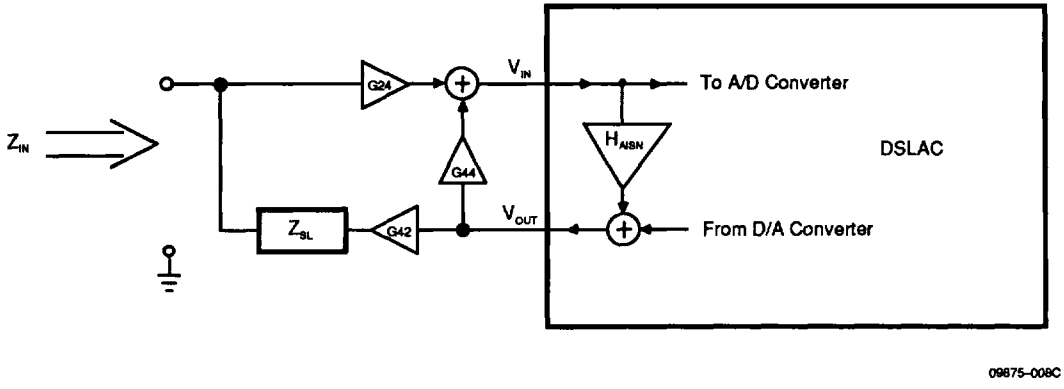

Figure 4. Input Impedance Modification Due to AISN

Command Description and Formats

Microprocessor Interface Description

A microprocessor may be used to program the DSLAC and control its operation using the Microprocessor Interface (MPI). Data programmed previously may be read out for verification. For each channel, commands are provided to assign values to the following parameters:

–Transmit time slot
–Receive time slot
–Transmit clock slot
–Receive clock slot
–Transmit gain
–Receive loss
–B-filter coefficients
–X-filter coefficients
–R-filter coefficients
–Z-filter coefficients
–Adaptive B filter parameters
–AISN coefficient
–Read/Write SLIC Input/Output
–Select A-law or μ-law code
–Select Transmit PCM Port A or B
–Select Receive PCM Port A or B
–Enable/disable B filter
–Enable/disable Z filter
–Enable/disable X filter
–Enable/disable R filter
–Enable/disable GX filter
–Enable/disable GR filter
–Enable/disable AX amplifier
–Enable/disable AR amplifier
–Enable/disable adaptive B filter
–Select test modes
–Select active or inactive (standby) mode

The following description of the MPI is valid for either Channel 1 or 2. Whenever $\overline{CS}$ is specified, it refers to either $\overline{CS_1}$ or $\overline{CS_2}$. If desired, both channels may be programmed simultaneously with identical information by activating $\overline{CS_1}$ and $\overline{CS_2}$ at the same time.

The MPI consists of serial data input (D_{IN}), output (D_{OUT}), data clock (DCLK), and a separate chip select (CS_1 and $\overline{CS_2}$) input for each channel (Figure 5). The serial input consists of 8-bit command words which may be followed with additional bytes of input data or may be followed by the DSLAC sending out bytes of data. All data input and output is MSB (D_7) first and LSB (D_0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going HIGH for at least the minimum off-period before the next byte is read or written.

All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All commands that are followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going LOW. The DSLAC will not accept any input commands until all the data has been shifted out. Unused bits in the data bytes are read out as zeros.

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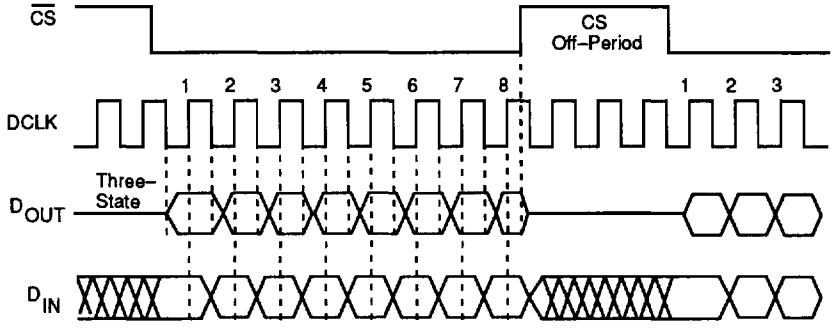

Figure 5. Microprocessor Interface Timing Diagram

An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the CS lines are held in the HIGH state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK may be run to a number of DSLACs and the individual $\overline{CS}$ lines will select the appropriate device to access. It should be noted that the DCLK can stay in the HIGH state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. DCLK can stay in the LOW state indefinitely with no loss of internal control information, provided the $\overline{CS}$ lines remain at a HIGH level.

Summary of MPI Commands**

C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Description
1.	00	0	0	0	0	0	0	0	0	Inactivate (standby mode)
2.	02	0	0	0	0	0	0	1	0	Reset
3.	06	0	0	0	0	0	1	1	0	No Operation
4.	08	0	0	0	0	1	0	0	0	Reset to Normal Conditions
5.	0E	0	0	0	0	1	1	1	0	Activate
6.	1*	0	0	0	1	0	0	*	0	MCLK Selection
7.	40	0	1	0	0	0	0	0	0	Write TX Time Slot & PCM Highway
8.	41	0	1	0	0	0	0	0	1	Read TX Time Slot & PCM Highway
9.	42	0	1	0	0	0	0	1	0	Write RX Time Slot & PCM Highway
10.	43	0	1	0	0	0	0	1	1	Read RX Time Slot & PCM Highway
11.	44	0	1	0	0	0	1	0	0	Write RX & TX Clock Slot Selection
12.	45	0	1	0	0	0	1	0	1	Read RX & TX Clock Slot Selection
13.	50	0	1	0	1	0	0	0	0	Write AISN, PCM delay, Analog gains
14.	51	0	1	0	1	0	0	0	1	Read AISN, PCM delay, Analog gains
15.	52	0	1	0	1	0	0	1	0	Write SLIC Input/Output register
16.	53	0	1	0	1	0	0	1	1	Read SLIC Input/Output register
17.	54	0	1	0	1	0	1	0	0	Write SLIC Input/Output direction
18.	55	0	1	0	1	0	1	0	1	Read SLIC I/O direction and Power Down bit
19.	60	0	1	1	0	0	0	0	0	Write Operating Functions
20.	61	0	1	1	0	0	0	0	1	Read Operating Functions
21.	70	0	1	1	1	0	0	0	0	Write Operating Conditions
22.	71	0	1	1	1	0	0	0	1	Read Operating Conditions
23.	73	0	1	1	1	0	0	1	1	Read Revision Code Number
24.	80	1	0	0	0	0	0	0	0	Write GX Filter Coefficients
25.	81	1	0	0	0	0	0	0	1	Read GX Filter Coefficients
26.	82	1	0	0	0	0	0	1	0	Write GR Filter Coefficients
27.	83	1	0	0	0	0	0	1	1	Read GR Filter Coefficients
28.	84	1	0	0	0	0	1	0	0	Write Z Filter Coefficients
29.	85	1	0	0	0	0	1	0	1	Read Z Filter Coefficients
30.	86	1	0	0	0	0	1	1	0	Write B Filter Coefficients
31.	87	1	0	0	0	0	1	1	1	Read B Filter Coefficients
32.	88	1	0	0	0	1	0	0	0	Write X Filter Coefficients
33.	89	1	0	0	0	1	0	0	1	Read X Filter Coefficients
34.	8A	1	0	0	0	1	0	1	0	Write R Filter Coefficients
35.	8B	1	0	0	0	1	0	1	1	Read R Filter Coefficients
36.	8C	1	0	0	0	1	1	0	0	Write Echo Path Gain
37.	8D	1	0	0	0	1	1	0	1	Read Echo Path Gain
38.	8E	1	0	0	0	1	1	1	0	Write Error Level Threshold
39.	8F	1	0	0	0	1	1	1	1	Read Error Level Threshold

*Code changes with function.
**All codes not listed are reserved by AMD and should not be used.

THE COMMAND STRUCTURE

This section describes in detail each of the MPI commands. Each of the commands is shown along with the format of any additional data bytes that follow. For details of the filter coefficients of the form $C_{xy}m_{bxy}$, please refer to the "Description of Coefficients" section.

1. **Inactivate** (standby mode)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

During the inactive mode (of one or both channels):
a) all of the programmed information is retained.
b) the Microprocessor Interface (MPI) remains active.
c) the PCM outputs are in high impedance and the PCM inputs are disabled.
d) the analog output is tied to zero volts through an internal resistor (~3 kohm).

2. **Reset**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	0

The reset state of the device is:
a) A-law is selected.
b) B, X, R, and Z filters are disabled and AISN gain is zero.
c) transmit (GX & AX) and Receive (GR & AR) gains are set to unity.
d) all SLIC I/O lines are configured as inputs.
e) normal conditions are selected (see Command #4).
f) the B-filter Adaptive mode is reset.
g) the channel is placed in the inactive (standby) mode.

3. **No Operation**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	1	0

4. **Reset to Normal Conditions**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0

Reset to Normal Conditions performs the following operations:
a) does not insert 6 dB loss in receive path.
b) receive & transmit paths are not cutoff.
c) high pass filter is enabled.
d) test modes are turned off.
e) PCM delay is inserted.

5. **Activate** (Operational Mode)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	1	0

This command places the device in the active mode. No valid PCM data is transmitted until after the second FS pulse is received following the execution of the Activate command.

6. MCLK Selection

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	A	0

MCLK may be selected to operate from a 2.048-MHz or 4.096-MHz external clock.
A = 0: 2.048 MHz
A = 1: 4.096 MHz

7. Write, Transmit Time Slot, & PCM Highway Selection

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	0	0	0	0	0
Output data:	PCM	TS	TS	TS	TS	TS	TS	TS

PCM = 0: Highway A TS: Time slot number 0 to 127
PCM = 1: Highway B

The Transmit section of both channels must not be set to the same time slot on the same output port simultaneously.

8. Read, Transmit Time Slot, & PCM Highway Selection

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	0	0	0	0	1
Output data:	PCM	TS	TS	TS	TS	TS	TS	TS

9. Write Receive Time Slot & PCM Highway Selection

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	0	0	0	1	0
Input data:	PCM	TS	TS	TS	TS	TS	TS	TS

PCM = 0: Highway A TS: Time slot number 0 to 127
PCM = 1: Highway B

10. Read, Receive Time Slot, & PCM Highway Selection

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	0	0	0	1	1
Output data:	PCM	TS	TS	TS	TS	TS	TS	TS

11. Write, Transmit, & Receive Clock Slot Selection

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	0	0	1	0	0
Input data:	—	—	RCS	RCS	RCS	TCS	TCS	TCS

TCS: Transmit Clock Slot number 0 to 7
RCS: Receive Clock Slot number 0 to 7

12. Read, Transmit, & Receive Clock Slot Selection

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	0	0	1	0	1
Output data:	—	—	RCS	RCS	RCS	TCS	TCS	TCS

13. Write AISN, PCM Delay, & Analog Gains

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	1	0	0	0	0
Input data:	PCD	AX	AR	A	B	C	D	E

PCM Delay: PCD = 0 Delay inserted (SLAC compatible)
PCD = 1 Delay removed (high speed)

Transmit Analog Gain: AX = 0 0 dB gain
AX = 1 6.02 dB gain

Receive Analog Loss: AR = 0 0 dB loss
AR = 1 6.02 dB loss

AISN coefficient: A, B, C, D, E

The Analog Impedance Scaling Network (AISN) gain can be varied from −0.9375 to 0.9375 in multiples of 0.0625. The gain coefficient is decoded using the following equation:

$$h_{AISN} = 0.0625\,[(A \bullet 2^4 + B \bullet 2^3 + C \bullet 2^2 + D \bullet 2^1 + E \bullet 2^0) - 16],$$

where h_{AISN} is the gain of the AISN and A, B, C, D, and E = 0 or 1. A value of ABCDE = "10000" implements a special digital loopback mode, and a value of ABCDE = "00000" indicates a gain of 0 (cutoff).

14. Read AISN, PCM Delay, & Analog Gains

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	1	0	0	0	1
Output data:	PCD	AX	AR	A	B	C	D	E

15. Write SLIC Input/Output Register

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	1	0	0	1	0
Input data:	—	—	—	C5	C4	C3	C2	C1

C1 through C5 are set to 1 or 0. The data will appear latched on the C1 through C5 SLIC I/O pins, provided they were set in the output mode (see Command #17). The data for any of the pins set to the input mode will be ignored.

16. Read SLIC Input/Output Register

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	1	0	0	1	1
Output data:	—	—	—	C5	C4	C3	C2	C1

The logic state of pins C1 through C5 is read regardless of the direction programmed into the Input/Output register.

17. Write SLIC Input/Output Direction

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	1	0	1	0	0
Input data:	—	—	—	A	B	C	D	E

Pins C1 through C5 are set to input or output modes individually. The input mode is set when the appropriate data bit is a 0, and the output mode is set when the data bit is a 1. All unused SLIC I/O pins should be programmed as outputs to reduce power consumption.

Data bit A sets pins C51 or C52.
Data bit B sets pins C41 or C42.
Data bit C sets pins C31 or C32.
Data bit D sets pins C21 or C22.
Data bit E sets pins C11 or C12.

18. Read SLIC Input/Output Direction and Power Interrupt Bit

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	0	1	0	1	0	1
Output data:	PI	—	—	A	B	C	D	E

PI = 0 There has not been a power interruption since the last software reset command.

PI = 1 A power interruption has been previously detected requiring the DSLAC to be completely reprogrammed. This bit is cleared by issuing a software reset command.

19. Write Operating Functions

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	1	0	0	0	0	0
Input data:	ABF	A/μ	EGR	EGX	EX	ER	EZ	EB

Adaptive B-Filter: ABF = 0 B filter non-adaptive mode
ABF = 1 B filter adaptive mode

A-law/μ-law: A/μ = 0 A-law coding
A/μ = 1 μ-law coding

GR Filter: EGR = 0 GR filter disabled
EGR = 1 GR filter enabled

GX Filter: EGX = 0 GX filter disabled
EGX = 1 GX filter enabled

X Filter: EX = 0 X filter disabled
EX = 1 X filter enabled

R Filter: ER = 0 R filter disabled
ER = 1 R filter enabled

Z Filter: EZ = 0 Z filter disabled
EZ = 1 Z filter enabled

B Filter: EB = 0 B filter disabled
EB = 1 B filter enabled

Note: The enable adaptive B-filter command is only effective when used with the enable B-filter command.

20. Read Operating Functions

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	1	0	0	0	0	1
Output data:	ABF	A/U	EGR	EGX	EX	ER	EZ	EB

21. Write Operating Conditions

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	1	1	0	0	0	0
Input data:	CTP	CRP	HPF	RG	ALB	TLB	—	—

Cut off Transmit Path:
CTP = 0 Transmit path connected
CTP = 1 Transmit path cut off

Cut off Receive Path:
CRP = 0 Receive path connected
CRP = 1 Receive path cut off

High-Pass Filter:
HPF = 0 High-pass filter enabled
HPF = 1 High-pass filter disabled

Receive Path Gain:
RG = 0 6 dB loss not inserted
RG = 1 6 dB loss inserted

Analog Loopback:
ALB = 0 Analog loopback disabled
ALB = 1 Analog loopback enabled

TSA Loopback:
TLB = 0 TSA loopback disabled
TLB = 1 TSA loopback enabled

22. Read Operating Conditions

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	1	1	0	0	0	1
Output data:	CTP	CRP	HPF	RG	ALB	TLB	—	—

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23. Read Revision Code Number

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	0	1	1	1	0	0	1	1
Output data:	#	#	#	#	#	#	#	#

This command returns an eight-bit number describing the revision number of the DSLAC.

24. Write GX Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	0	0	0	0
Input data byte 1:	C40		m40		C30		m30	
Input data byte 2:	C20		m20		C10		m10	

The coefficient for the GX filter is defined as:

$$H_{GX} = 1 + \left(C_{10} \bullet 2^{-m10}\{1 + C_{20} \bullet 2^{-m20}[1 + C_{30} \bullet 2^{-m30}(1 + C_{40} \bullet 2^{-m40})]\}\right).$$

25. Read GX Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	0	0	0	1
Output data byte 1:	C40		m40		C30		m30	
Output data byte 2:	C20		m20		C10		m10	

26. Write GR Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	0	0	1	0
Input data byte 1:	C40		m40		C30		m30	
Input data byte 2:	C20		m20		C10		m10	

The coefficient for the GR filter is defined as:

$$H_{GR} = C_{10} \bullet 2^{-m10}\{1 + C_{20} \bullet 2^{-m20}[1 + C_{30} \bullet 2^{-m30}(1 + C_{40} \bullet 2^{-m40})]\}.$$

27. Read GR Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	0	0	1	1
Output data byte 1:	C40		m40		C30		m30	
Output data byte 2:	C20		m20		C10		m10	

28. Write Z Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	0	1	0	0
Input data byte 1:	C26		m26		C16		m16	
Input data byte 2:	C27		m27		C17		m17	
Input data byte 3:	C40		m40		C30		m30	
Input data byte 4:	C20		m20		C10		m10	
Input data byte 5:	C41		m41		C31		m31	
Input data byte 6:	C21		m21		C11		m11	
Input data byte 7:	C42		m42		C32		m32	
Input data byte 8:	C22		m22		C12		m12	
Input data byte 9:	C43		m43		C33		m33	
Input data byte 10:	C23		m23		C13		m13	
Input data byte 11:	C44		m44		C34		m34	
Input data byte 12:	C24		m24		C14		m14	
Input data byte 13:	C45		m45		C35		m35	
Input data byte 14:	C25		m25		C15		m15	

The Z-transform equation for the Z filter is defined as:

$$H_Z(z) = Z_0 + Z_1z^{-1} + Z_2z^{-2} + Z_3z^{-3} + Z_4z^{-4} + Z_5z^{-5} + \frac{Z_6}{1 - Z_7z^{-1}.}$$

The coefficients for the FIR Z section are defined as:

$$Z_i = C_{1i} \bullet 2^{-m1i}\{1 + C_{2i} \bullet 2^{-m2i}[1 + C_{3i} \bullet 2^{-m3i}(1 + C_{4i} \bullet 2^{-m4i})]\}$$
for i = 1,2,3,4,5.

The coefficients for the IIR Z section are defined as:

$$Z_i = C_{1i} \bullet 2^{-m1i}(1 + C_{2i} \bullet 2^{-m2i})$$
for i = 6 or 7.

29. Read Z-Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	0	1	0	1
Output data byte 1:	C26		m26		C16		m16	
Output data byte 2:	C27		m27		C17		m17	
Output data byte 3:	C40		m40		C30		m30	
Output data byte 4:	C20		m20		C10		m10	
Output data byte 5:	C41		m41		C31		m31	
Output data byte 6:	C21		m21		C11		m11	
Output data byte 7:	C42		m42		C32		m32	
Output data byte 8:	C22		m22		C12		m12	
Output data byte 9:	C43		m43		C33		m33	
Output data byte 10:	C23		m23		C13		m13	
Output data byte 11:	C44		m44		C34		m34	
Output data byte 12:	C24		m24		C14		m14	
Output data byte 13:	C45		m45		C35		m35	
Output data byte 14:	C25		m25		C15		m15	

30. Write B-Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	0	1	1	0
Input data byte 1:	C30		m30		C20		m20	
Input data byte 2:	C10		m10		C31		m31	
Input data byte 3:	C21		m21		C11		m11	
Input data byte 4:	C32		m32		C22		m22	
Input data byte 5:	C12		m12		C33		m33	
Input data byte 6:	C23		m23		C13		m13	
Input data byte 7:	C34		m34		C24		m24	
Input data byte 8:	C14		m14		C35		m35	
Input data byte 9:	C25		m25		C15		m15	
Input data byte 10:	C36		m36		C26		m26	
Input data byte 11:	C16		m16		C37		m37	
Input data byte 12:	C27		m27		C17		m17	
Input data byte 13:	C48		m48		C38		m38	
Input data byte 14:	C28		m28		C18		m18	

The z = transform equation for the B filter is defined as:

$$H_B(z) = B_0 + B_1z^{-1} + B_2z^{-2} + B_3z^{-3} + B_4z^{-4} + B_5z^{-5} + B_6z^{-6} + \frac{B_7z^{-7}}{1 - B_8z^{-1}}.$$

The coefficients for the FIR B section and the gain of the IIR B section are defined as:

$$B_i = C_{1i} \bullet 2^{-m1i}[1 + C_{2i} \bullet 2^{-m2i}(1 + C_{3i} \bullet 2^{-m3i})].$$

The feedback coefficient of the IIR B section is defined as:

$$B_8 = C_{18} \bullet 2^{-m18}\ \{1 + C_{28} \bullet 2^{-m28}[1 + C_{38} \bullet 2^{-m38}(1 + C_{48} \bullet 2^{-m48})]\}.$$

31. Read B-Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	0	1	1	1
Output data byte 1:	C30		m30		C20		m20	
Output data byte 2:	C10		m10		C31		m31	
Output data byte 3:	C21		m21		C11		m11	
Output data byte 4:	C32		m32		C22		m22	
Output data byte 5:	C12		m12		C33		m33	
Output data byte 6:	C23		m23		C13		m13	
Output data byte 7:	C34		m34		C24		m24	
Output data byte 8:	C14		m14		C35		m35	
Output data byte 9:	C25		m25		C15		m15	
Output data byte 10:	C36		m36		C26		m26	
Output data byte 11:	C16		m16		C37		m37	
Output data byte 12:	C27		m27		C17		m17	
Output data byte 13:	C48		m48		C38		m38	
Output data byte 14:	C28		m28		C18		m18	

32. Write X-Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	1	0	0	0
Input data byte 1:	C40		m40		C30		m30	
Input data byte 2:	C20		m20		C10		m10	
Input data byte 3:	C41		m41		C31		m31	
Input data byte 4:	C21		m21		C11		m11	
Input data byte 5:	C42		m42		C32		m32	
Input data byte 6:	C22		m22		C12		m12	
Input data byte 7:	C43		m43		C33		m33	
Input data byte 8:	C23		m23		C13		m13	
Input data byte 9:	C44		m44		C34		m34	
Input data byte 10:	C24		m24		C14		m14	
Input data byte 11:	C45		m45		C35		m35	
Input data byte 12:	C25		m25		C15		m15	

The z-transform equation for the X filter is defined as:

$$H_X(z) = X_0 + X_1 z^{-1} + X_2 z^{-2} + X_3 z^{-3} + X_4 z^{-4} + X_5 z^{-5}.$$

The coefficients for the X filter are defined as:

$$X_i = C_{1i} \bullet 2^{-m1i}\{1 + C_{2i} \bullet 2^{-m2i}[1 + C_{3i} \bullet 2^{-m3i}(1 + C_{4i} \bullet 2^{-m4i})]\}.$$

33. Read X-Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	1	0	0	1
Output data byte 1:	C40		m40		C30		m30	
Output data byte 2:	C20		m20		C10		m10	
Output data byte 3:	C41		m41		C31		m31	
Output data byte 4:	C21		m21		C11		m11	
Output data byte 5:	C42		m42		C32		m32	
Output data byte 6:	C22		m22		C12		m12	
Output data byte 7:	C43		m43		C33		m33	
Output data byte 8:	C23		m23		C13		m13	
Output data byte 9:	C44		m44		C34		m34	
Output data byte 10:	C24		m24		C14		m14	
Output data byte 11:	C45		m45		C35		m35	
Output data byte 12:	C25		m25		C15		m15	

34. Write R-Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	1	0	1	0
Input data byte 1:	C40		m40		C30		m30	
Input data byte 2:	C20		m20		C10		m10	
Input data byte 3:	C41		m41		C31		m31	
Input data byte 4:	C21		m21		C11		m11	
Input data byte 5:	C42		m42		C32		m32	
Input data byte 6:	C22		m22		C12		m12	
Input data byte 7:	C43		m43		C33		m33	
Input data byte 8:	C23		m23		C13		m13	
Input data byte 9:	C44		m44		C34		m34	
Input data byte 10:	C24		m24		C14		m14	
Input data byte 11:	C45		m45		C35		m35	
Input data byte 12:	C25		m25		C15		m15	

The z-transform equation for the R filter is defined as:

$$H_R(z) = R_0 + R_1z^{-1} + R_2z^{-2} + R_3z^{-3} + R_4z^{-4} + R_5z^{-5}.$$

The coefficients for the R filter are defined as:

$$R_i = C_{1i} \bullet 2^{-m1i}\{1 + C_{2i} \bullet 2^{-m2i}[1 + C_{3i} \bullet 2^{-m3i}(1 + C_{4i} \bullet 2^{-m4i})]\}.$$

35. Read R-Filter Coefficients

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	1	0	1	1
Output data byte 1:	C40		m40		C30		m30	
Output data byte 2:	C20		m20		C10		m10	
Output data byte 3:	C41		m41		C31		m31	
Output data byte 4:	C21		m21		C11		m11	
Output data byte 5:	C42		m42		C32		m32	
Output data byte 6:	C22		m22		C12		m12	
Output data byte 7:	C43		m43		C33		m33	
Output data byte 8:	C23		m23		C13		m13	
Output data byte 9:	C44		m44		C34		m34	
Output data byte 10:	C24		m24		C14		m14	
Output data byte 11:	C45		m45		C35		m35	
Output data byte 12:	C25		m25		C15		m15	

36. Write Echo Path Gain

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	1	1	0	0
Input data byte 1:	C80		m80		C70		m70	
Input data byte 2:	C60		m60		C50		m50	
Input data byte 3:	C40		m40		C30		m30	
Input data byte 4:	C20		m20		C10		m10	

The equation for the Echo Path Gain is defined as:

$$EPG = 8 \bullet C_{10} \bullet 2^{-m10} \left(1 + C_{50} \bullet 2^{-m50}\{1 + C_{60} \bullet 2^{-m60}[1 + C_{70} \bullet 2^{-m70}(1 + C_{80} \bullet 2^{-m80})]\}\right),$$

C_{20}, M_{20}, C_{30}, M_{30}, C_{40}, and M_{40} must be zero.

37. Read Echo Path Gain

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	1	1	0	1
Output data byte 1:	C80		m80		C70		m70	
Output data byte 2:	C60		m60		C50		m50	
Output data byte 3:	C40		m40		C30		m30	
Output data byte 4:	C20		m20		C10		m10	

38. Write Error Level Threshold

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	1	1	1	0
Input data byte 1:	C20		m20		C10		m10	

The equation for the Echo Path Gain is defined as:

$$ELT = C_{10} \bullet 2^{-m10}(1 + C_{20} \bullet 2^{-m20}).$$

39. Read Error Level Threshold

	D7	D6	D5	D4	D3	D2	D1	D0
Command:	1	0	0	0	1	1	1	1
Output data byte 1:	C20		m20		C10		m10	

Programmable Filters

General Description of CSD Coefficients

The filter functions are performed by a series of multiplications and accumulations. A multiplication is accomplished by repeatedly shifting the multiplicand and summing the result with the previous value at that summation node. The method used in the DSLAC is known as Canonic Signed Digit (CSD) multiplication and splits each coefficient into a series of CSD coefficients.

Each programmable FIR filter section has the following general transfer function:

$$HF(z) = h_0 + h_1z^{-1} + h_2z^{-2} + \ldots + h_nz^{-n} \qquad \text{eq. (1)}$$

where the number of taps in the filter = n + 1.

The transfer function for IIR part of Z and B filters is:

$$HI(z) = \frac{1}{1 - h_{(n+1)}z^{-1}} \qquad \text{eq. (2)}$$

The values of the user-defined coefficients (h_i) are assigned via the MPI. Each of the coefficients (h_i) is defined in the following general equation:

$$h_i = B_1 2^{-M_1} + B_2 2^{-M_2} + \ldots + B_N 2^{-M_N}, \qquad \text{eq. (3)}$$

where:

the number of shifts = $M_i \leq M_{i+1}$

sign = $B_i = \pm 1$

N = Number of CSD coefficients.

The value of h_i in (3) represents a decimal number which is broken down into a sum of successive values of:

± 1.0 multiplied by 2^{-0}, or 2^{-1}, or $2^{-2} \ldots 2^{-7} \ldots$

or

± 1.0 multiplied by 1, or 1/2, or 1/4 ... 1/128....

The limit on the negative powers of 2 is determined by the length of the registers in the ALU.

The coefficient h_i in Equation 3 can be considered to be a value made up of N binary 1s in a binary register where the leftmost part represents whole numbers, the rightmost part represents decimal fractions, and a decimal point separates them. The first binary 1 is shifted M_1 bits to the right of the decimal point, the second binary 1 is shifted M_2 bits to the right of the decimal point, the third binary 1 is shifted M_3 bits to the right of the decimal point, and so on.

Note that when M_1 is 0, the resulting value is a binary 1 in front of the decimal point, that is, no shift. If M_2 is also 0, the result is another binary 1 in front of the decimal point, giving a total value of binary "10" in front of the decimal point (i.e., a decimal value of 2.0). The value of N, therefore, determines the range of values the coefficient h_i can take; for example, if N = 3 the maximum and minimum values are ±3, and if N = 4 the values are between ±4.

Detailed Description of DSLAC Coefficients

The CSD coding scheme in the DSLAC uses a value called m_i, where m_1 represents the distance shifted right of the decimal point for the first binary 1, m_2 represents the distance shifted to the right of the *previous* binary 1, and m_3 represents the number of shifts to the right of the second binary 1. Note that the range of values determined by N is unchanged. Equation 3 is now modified (in the case of N = 4) to:

$$h_i = B_1 2^{-M1} + B_2 2^{-M2} + B_3 2^{-M3} + B_4 2^{-M4} \qquad \text{eq. (4)}$$

$$h_i = C_1 2^{-m1} + C_1C_2 2^{-(m1+m2)} + C_1C_2C_3 2^{-(m1+m2+m3)} + C_1C_2C_3C_4 2^{-(m1+m2+m3+m4)} \qquad \text{eq. (5)}$$

$$h_i = C_1 2^{-m1} \bullet \{1 + C_2 2^{-m2} \bullet [1 + C_3 2^{-m3} \bullet (1 + C_4 2^{-m4})]\} \qquad \text{eq. (6)}$$

where:

$M_1 = m_1$	and	$B_1 = C_1$
$M_2 = m_1 + m_2$		$B_2 = C_1 \bullet C_2$
$M_3 = m_1 + m_2 + m_3$		$B_3 = C_1 \bullet C_2 \bullet C_3$
$M_4 = m_1 + m_2 + m_3 + m_4$		$B_4 = C_1 \bullet C_2 \bullet C_3 \bullet C_4$

In the DSLAC, a coefficient h_i consists of N CSD coefficients, each being made up of 4 bits and formatted as $C_{xy}m_{xy}$, where C_{xy} is one bit (MSB) and m_{xy} is three bits. Each CSD coefficient is broken down as follows:

C_{xy} is the sign bit (0 = positive, 1 = negative).

m_{xy} is the 3-bit shift code. It is encoded as a binary number as follows:

000:	0 shifts
001:	1 shifts
010:	2 shifts
011:	3 shifts
100:	4 shifts
101:	5 shifts
110:	6 shifts
111:	7 shifts

y is the coefficient number (the "i" in h_i).

x is the position of this CSD coefficient within the h_i coefficient. It represents the relative position of the binary 1 represented by this CSD coefficient within the hi coefficient. The most significant binary 1 is represented by x = 1. The next most significant binary 1 is represented by x = 2, and so on.

Thus, $C_{13}m_{13}$ represents the sign and the relative shift position for the first (most significant) binary 1 in the 4th (h_3) coefficient.

The number of CSD coefficients, N, is limited to 4 in the GR, GX, R, X, Z, and the IIR part of the B filter, and 3 for the FIR part of the B filter. Note also that the GX filter coefficient equation is slightly different from that of the other filters:

$$h_{iGX} = 1 + h_i \qquad \text{eq. (7)}$$

Please refer to the section detailing the commands for complete details on the programming of the coefficients.

4

Adaptive B-Filter Overview

The DSLAC B filter is designed to work with pre-programmed coefficients or with coefficients determined by an adaptive algorithm. The adaptive algorithm can be operated in a mode where it continuously adapts (Am79C02A only) or where it adapts for a short period and then holds its value.

Operation with pre-programmed coefficients requires only the use of MPI Command #30 to feed in the coefficients. The adaptive mode uses some pre-programmed coefficients (may be any legal coefficients or zero coefficients) and generates new ones using an algorithm which, by a series of iterations, minimizes the receive signal that is echoed in the transmit signal (due to mismatches in the SLIC, hybrid, and line). Adaptation only applies to the FIR part of the filter.

In the continuous adaptation mode, the algorithm is switched on (via MPI Command #19) after a call is connected and remains on until the call ends. In this way, the B filter is continually being optimized to the received signal.

In the adapt and freeze mode, the algorithm is used only when a line is brought into service and the DSLAC is activated. The algorithm is switched on and is allowed to converge with the received signal, which is a band-limited white noise signal generated in the exchange for this purpose. The noise signal need only be injected for less than a second to yield converged coefficients. The adaptive mode is then switched off (via Command #19).

The converged coefficients may be read out of the DSLAC (using MPI Command #31) and stored for future reference. The DSLAC is now optimized for general input signals.

Adaptive Filter Programming

The purpose of the B filter is to cancel the received signal that leaks across the hybrid into the transmit path. The B filter transfer function must match (as closely as possible) the transfer function of the echo path.

There are two programmable registers associated with the adaptive B filtering. The Echo Path Gain (EPG) is a programmable value that predicts the amount of the receive signal leaking across the hybrid to the transmit path. The EPG is used as part of an algorithm which stops the adaptive filter from iterating in the presence of signals from the subscriber line (near-end talker).

The Error Level Threshold (ELT) is a programmable value that determines the trans-hybrid loss the adaptive filter will attempt to meet. The adaptive algorithm will continue to iterate until it meets the loss requirement specified by the ELT. Both the EPG and ELT values are generated by the AmSLAC-II software program. Please refer to the AmSLAC-II Technical Manual (order no. 10249A).

User Test Modes

The DSLAC supports testing by providing both digital and analog loopback paths as shown in Figure 6. In the TSA Loopback Mode, the DR input is connected to the DX output in the Time Slot Assigner circuitry. The TSA Loopback Mode is programmed via Command #21.

A different type of digital loopback is provided when the AISN register is programmed with a value of "10000." In this case, the AISN circuitry is disabled and the V_{OUT} pad is connected internally to V_{IN}. This allows the D/A and A/D converters to be included in the digital loopback test. This mode is programmed via Command #13. Note that the signal which is connected internally from V_{OUT} to V_{IN} is also present on the V_{OUT} pin.

The V_{IN} input can be connected to the V_{OUT} output through the Z filter for analog loopback. The response of the line to low frequencies can be tested by disabling the high-pass filter. Additionally, the receive and transmit paths may be cut off.

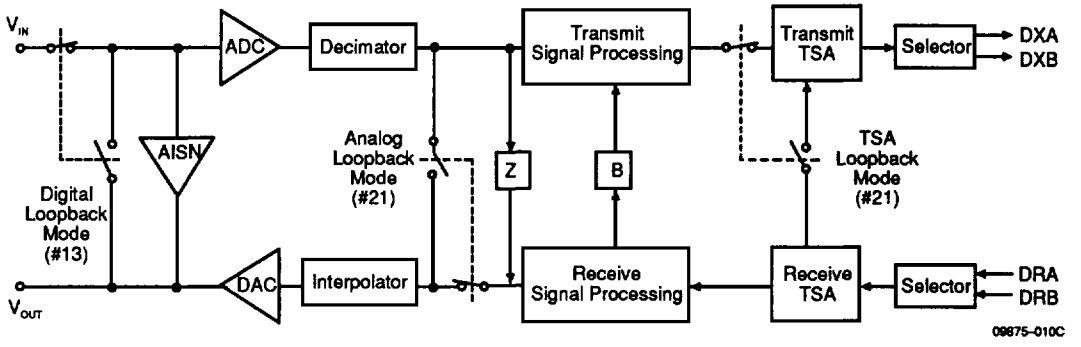


Figure 6. Test Mode Operation

4

APPLICATIONS

The DSLAC performs a programmable CODEC-filter function for two telephone lines. It interfaces to the telephone lines through either a transformer or an electronic SLIC such as the Am795X series devices. The DSLAC provides latched digital I/O to control and monitor two SLICs and has a 256-kHz clock output to operate the switched mode regulator in an Am795X. When several line conditions must be matched, the physical SLIC can be constant, and its characteristics (such as apparent impedance, attenuation, and hybrid balance) can be altered by programming each channel's coefficients to suit the line. For a transformer-based SLIC, the DSLAC can drive the transformer without a buffer.

Connection to a dual, PCM highway backplane is through a simple buffer chip. Several DSLACs can be bussed together into one bus interface buffer. An intelligent bus interface chip is not required because each DSLAC provides its own buffer control. The DSLAC can be controlled through the Microprocessor Interface, either by a microprocessor on the linecard or by a central processor.

Figures 7 and 8 illustrate typical Am79C02 DSLAC applications. Figure 7 shows the basic system architecture. Figure 8 illustrates the significant details of the interface to an Am795X-based SLIC and to a transformer-based SLIC.

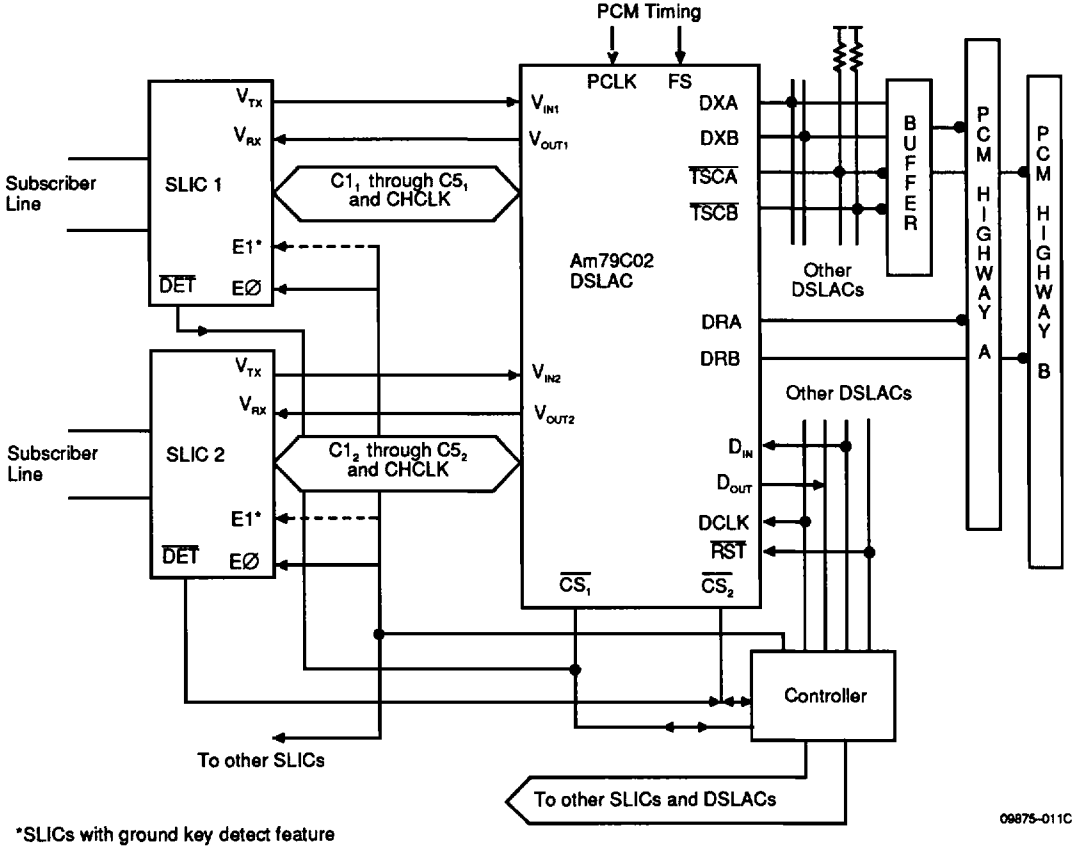


Figure 7. Basic System Architecture

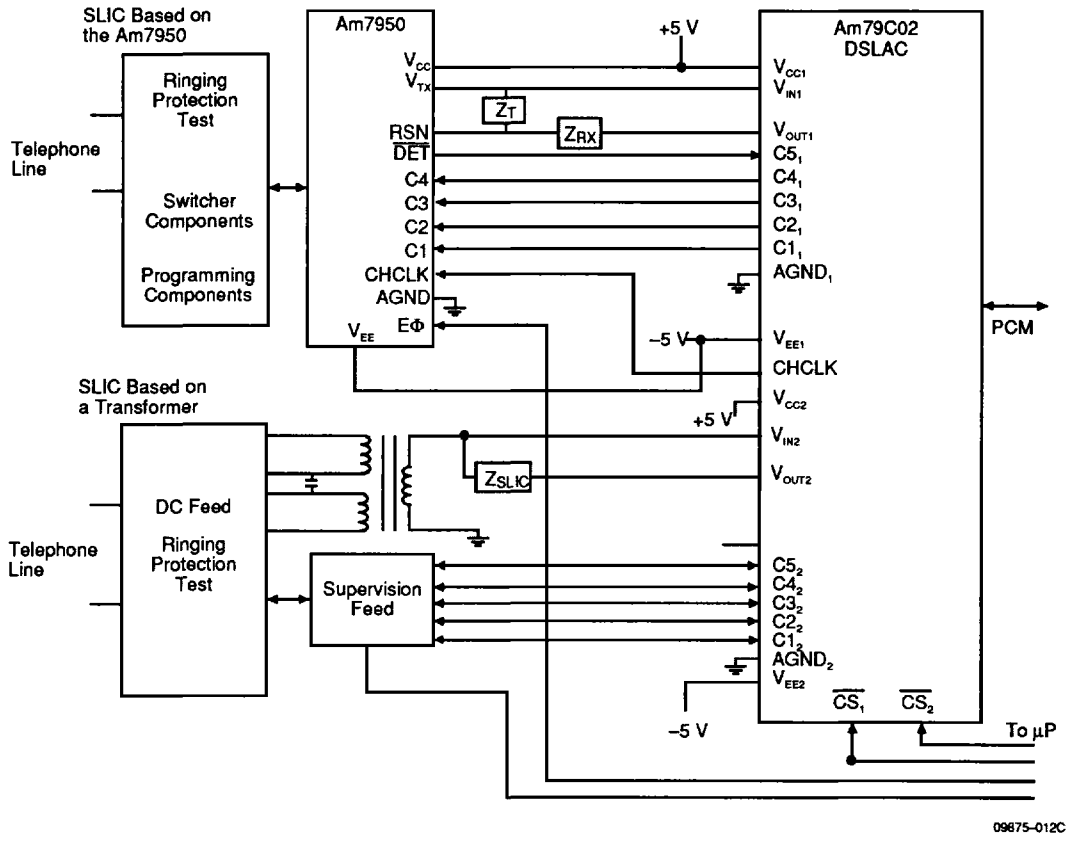


Figure 8. Typical SLIC Connections

Controlling the SLIC

SLIC Chopper Clock

The CHCLK output pin on the DSLAC drives the CHCLK inputs for Am795X series SLICs. The CHCLK output is a 256-kHz TTL-compatible signal that can drive two SLICs. It is only active when one or both channels are activated; otherwise it is held HIGH internally.

SLIC Input/Output

The DSLAC has 5 TTL-compatible I/O pins (C1 to C5) for each channel. On the 40-pin DSLAC, only C1 through C4 are available. On the 44-pin version, C5 (one for each channel) is also available and can be used for another function (for example, to control metering signal injection). The outputs are programmed using Command #15 and the status is read back using Command #16. The direction of the pins (input or output) is specified by programming the SLIC I/O direction register (Command #17).

Calculating Filter Coefficients with AmSLAC-II

AmSLAC-II is a software program which models the DSLAC, the line conditions, the SLIC, and the line card components to obtain the coefficients of the programmable filters of the DSLAC and some of the transmission performance plots.

The following parameters relating to the desired line conditions and the components/circuits used in the line card are to be provided as input to the program:

1. **Line Impedance.** The line impedance or the balance impedance of the line which is usually specified by the local PTT.
2. **Desired Impedance.** This is the desired terminating impedance at the exchange. This impedance is also specified by the local PTT.
3. **SLIC Impedance.** This is the actual terminating impedance at the exchange.
4. **GR Filter Attenuation.** This is the desired attenuation for the GR filter.
5. **GX Filter Gain.** This is the desired gain of the GX filter.
6. **Receive Buffer Transfer Function.** It is quite common to use an amplifier and/or filter between the SLIC and the SLAC in the design of the line card. The

transfer function of this amplifier/filter is called the Receive Buffer Transfer Function.

7. **Transmit Buffer Transfer Function**. Same as the Receive Buffer Transfer Function but for the Transmit path.
8. **Fuse Resistance and Coupling**. This is the value of the Fuse Resistance and the Coupling capacitor used in the line card.
9. **Two-Wire Return Loss Template**. The Two-Wire Return Loss Template is usually specified by the local PTT.
10. **Four-Wire Return Loss Template**. The Four-Wire Return Loss Template is usually specified by the local PTT.

The output from the AmSLAC-II program includes the coefficients of the GR, GX, Z, R, X, B, and EPG filters as well as transmission performance plots of (1) two-wire return loss, (2) receive and transmit path frequency response, and (3) four-wire return loss.

The software supports the use of the AMD Am795X series SLICs or a transformer SLIC, or allows entry of the transfer functions describing the behavior of any type of SLIC (hybrid).

Systems for Customer Evaluation

The DSLAC Low Noise Evaluation Board is designed to demonstrate the high performance capabilities of the DSLAC. The board is used to evaluate the DSLAC available in a 40-pin DIP package.

The SLAC/DSLAC Computer Interface Board provides a friendly, computer-driven interface to control up to two DSLAC Low Noise Evaluation Boards or SLAC Low Noise Boards. The Computer Interface Board allows an IBM®-compatible PC-XT™ or PC-AT™ to control a SLAC, DSLAC, and a SLIC via its serial port. The board is designed to operate with the DSLACIF software program which runs on the PC. A block diagram of a typical lab setup is shown in Figure 9.

The Computer Interface Board can also interface to a Hewlett-Packard 3779 series PMA or a Wandel and Goltermann (W&G) PCM-4. These PCM Channel Measurement Sets are used to measure the quality of signal transmission through the DSLAC.

An RS-232C serial port on the SLAC/DSLAC Computer Interface Board is designed to plug directly into a serial port on the back of a PC. The DSLACIF program which controls the Computer Interface Board will operate on an IBM PC-XT, PC-AT, or compatible computer containing at least 1 serial port and having at least 512 KB of memory. The program is capable of running from a floppy disk (360 KB) or from a hard disk. The DSLACIF program is completely menu driven and an extensive on-line HELP facility is available.

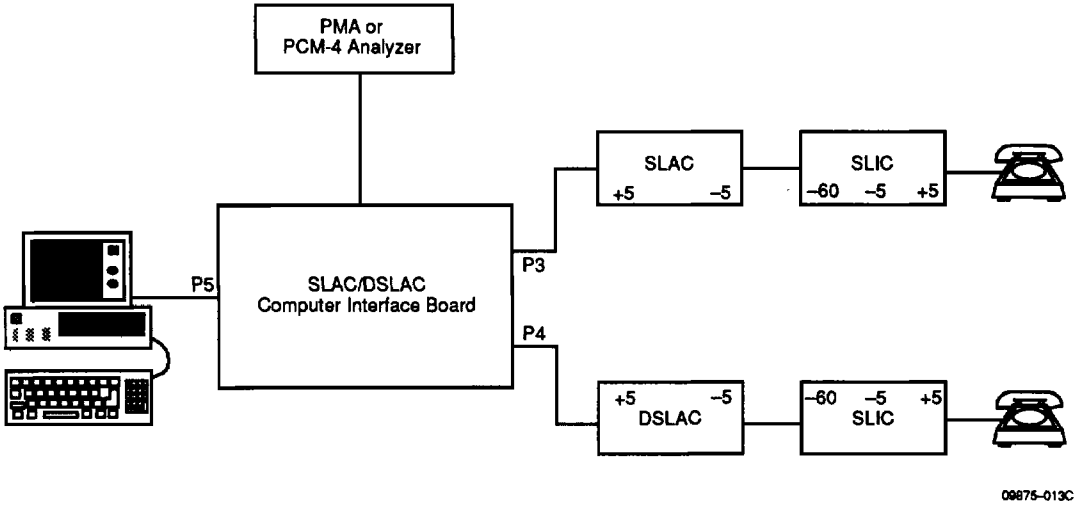


Figure 9. Evaluation System Block Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	$-60 \le T_A \le +125°C$
Ambient Operating Temperature	$-40 \le T_A \le +85°C$
Ambient relative humidity (noncondensing)	5% to 100%
V_{CCA1} with respect to AGND	−0.4 V to +6.0 V
V_{CCA2} with respect to AGND	−0.4 V to +6.0 V
V_{CCD1} with respect to $DGND_1$	−0.4 V to +6.0 V
V_{CCD2} with respect to $DGND_2$	−0.4 V to +6.0 V
V_{CCP} with respect to PGND	−0.4 V to +6.0 V
V_{EE1} with respect to AGND	+0.4 V to −6.0 V
V_{EE2} with respect to AGND	+0.4 V to −6.0 V
V_{IN} with respect to V_{CCA} (V_{EE} = −5 V)	+0.4 V to −10.0 V
V_{IN} with respect to V_{EE} (V_{CCA} = +5 V)	−0.4 V to +10.0 V
Any other pin with respect to $DGND_1$	−0.4 V to V_{CC}

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Analog Supply V_{CCA1}, V_{CCA2}	+5.0 V ±5%
Digital Supply V_{CCD1}, V_{CCD2}, V_{CCP}	+5.0 V ±5%
Analog Supply V_{EE1}, V_{EE2}	−5.0 V ±5%
$DGND_1$, $DGND_2$, PGND	0 V
$AGND_1$, $AGND_2$	±50 mV
Ambient Temperature	$0 \le T_A \le +70°C$
Ambient Relative Humidity	15% to 85%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise noted

Typical values are for T_A = 25°C and nominal supply voltages. Minimum and maximum specifications are over the temperature and supply voltage ranges shown in "Operating Ranges."

Parameter Symbol	Parameter Descriptions	Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Voltage	−0.5		0.8	V
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V
I_{IL}	Input Leakage Current			±10	µA
V_{OL}	Output LOW Voltage (I_{OL} = −2 mA)			0.4	V
V_{OH}	Output HIGH Voltage (I_{OH} = 400 µA)	2.4			V
V_{OLTSC}	Output LOW Voltage on $\overline{TSCA}$, $\overline{TSCB}$ (I_{OL} = 14 mA)			0.4	V
I_{OL}	Output Leakage Current (H_i-Z State)			±10	µA
V_{IR}	Analog input Voltage Range (AX = 0 dB) (AX = 6.02 dB)			±3.1466 ±1.5733	V V
V_{IOS}	Offset Voltage allowed on V_{IN}			±35	mV
I_{IL} (V_{IN})	Input Leakage Current on V_{IN}			±10	µA
Z_{OUT}	V_{OUT} output impedance		1	10	ohms
I_{OUT}	V_{OUT} output current (f < 3400 Hz) (Note 1)			±6.3	mA
V_{OR}	V_{OUT} Voltage Range (AR = 0 dB) (AR = −6.02 dB)			±3.1466 ±1.5733	V V
V_{OOS}	V_{OUT} Offset Voltage (AISN off)			±15	mV
V_{OOSA}	V_{OUT} Offset Voltage due to AISN			±15	mV
LIN_{AISN}	Linearity of AISN circuitry (input = 0 dBm0)			±1/4	LSB
PD	Power Dissipation both channels active 1 channel active both channels inactive (Note 2)		180 120 12	300 160	mW mW mW
I_{CC}	Total +5 V current, both channels active 1 channel active both channels inactive (Note 2)		24 18 2.5		mA mA mA
I_{EE}	Total −5 V current, both channels active 1 channel active both channels inactive (Note 2)		10 5 0.05		mA mA mA
C_I	Input Capacitance (Digital)		15		pF
C_O	Output Capacitance (Digital)		15		pF
PSSR	Power Supply Rejection Ratio (1.02 kHz, 100 mV_{RMS}, either supply or path, GX = GR = 0dB)	40			dB

Notes: 1. When the DSLAC is in the inactive mode, the analog output will present a 0 V output level through an ~3K resistor.
2. Power Dissipation in the inactive mode is measured with all digital inputs at $V_{ih} = V_{CC}$ and $V_{il} = V_{SS}$ and with no load connected to V_{OUT1} or V_{OUT2}.

Transmission Characteristics

When the gain in the receive path is set at 0 dB, an 813-Hz PCM sine wave input with level 0 dBm0 will correspond to a nominal RMS voltage of 1.55 volts for μ-law and 1.555 volts for A-law at the analog output. When the gain in the transmit path is set at 0 dB, an 813-Hz sine wave signal with a nominal RMS voltage of 1.55 volts for μ-law and 1.555 volts for A-law will correspond to a level of 0 dBm0 at the digital output.

When relative levels (dBm0) are used in any of the following transmission specifications, the specification holds for any setting of the AX + GX gain from 0 to 12 dB and the AR + GR loss from 0 to 12 dB. Performance specification for settings of the AX + GX gain from 12 to 18 dB and the AR + GR loss from 12 to 18 dB will be determined as the device is characterized.

These performance specifications are valid for the commercial temperature range device only. The specifications for the industrial temperature range device will be released after full characterization.

Gain Stability

For a 0 dBm0 813-Hz (A-law) or 1014-Hz (μ-law) sine wave signal, the gains in the transmit and in the receive path (with B = 0, Z = 0 & X = R = 1) will not deviate from their ideal value by more than ±0.2 dB.

The variation of the digital to digital loop gain (when the analog input and output ports are connected together) or the analog to analog loop gain (when the digital input and output ports are connected together) will be within ±0.2 dB. The above specifications apply with reference to aging, temperature, and supply voltage variations within the specifications of the "Operating Ranges".

Attenuation Distortion

The attenuation of the signal in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown. The reference frequency is 813 Hz and the signal level is 0 dBm0. The deviation is less than ±0.125 dB for 300 Hz < f < 3000 Hz.

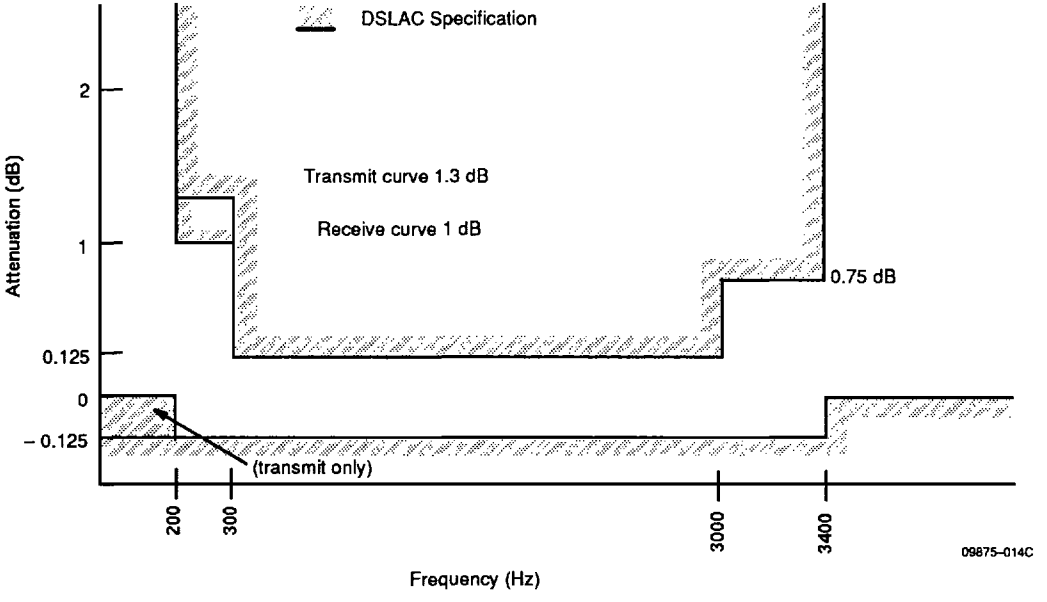


Figure 10. Attenuation Distortion (Single Ended)

Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

Group Delay

The Group Delay spec is defined as the sum of the minimum values of the group delays for the transmit and the receive paths when the transmit and receive time slots are identical and the B, X, R, and Z filters are disabled. For PCLK frequencies of greater than 1.536 MHz, the group delay is less than 630 µs. For PCLK frequencies of less than 1.025 MHz, the group delay is less than 695 µs. (At PCLK frequencies between these two values, the group delay may vary from one cycle to the next.)

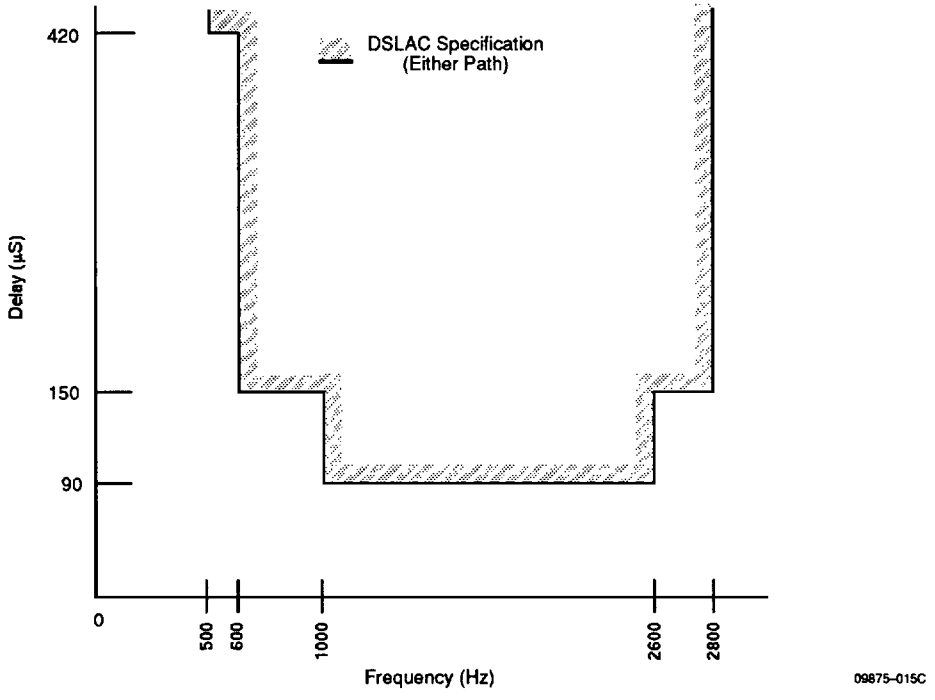


Figure 11. Group Delay Distortion

Discrimination Against Out-of-Band Input Signals

When an out-of-band sine wave signal with frequency f and level A is applied to the analog input, the level of any frequency component below 4 kHz at the digital output, caused by the out-of-band signal, is at least the specified dB level below the level of a signal at the same output originating from an 813-Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are:

Frequency of out-of-band signal	Amplitude of out-of-band signal	Level below A
16.6 Hz < f < 60 Hz	−25 dBm0 < A < 0 dBm0	20 dB
60 Hz < f < 100 Hz	−25 dBm0 < A < 0 dBm0	10 dB
3400 Hz < f < 4600 Hz	−25 dBm0 < A < 0 dBm0	see Figure 12
4600 Hz < f < 72 kHz	−25 dBm0 < A < 0 dBm0	32 dB
4600 Hz < f < 100 kHz	A = 0 dBm0	35 dB

The attenuation of the waveform below amplitude A between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Attenuation (dB)} = 14 - 14 \sin \frac{\pi(4000-f)}{1200}$$

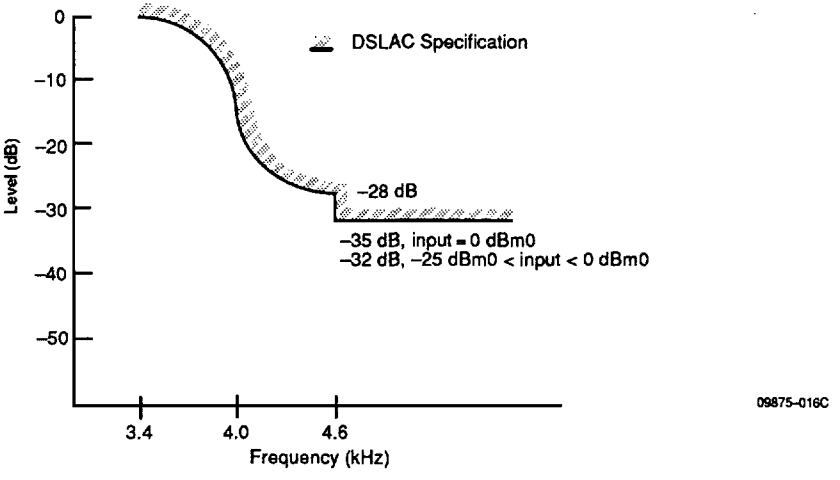


Figure 12. Discrimination Against Out-of-Band Signals

Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals between 4.6 kHz and 24 kHz at the analog output is less than –32 dBm0. The level of spurious out-of-band signals between 24 kHz and 90 kHz is given by:

$(23 - 40 \bullet \log_{10} f)$,

where f is the frequency in kHz.

Between 90 kHz and 1 MHz, the signal at the analog output is less than –55 dBV. With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 13. The amplitude of the Spurious Out-of-Band signals between 3400 Hz and 4600 Hz is given by the formula:

$$A = -14 - 14 \sin \frac{\pi (f - 4000)}{1200}$$

Harmonic Distortion

The output signal level, at any single frequency in the range of 300 Hz to 3400 Hz, other than that due to an applied 0 dBm0 sine wave signal with frequency f in the same frequency range, is less than –46 dBm0. With f swept between 0 to 300 Hz and 3400 to 12 kHz, any generated output signals other than f are less than –28 dBm0. This specification is valid for either transmission path.

Intermodulation Distortion

Two sine wave signals of different frequencies f_1 and f_2 (not harmonically related) in the range 300 Hz to 3400 Hz and of equal levels in the range –4 dBm0 to –21 dBm0 do not produce any

$2 \bullet f_1 - f_2$

products having a level greater than –42 dB relative to the level of the two input signals.

A sine wave signal in the frequency band 300 Hz to 3400 Hz with input level –9 dBm0 and a 50-Hz signal with input level –23 dBm0, will not give any intermodulation products exceeding a level of –56 dBm0. These specifications are valid for either transmission path.

Idle Channel Noise

When the signal at the analog input is zero and the digital output (DXA or DXB) is connected to the digital input (DRA or DRB), the maximum levels of the noise measured at the analog output are:

Weighted noise:	–68 dBm0p
Unweighted noise (300–3400 Hz):	–55 dBm0

When the signal at the analog input is zero, the maximum level of the noise measured at the digital output does not exceed –68 dBm0p (A-law) or 19 dBrnc0 (μ-law). When PCM code words representing zero volts are applied to the digital input, the maximum level of the noise measured at the analog output does not exceed –78 dBm0p (A-law) or 12 dBrnc0 (μ-law). No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.

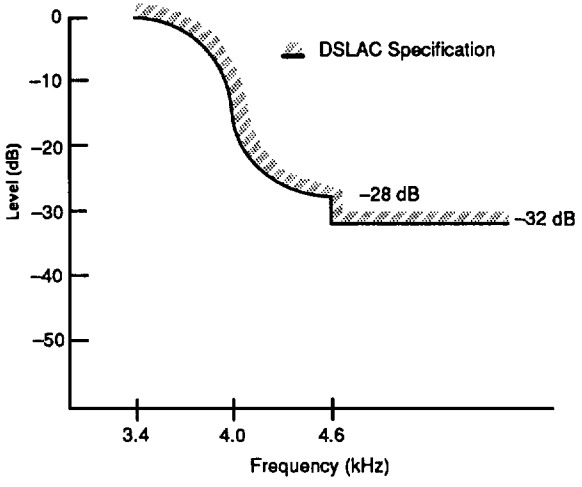


Figure 13. Spurious Out-of-Band Signals

Crosstalk

Transmit to Receive crosstalk within a channel. The crosstalk level at the analog output due to a 0 dBm0 sine wave signal in the frequency range 300 Hz to 3400 Hz, applied to the analog input, is less than –75 dBm0.

Receive to Transmit crosstalk within a channel. The crosstalk level at the digital output due to a 0 dBm0 sine wave signal in the frequency range 300 Hz to 3400 Hz, applied to the digital input, is less than –75 dBm0.

Transmit to Transmit crosstalk between channels. With a 0 dBm0 sine wave signal in the frequency range 300 Hz to 3400 Hz applied to the analog input of one channel, the level at the digital output of the other channel does not exceed –76 dBm0.

Transmit to Receive crosstalk between channels. The crosstalk level at the analog output of one channel due to a 0 dBm0 sine wave signal in the frequency range 300 Hz to 3400 Hz, applied to the analog input of the other channel, will be less than –78 dBm0.

Receive to Transmit crosstalk between channels. The crosstalk level at the digital output of one channel due to a 0 dBm0 sine wave signal in the frequency range 300 Hz to 3400 Hz, applied to the digital input of the other channel, will be less than –76 dBm0.

Receive to Receive crosstalk between channels. The crosstalk level at the analog output of one channel due to a 0dBm0 sine wave signal in the frequency range 300Hz to 3400 Hz, applied to the digital input of the other channel, will be less than –78 dBm0.

Variation of Gain with Input Level

The gain deviation relative to the gain at –10 dBm0 is within the limits shown for either transmission path when the input signal is a noise signal (for example, CCITT Rec. O.131).

The gain deviation relative to the gain at –10 dBm0 is within the limits shown for either transmission path when the input is a sine wave signal in the frequency range 700 Hz to 1100 Hz (excluding submultiples of 8 kHz).

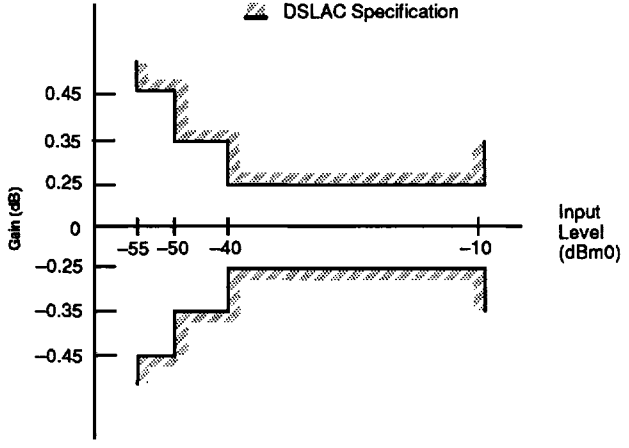


Figure 14. Gain Tracking with Noise Input

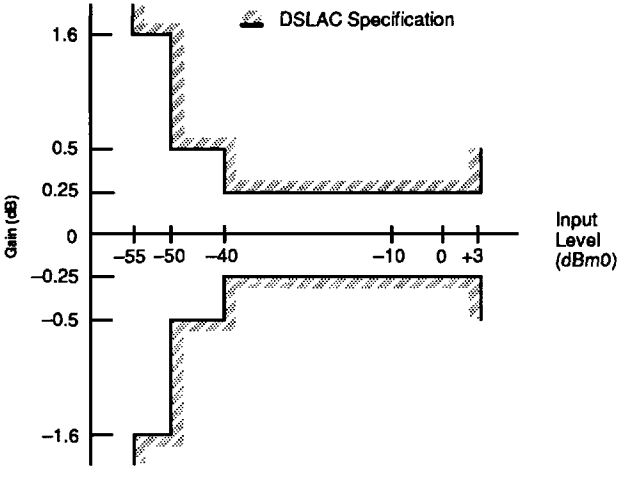


Figure 15. Gain Tracking with Tone Input

Total Distortion, Including Quantizing Distortion

The signal-to-total distortion ratio will exceed the limits shown for the receive path when the input signal is a noise signal (for example, CCITT Rec. O.131). The transmit path specification is 1 dB less than that shown for the receive path.

The signal-to-total distortion will exceed the limits shown for either transmission path when the input is a sine wave signal in the frequency range 700 Hz to 1100 Hz (excluding submultiples of 8 kHz).

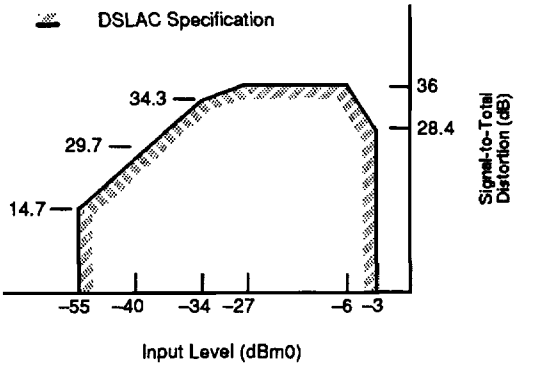


Figure 16. Total Distortion with Noise Input (Receive Path)

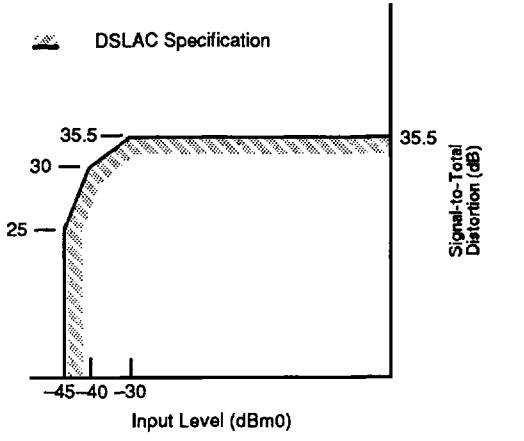


Figure 17. Total Distortion with Tone Input (Both Paths)

Overload Compression

Figure 18 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0).

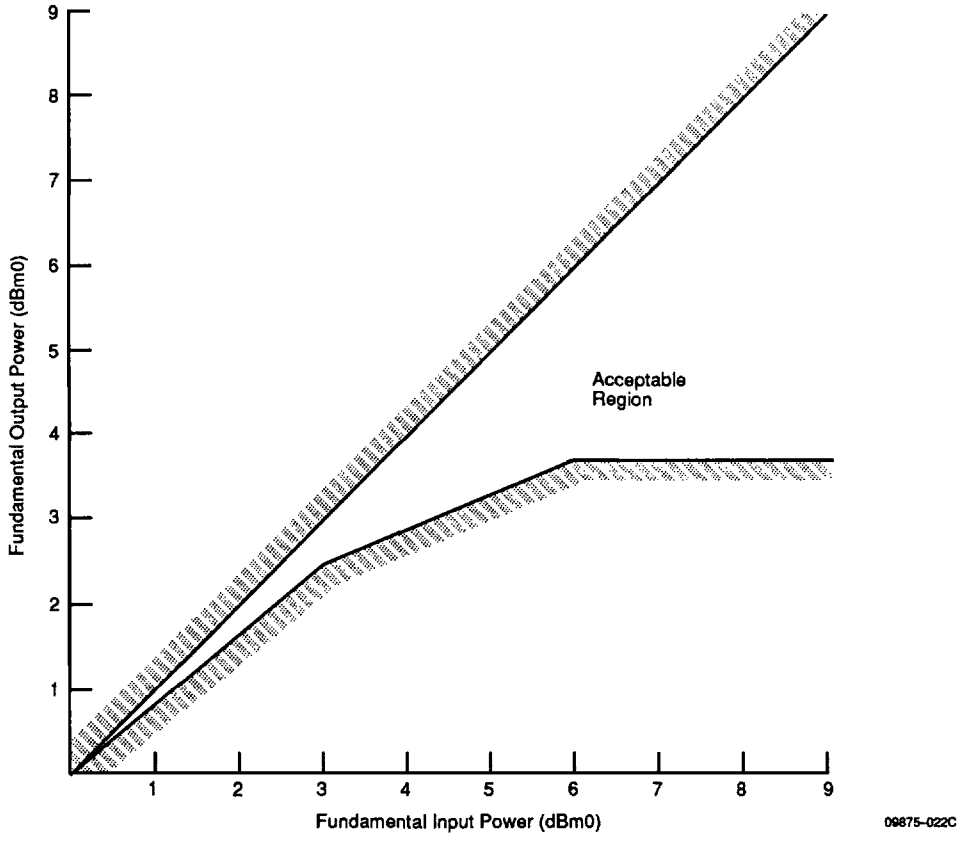


Figure 18. Overload Compression

SWITCHING CHARACTERISTICS over operating range unless otherwise noted

Microprocessor Interface

Min. and Max. values are valid for all digital outputs with a 150 pF load, except C1 to C5 with a 30 pF load. Pullup resistors of 360 ohms are attached to $\overline{TSCA}$ and $\overline{TSCB}$.

No.	Symbol	Parameter	Min.	Typ.	Max.	Units
1	t_{DCY}	Data Clock Period	244			ns
2	t_{DCH}	Data Clock HIGH Pulse Width (Note 1)	97			ns
3	t_{DCL}	Data Clock LOW Pulse Width (Note 1)	97			ns
4	t_{DCR}	Rise Time of Clock			25	ns
5	t_{DCF}	Fall Time of Clock			25	ns
6	t_{ICSS}	Chip Select Setup Time, Input Mode	70		t_{DCY}	ns
7	t_{ICSH}	Chip Select Hold Time, Input Mode	0		t_{DCH} –20	ns
8	t_{ICSL}	Chip Select Pulse Width, Input Mode		8t_{DCY}		ns
9	t_{ICSO}	Chip Select off Time, Input Mode (Note 7)		5		µs
10	t_{IDS}	Input Data Setup Time	30			ns
11	t_{IDH}	Input Data Hold Time	30			ns
12	t_{OLH}	SLIC Output Latch Valid	20		1000	ns
13	t_{OCSS}	Chip Select Setup Time, Output Mode	70		t_{DCY}	ns
14	t_{OCSH}	Chip Select Hold Time, Output Mode	0		t_{DCH} –20	ns
15	t_{OCSL}	Chip Select Pulse Width, Output Mode		8t_{DCY}		ns
16	t_{OCSO}	Chip Select Off Time, Output Mode (Note 7)		5		µs
17	t_{ODD}	Output Data Turn On Delay (Note 5)			50	ns
18	t_{ODH}	Output Data Hold Time	10			ns
19	t_{ODOF}	Output Data Turn off Delay			50	ns
20	t_{ODC}	Output Data Valid	10		50	ns

PCM Interface

No.	Symbol	Parameter	Min.	Typ.	Max.	Units
21	t_{PCY}	PCM Clock Period (Note 2)	0.122		7.8125	µs
22	t_{PCH}	PCM Clock HIGH Pulse Width	48		3890	ns
23	t_{PCL}	PCM Clock LOW Pulse Width	48		3890	ns
24	t_{PCF}	Fall Time of Clock			15	ns
25	t_{PCR}	Rise Time of Clock			15	ns
26	t_{FSS}	FS Setup Time	25		t_{PCY}–50	ns
27	t_{FSH}	FS Hold Time	50			ns
28	t_{TSD}	Delay to $\overline{TSC}$ Valid (with Programmable Delay) (Note 3)	5 30		80 80	ns ns
29	t_{TSO}	Delay to $\overline{TSC}$ off (with Programmable Delay) (Note 6)	5 30		80 80	ns ns
30	t_{DXD}	PCM Data Output Delay (with Programmable Delay) (Note 4)	3 30		70 150	ns ns
31	t_{DXH}	PCM Data Output Hold Time (with Programmable Delay) (Note 4)	5 30		70 150	ns ns
32	t_{DXZ}	PCM Data Output Delay to High-Z (with Programmable Delay) (Note 4)	5 30		70 150	ns ns
33	t_{DRS}	PCM Data Input Setup Time	25		70	ns
34	t_{DRH}	PCM Data Input Hold Time	5		150	ns

Master Clock

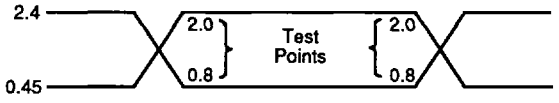
For 2.048 MHz ± 100 ppm or 4.096 MHz ± 100 ppm operation:

No.	Symbol	Parameter	Min.	Typ.	Max.	Units
35	t_{MCY}	Master Clock Period (2.048 MHz)	488.23	488.28	488.33	ns
		Master Clock Period (4.096 MHz)	244.11	244.14	244.17	ns
36	t_{MCR}	Rise Time of Clock			15	ns
37	t_{MCF}	Fall Time of Clock			15	ns
38	t_{MCH}	MCLK HIGH Pulse Width (2.048 MHz)	200			ns
		MCLK HIGH Pulse Width (4.096 MHz)	80			ns
39	t_{MCL}	MCLK LOW Pulse Width (2.048 MHz)	200			ns
		MCLK LOW Pulse Width (4.096 MHz)	80			ns

Notes
1. DCLK may be stopped in the HIGH or LOW state indefinitely without loss of information. If DCLK is stopped in the HIGH state, $\overline{CS}$ can subsequently make any number of transitions without activating the Microprocessor Interface logic.
2. The maximum allowed PCM clock frequency is 8.192 MHz. The actual PCM clock rate is dependent on the number of channels allocated within a frame. The minimum clock frequency is 128 kHz. A PCLK of 1.544 MHz may easily be used for standard U.S. transmission systems.
3. TSC is delayed from FS by a typical value of $N \cdot t_{PCY}$, where N is the value stored in the time/clock-slot register.
4. There is a special conflict detection circuitry which will prevent high power dissipation from occurring when the DXA or DXB pins of two DSLACs are tied together and one DSLAC starts to transmit before the other has gone into a high impedance state.
5. The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.
6. t_{TSO} is defined as the time at which the output achieves the open circuit condition.
7. The DSLAC requires 40 cycles of the 8-MHz internal clock (5 µs) between SIO operations. If the MPI is being accessed while the MCLK input is not active, a Chip Select Off time of 20 µs is required.

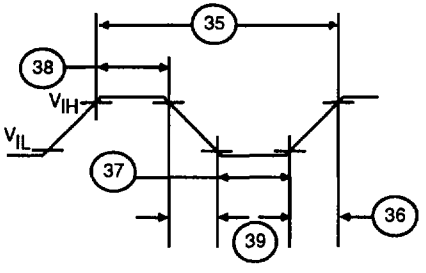
SWITCHING WAVEFORMS

Input and Output Waveforms for AC Tests



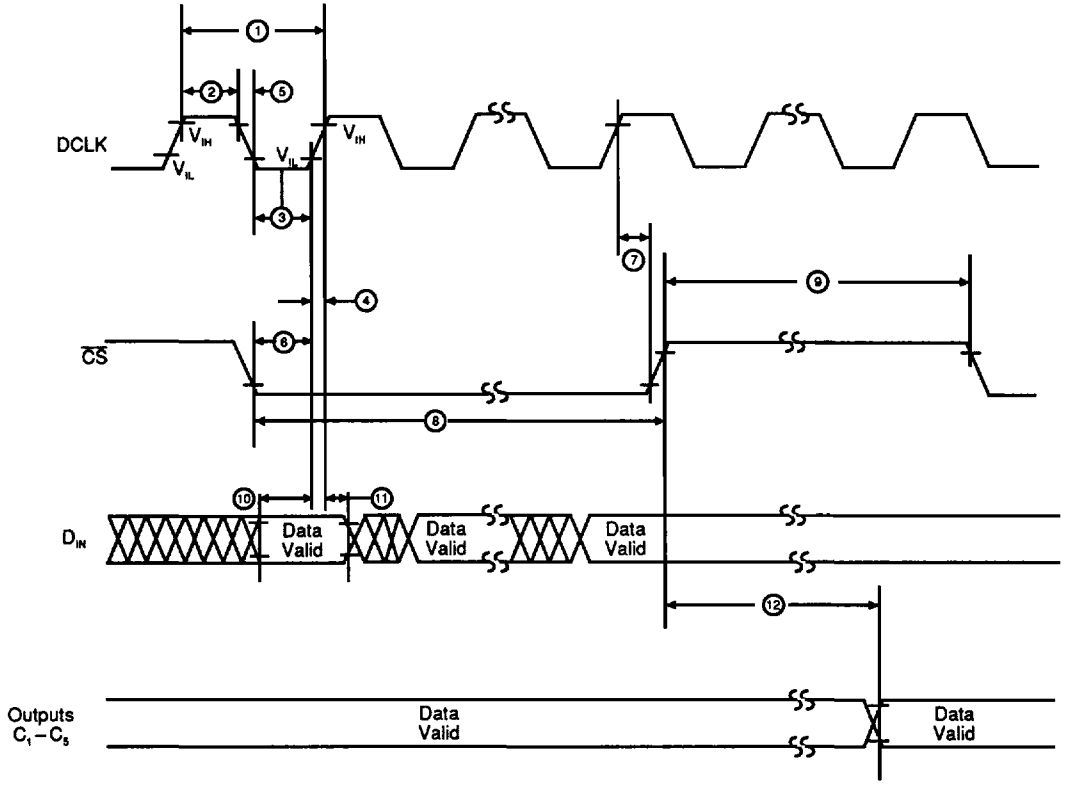
09875-023C

Master Clock Timing



09875-024C

Microprocessor Interface (Input Mode)



09875-025C

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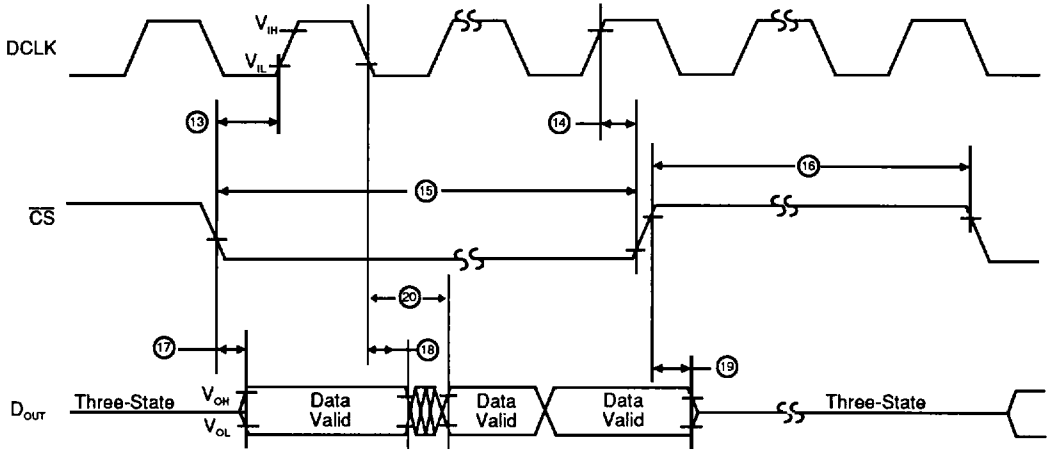
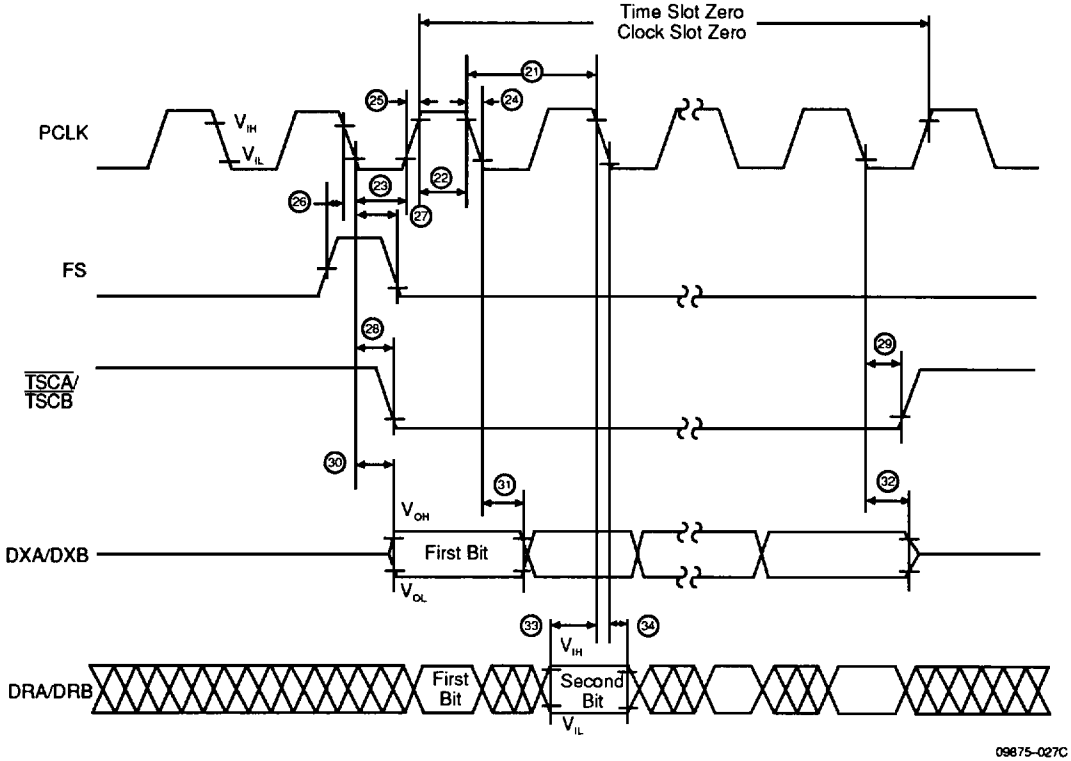
Microprocessor Interface (Output Mode)



09875-026C

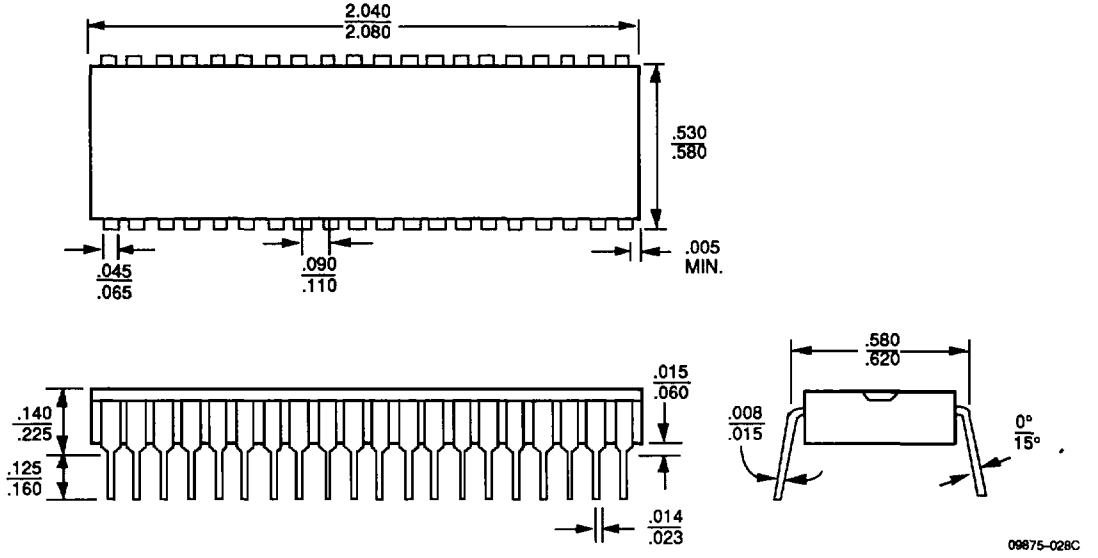
PCM Highway Timing



09875-027C

PHYSICAL DIMENSIONS

PD 040



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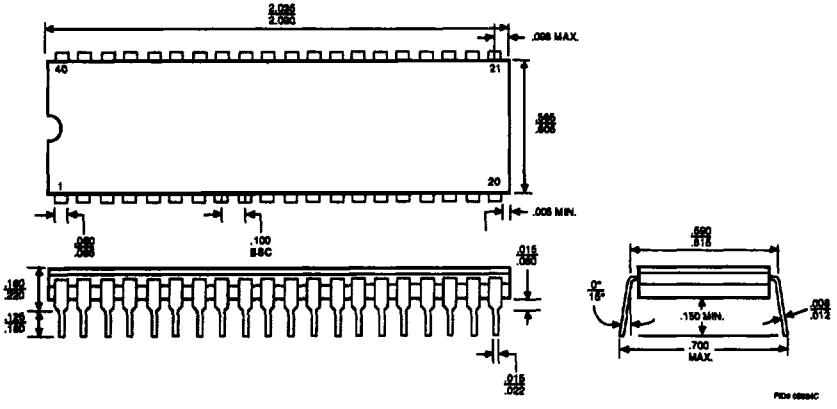
PHYSICAL DIMENSIONS

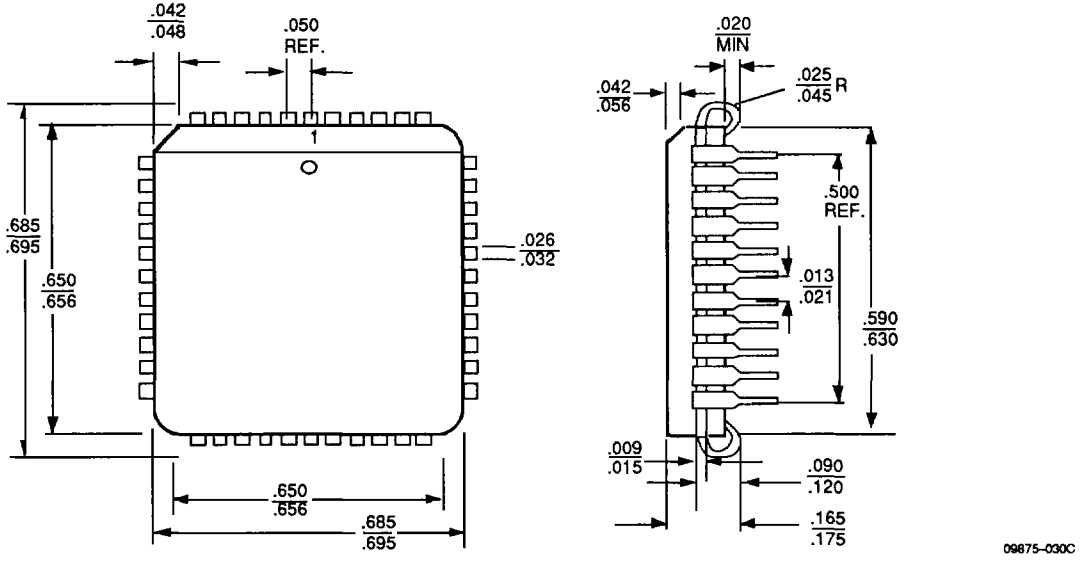
CD 040



09875-029C

PHYSICAL DIMENSIONS

PL 044



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