SPEED/PACKAGE AVAILABILITY

74 A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

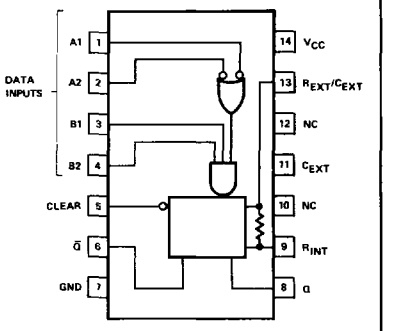
TEST CONDITIONS		FROM INPUT	TO OUTPUT	74 C_L=15pF R_L=400Ω MIN	TYP	MAX	UNIT
$t_{wq(min)}$					45	65	ns
t_{wq}					C_{ext} = 1000pF R_{ext} = 10kΩ		
				3.08	3.42	3.76	ns
$t_{w(in)}$				40			ns
R_{ext}	External timing resistance			(54) 5		25	kΩ
				(74) 5		50	
C_{ext}	External timing capacitance				No restriction		μf
	Wiring cap. at R_{ext}/C_{ext} terminal					50	pF
					C_{ext} = 0 R_{ext} = 5kΩ		
Propagation delay time							
t_{PLH}	Low-to-high	Either A	Q		22	33	ns
t_{PHL}	High-to-low	Either A	$\overline{Q}$		30	40	
t_{PLH}	Low-to-high	Either B	Q		19	28	
t_{PHL}	High-to-low	Either B	$\overline{Q}$		27	36	
t_{PLH}	Low-to-high	Clear	$\overline{Q}$		30	40	
t_{PHL}	High-to-low	Clear	Q		18	27	

Load circuit and typical waveforms are shown at the front of section.

$t_w = 0.32\ R_T C_{ext}\left(1 + \frac{0.7}{R_T}\right)$

PIN CONFIGURATION

A,F PACKAGE



TRUTH TABLE

INPUTS A_1	A_2	B_1	B_2	OUTPUTS Q	Q
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎍
L	X	H	↑	⎍	⎍
X	L	H	H	L	H
X	L	↑	H	⎍	⎍
X	L	H	↑	⎍	⎍
H	↓	H	H	⎍	⎍
↓	↓	H	H	⎍	⎍
	H	H	H	⎍	⎍

NOTES:

A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎍ = one low-level pulse, X = irrelevant (any input, including transitions).

B. NC = no internal connection.

C. To use the internal timing resistor of N74122 (10kΩ nominal), connect R_{int} to V_{CC}.

D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).