



MACH131-7/10/12/15/20

High-Density EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 64 Macrocells
- 7.5 ns t_{PD}
- 133 MHz f_{CNT}
- 70 Bus-Friendly Inputs
- Peripheral Component Interconnect (PCI) Compliant
- Programmable power-down mode
- 64 Outputs
- 64 Flip-flops; 4 clock choices
- 4 "PAL26V16" Blocks
- Pin-compatible with MACH130, MACH230, MACH231, MACH435
- JEDEC compatible with MACH130

GENERAL DESCRIPTION

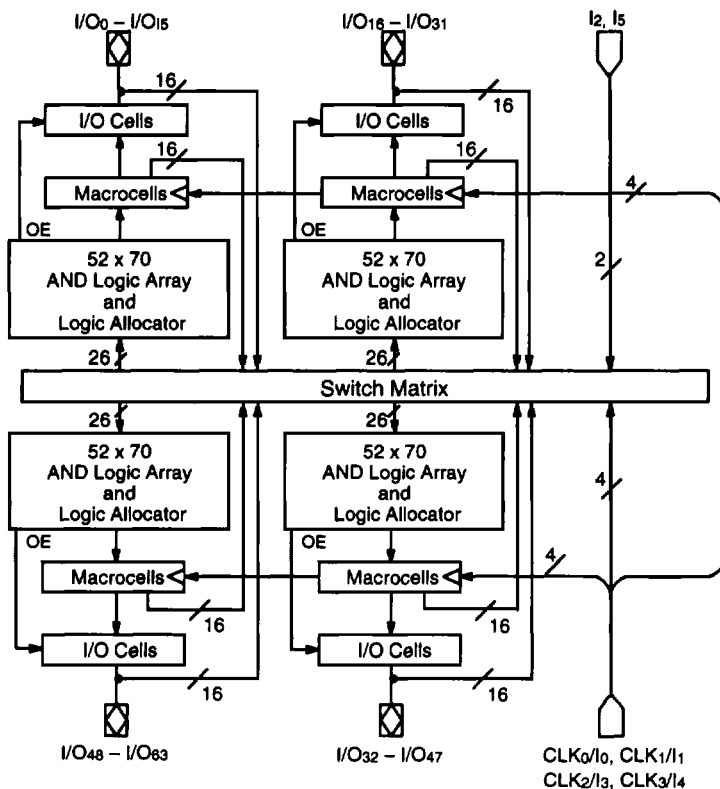
The MACH131 is a member of AMD's EE CMOS Performance Plus MACH 1 family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH131 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL26V12" structures complete with product-term arrays and programmable macrocells, including additional buried macrocells. The switch matrix connects the PAL blocks to each other and to all

input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH131 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell.

BLOCK DIAGRAM



18889C-1