

Description

The PUMA 84 range of devices provide a high density, surface mount memory solution with density up to twice that of standard monolithic devices.

The PUMA 84 may accommodate various memory technologies including SRAM, FLASH and EEPROM. The devices are designed to offer a defined upgrade path and may be user configured as 8, 16 or 32 bits wide using eight Chip Selects (/CS1~8).

The PUMA84SV32000 is a 1Mx32 SRAM module housed in a JEDEC 84 pin surface mount J-ledged PLCC. Access times of 12, 15 or 20ns are available. The 3.3V low voltage device is available to commercial and industrial temperature grade.

The -L version has data retention capability and can be used in battery backup applications.

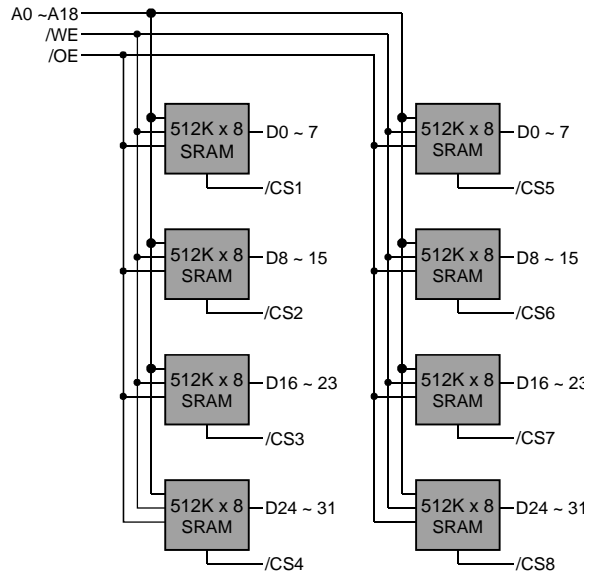
Features

- Access times of 12/15/20 ns.
- 3.3V ± 10%.
- Commercial and Industrial temperature grades
- JEDEC 84 'J' Ledged surface mount package.
- Industry standard pinout.
- May be organised as 1M x 32, 2M x 16 and 4M X 8
- Operating Power (32 Bit) 3.53W (max)
- Low power standby. (CMOS) 360mW (max)
- Low voltage data retention mode.
- Completely Static Operation.

Package Details

PUMA 84 - Plastic 84 'J' Ledged Package.
Max. Dimensions - 30.35 x 30.35 x 8.50 (max)
All Dimensions in mm.

Block Diagram



Pin Definition

See page 2.

Pin Functions

Description	Signal
Address Input	A0~A18
Data Input/Output	D0~D31
Chip Select	/CS1~8
Write Enable	/WE
Output Enable	/OE
No Connect	NC
Power	V _{CC}
Ground	GND

Pin Definition - PUMA84SV32000

Pin	Signal	Pin	Signal
1	V _{CC}	43	V _{CC}
2	NC	44	A13
3	/CS1	45	A12
4	/CS2	46	A11
5	/CS3	47	A10
6	/CS4	48	A9
7	A17	49	A8
8	A18	50	A7
9	D16	51	D0
10	NC	52	NC
11	NC	53	NC
12	NC	54	NC
13	NC	55	NC
14	D17	56	D1
15	D18	57	D2
16	D19	58	D3
17	V _{SS}	59	V _{SS}
18	D20	60	D4
19	D21	61	D5
20	D22	62	D6
21	D23	63	D7
22	V _{CC}	64	V _{CC}
23	D24	65	D8
24	D25	66	D9
25	D26	67	D10
26	D27	68	D11
27	V _{SS}	69	V _{SS}
28	D28	70	D12
29	D29	71	D13
30	D30	72	D14
31	NC	73	NC
32	NC	74	NC
33	NC	75	D15
34	NC	76	A14
35	D31	77	A15
36	A6	78	A16
37	A5	79	/WE
38	A4	80	/OE
39	A3	81	/CS5
40	A2	82	/CS6
41	A1	83	/CS7
42	A0	84	/CS8

Absolute Maximum Ratings⁽¹⁾

Parameter	Symbol	Min		Max	Unit
Voltage on any pin relative to V _{SS}	V _T ⁽²⁾	-0.5	to	+4.6	V
Power Dissipation	P _T			4.0	W
Storage Temperature	T _{STG}	-55	to	+125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

(2) V_T can be -2.0V pulse of less than 8ns

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	
Supply Voltage	V _{CC}	3.0	3.3	3.6	V	
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL}	-0.3	-	0.8	V	
Operating Temperature	T _A	0	-	70	°C	
	T _{AI}	-40	-	85	°C	(I Suffix)

Notes : (1) Pulse Width : -2.0V for less than 10ns.

DC Electrical Characteristics

(V_{CC}=3.3V±10%, T_A=-40°C to +85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current Address, /OE, /WE	I _{LI}	0V ≤ V _{IN} ≤ V _{CC}	-20	-	20	µA
Output Leakage Current	I _{LO}	/CS=V _{IH} , V _{I/O} = GND to V _{CC}	-20	-	20	µA
Average Supply Current ⁽¹⁾	32 Bit	I _{CC32} Min Cycle /CS ⁽²⁾ =V _{IL} , f=f _{max} , I _{OUT} =0mA	-	-	980	mA
	16 Bit	I _{CC16} As Above.	-	-	690	mA
	8 Bit	I _{CC8} As Above.	-	-	545	mA
Standby Supply Current	TTL	I _{SB} /CS=V _{IH} , f=f _{max}	-	-	400	mA
	CMOS	I _{SB1} /CS≥V _{CC} -0.2V, 0.2 ≤V _{IN} ≤V _{CC} -0.2V, f=0	-	-	100	mA
Output Voltage Low	V _{OL}	I _{OL} =8.0mA	-	-	0.4	V
Output Voltage High	V _{OH}	I _{OH} =-4.0mA	2.4	-	-	V

Notes (1) Typical values are at V_{CC}=3.3V, T_A=25°C and specified loading.

(2) /CS above refers to /CS1-4 for 16 Bit mode and /CS5-8 for 32 bit mode.

(3) At f=f_{MAX} address and data inputs are cycling at max frequency.

Capacitance

($V_{CC} = 3.3V \pm 10\%$, $T_A = 25^\circ C$)

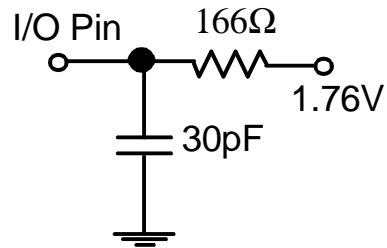
Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Input Capacitance	Address, /OE, /WE	C_{IN1}	$V_{IN}=0V$	-	-	70	pF
Input Capacitance	(Other)	C_{IN2}	$V_{IN}=0V$	-	-	12	pF
Output Capacitance	8 bit mode (worst case)	$C_{I/O}$	$V_{I/O}=0V$	-	-	70	pF

Note : These Parameters are calculated not measured.

Test Conditions

- Input pulse levels : 0V to 3.0V
- Input rise and fall times : 3ns
- Input and Output timing reference levels : 1.5V
- Output Load : See Load Diagram.
- $V_{CC} = 3.3V \pm 10\%$

Output Load



Operation Truth Table

/CS	/OE	/WE	Data Pins	Supply Current	Mode
H	X	X	High Impedance	I_{SB}, I_{SB1}	Standby
L	L	H	Data Out	$I_{CC32}, I_{CC16}, I_{CC8}$	Read
L	H	L	Data In	$I_{CC32}, I_{CC16}, I_{CC8}$	Write
L	L	L	Data In	$I_{CC32}, I_{CC16}, I_{CC8}$	Write
L	H	H	High Impedance	I_{SB}, I_{SB1}	High Z

Notes : $H = V_{IH}$; $L = V_{IL}$; $X = V_{IH}$ or V_{IL}

The above table reflects the operation of each of the RAMS on the module. Care should be taken to avoid bus contention on data lines using chip select signals.

Read Cycle

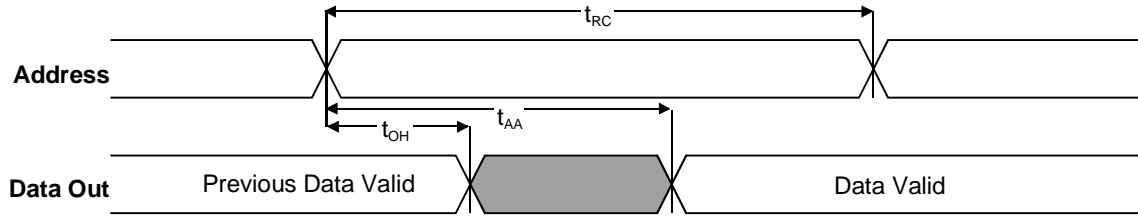
		012		015		020		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	t _{RC}	12	-	15	-	20	-	ns
Address Access Time	t _{AA}	-	12	-	15	-	20	ns
Chip Select Access Time	t _{ACS}	-	12	-	15	-	20	ns
Output Enable to Output Valid	t _{OE}	-	6	-	7	-	9	ns
Output Hold From Address Change	t _{OH}	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t _{CLZ}	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t _{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	t _{CHZ}	0	6	0	7	0	9	ns
Output Disable to Output in High Z	t _{OHZ}	0	6	0	7	0	9	ns

Write Cycle

		012		015		020		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	t _{WC}	12	-	15	-	20	-	ns
Chip Selection to End of Write	t _{CW}	10	-	12	-	15	-	ns
Address Valid to End of Write	t _{AW}	10	-	12	-	15	-	ns
Address Setup Time	t _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	10	-	12	-	12	-	ns
Write Pulse Width (/OE Low)	t _{WP}	12	-	15	-	20	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Write to Output in High Z	t _{WHZ}	0	6	0	7	0	9	ns
Data to Write Time Overlap	t _{DW}	6	-	7	-	9	-	ns
Data Hold time from Write Time	t _{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW}	3	-	3	-	3	-	ns

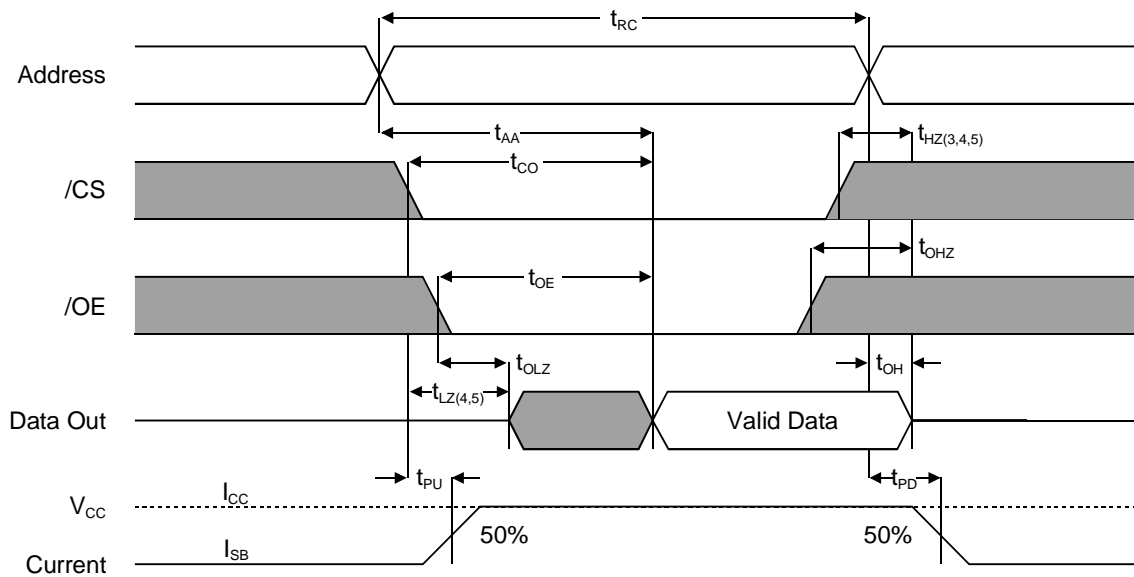
Read Cycle 1

(Address Controlled, /CS=/OE= V_{IL} , /WE= V_{IH})



Read Cycle 2

(/WE = V_{IH})

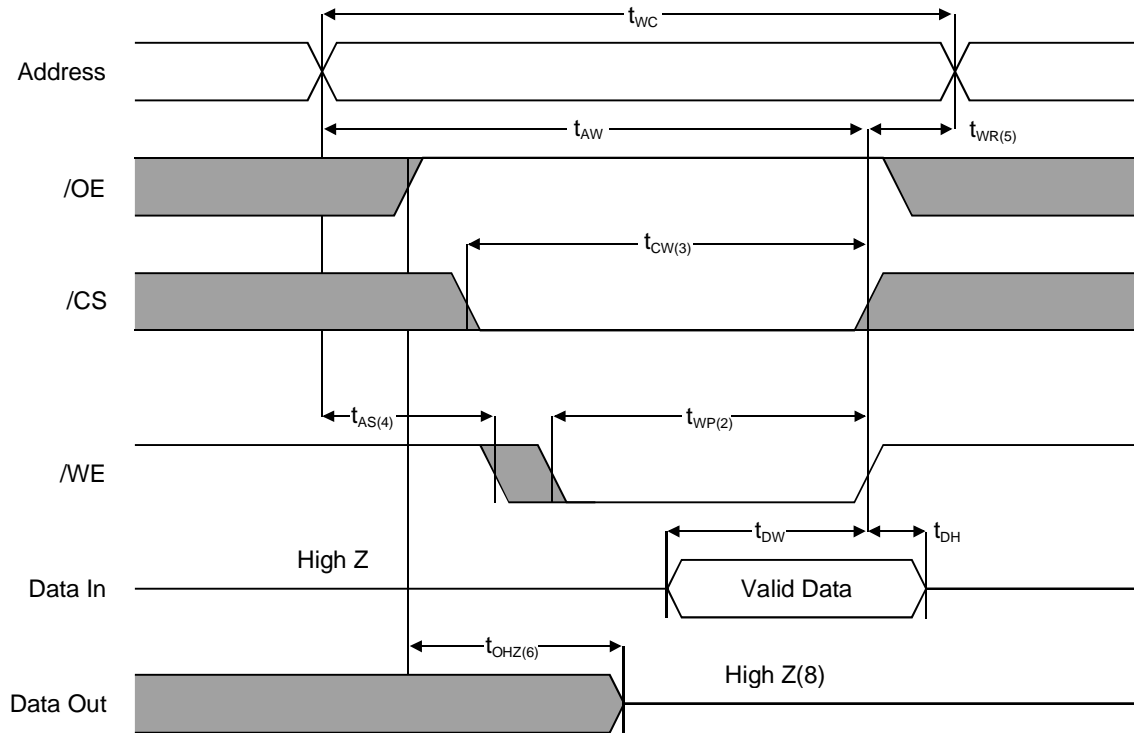


NOTES(READ CYCLE)

1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with /CS= V_{IL} .
7. Address valid prior to coincident with /CS transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

Write Cycle 1

(/OE = Clock)

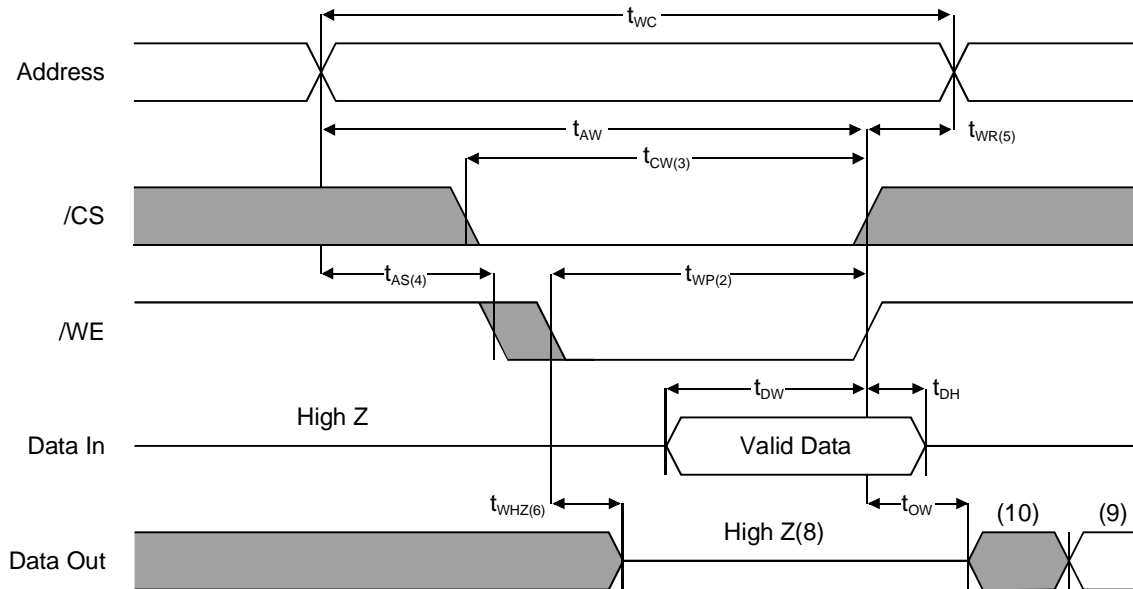


NOTES(WRITE CYCLE)

- All write cycle timing is referenced from the last valid address to the first transition address.
- A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
- t_{CW} is measured from the later of /CS going low to end of write.
- t_{AS} is measured from the address valid to the beginning of write.
- t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
- If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
- For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
- If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
- Dout is the read data of the new address.
- When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Write Cycle 2

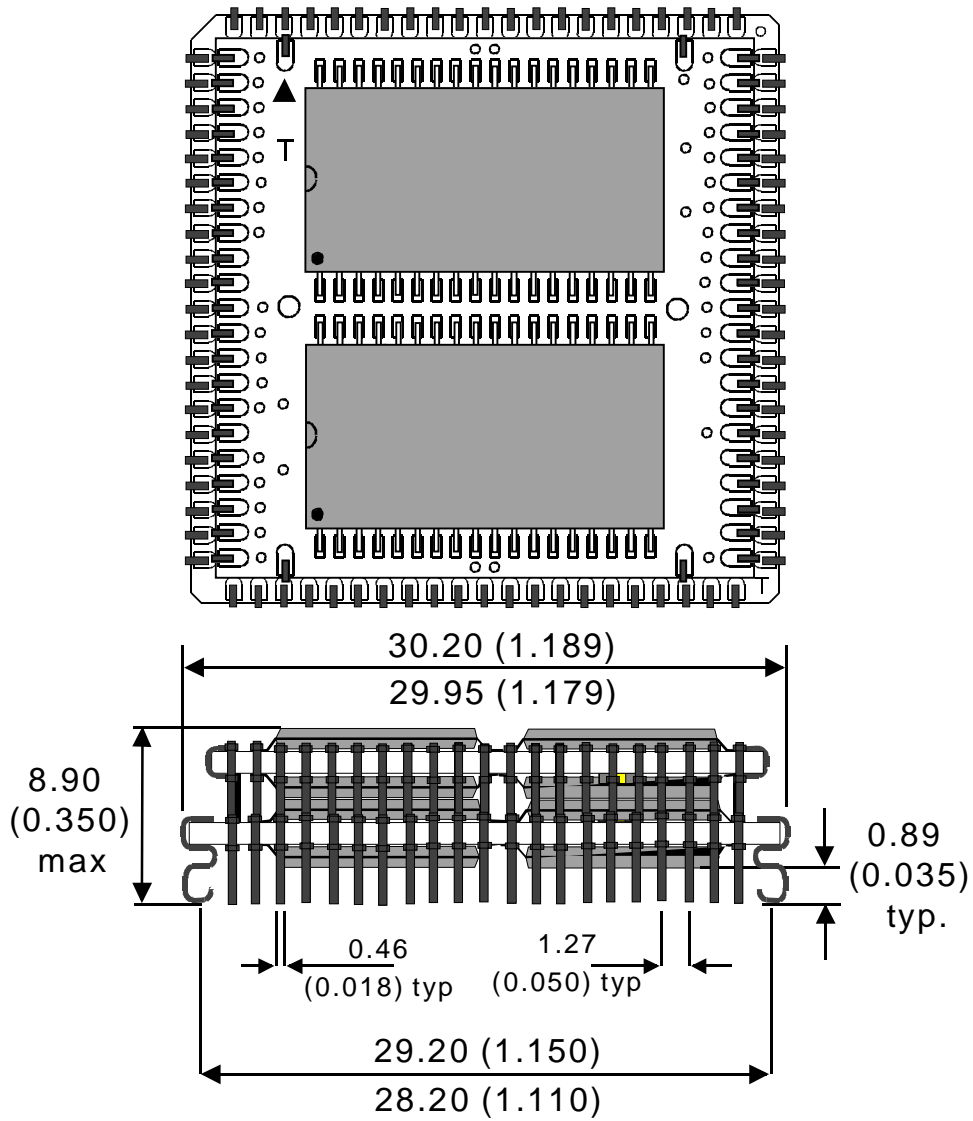
(/OE = Low Fixed)



NOTES(WRITE CYCLE)

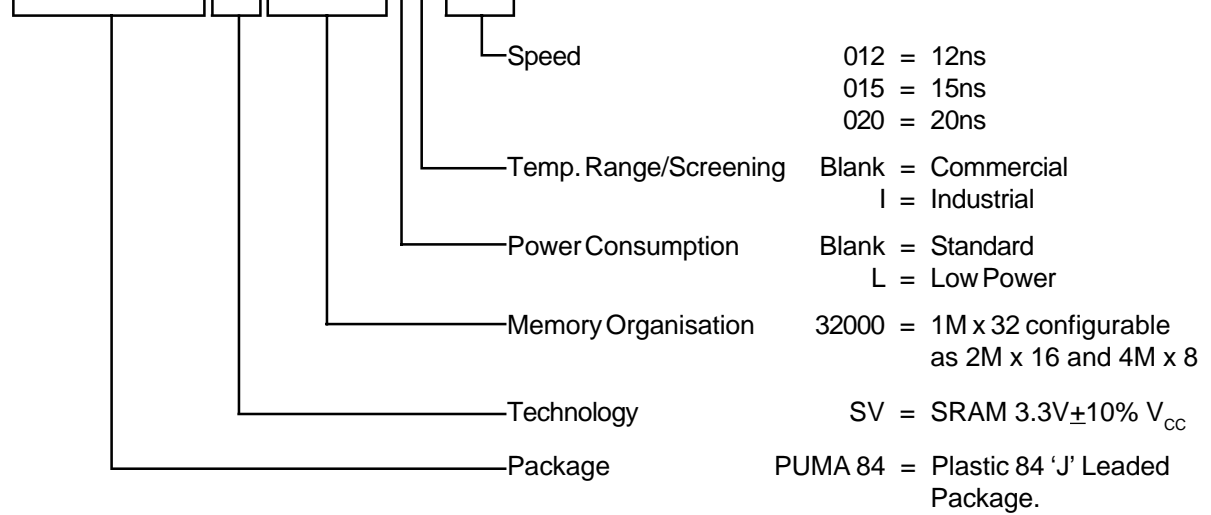
1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

PUMA 84 - Plastic 84 'J' Leaded Package.



Ordering Information

PUMA 84SV32000LI-012



Note :

Although this data is believed to be accurate the information contained herein is not intended to and does not create any warranty of merchantability or fitness for a particular purpose.

Our products are subject to a constant process of development. Data may be changed without notice.

Products are not authorised for use as critical components in life support devices without the express written approval of a company director.