

HN58C256AI Series

R10DS0218EJ0100

Rev.1.00

256k EEPROM (32-kword × 8-bit)

Oct 07, 2013

Description

Renesas Electronics' HN58C256AI are electrically erasable and programmable ROMs organized as 32768-word × 8-bit. They have realized high speed low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

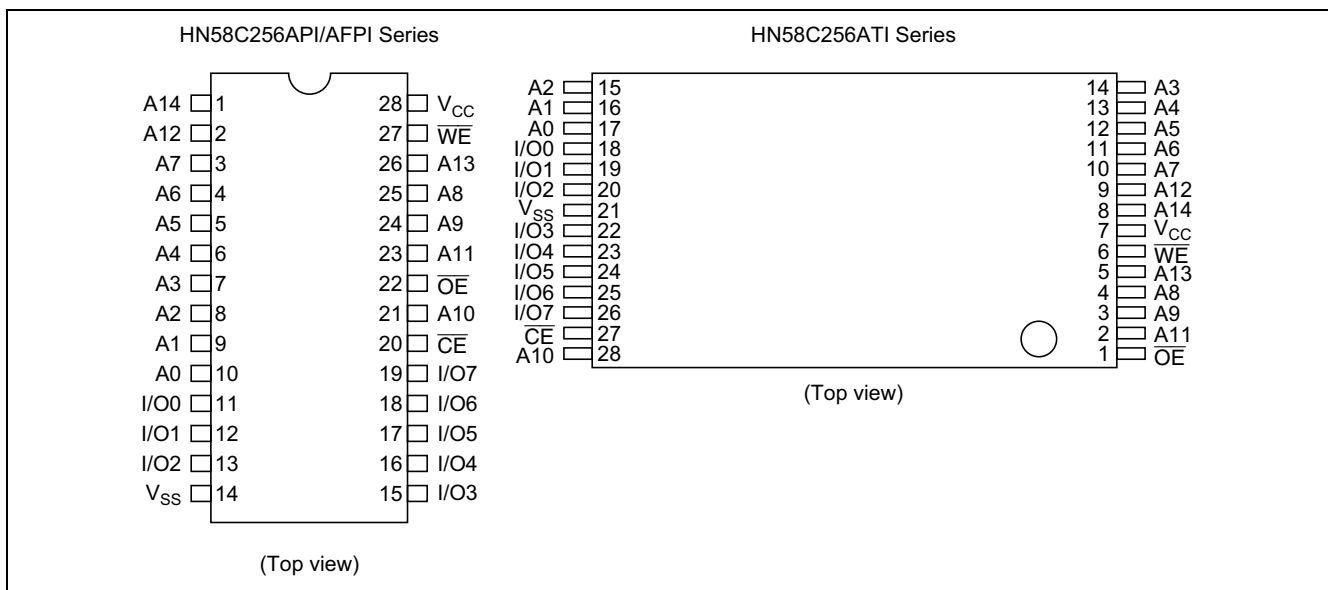
Features

- Single 5 V supply: 5 V ±10%
- Access time: 85 ns/100 ns (max)
- Power dissipation
 - Active: 20 mW/MHz, (typ)
 - Standby: 110 μW (max)
- On-chip latches: address, data, \overline{CE} , \overline{OE} , \overline{WE}
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Data polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10⁵ erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- There are lead free products

Ordering Information

| Orderable Part Name | Access time | Package | Shipping Container | Quantity |
|---------------------|-------------|---|--------------------|--|
| HN85C256API85E | 85ns | 600mil 28-pin plastic DIP PRDP0028AB-A (DP-28V) | Tube | Max. 13 pcs/tube Max. 325 pcs/inner box |
| HN85C256API10E | 100ns | | | |
| HN85C256AFPI85E | 85ns | 400mil 28-pin plastic SOP PRSP0028DC-A (FP-28DV) | Tube | Max. 25 pcs/tube Max. 1,000 pcs/inner box |
| HN85C256AFPI10E | 100ns | | | |
| HN85C256AFPI85EZ | 85ns | | Tape and reel | 1,000 pcs/reel |
| HN85C256AFPI10EZ | 100ns | | | |
| HN85C256ATI85E | 85ns | 28-pin plastic TSOP PTSA0028ZB-A (TFP-28DBV) | Tray | Max. 60 pcs/tray Max. 600 pcs/inner box |
| HN85C256ATI10E | 100ns | | | |

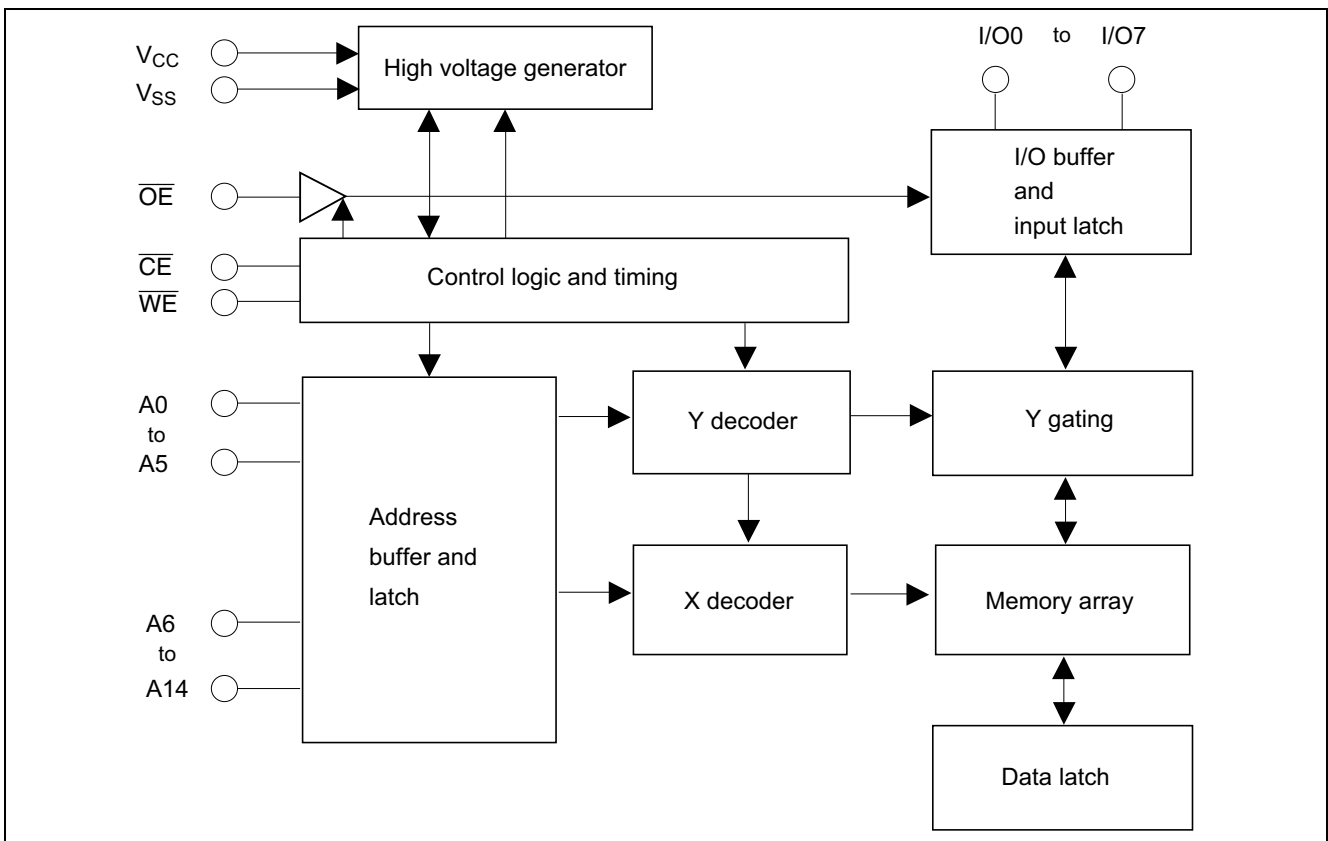
Pin Arrangement



Pin Description

| Pin Name | Function |
|-----------------|-------------------|
| A0 to A14 | Address input |
| I/O0 to I/O7 | Data input/output |
| \overline{OE} | Output enable |
| \overline{CE} | Chip enable |
| \overline{WE} | Write enable |
| V_{CC} | Power supply |
| V_{SS} | Ground |
| NC | No connection |

Block Diagram



Operation Table

| Operation | \overline{CE} | \overline{OE} | \overline{WE} | I/O |
|---------------|-----------------|-----------------|-----------------|-------------|
| Read | V_{IL} | V_{IL} | V_{IH} | Dout |
| Standby | V_{IH} | \times^{*1} | \times | High-Z |
| Write | V_{IL} | V_{IH} | V_{IL} | Din |
| Deselect | V_{IL} | V_{IH} | V_{IH} | High-Z |
| Write inhibit | \times | \times | V_{IH} | — |
| | \times | V_{IL} | \times | — |
| Data polling | V_{IL} | V_{IL} | V_{IH} | Dout (I/O7) |
| Program reset | \times | \times | \times | High-Z |

Note: 1. Don't care

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|-----------|--|------|
| Power supply voltage relative to V_{SS} | V_{CC} | -0.6 to +7.0 | V |
| Input voltage relative to V_{SS} | V_{in} | -0.5 ^{*1} to +7.0 ^{*3} | V |
| Operating temperature range ^{*2} | T_{opr} | -40 to +85 | °C |
| Storage temperature range | T_{stg} | -55 to +125 | °C |

- Notes: 1. V_{in} min: -3.0 V for pulse width \leq 50 ns
 2. Including electrical characteristics and data retention
 3. Should not exceed $V_{CC} + 1$ V.

Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|-----------------------|-----------|--------------------|-----|------------------------------|------|
| Supply voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input voltage | V_{IL} | -0.3 ^{*1} | — | 0.6 | V |
| | V_{IH} | 3.0 | — | $V_{CC} + 0.3$ ^{*2} | V |
| Operating temperature | T_{opr} | -40 | — | +85 | °C |

- Notes: 1. V_{IL} min: -1.0 V for pulse width \leq 50 ns
 2. V_{IH} max: $V_{CC} + 1.0$ V for pulse width \leq 50 ns

DC Characteristics

(Ta = -40 to +85°C, V_{CC} = 5.0 V ±10%)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|-----------------------------------|------------------|-----------------------|-----|-----|------|---|
| Input leakage current | I _{LI} | — | — | 2 | μA | V _{CC} = 5.5 V, V _{in} = 5.5 V |
| Output leakage current | I _{LO} | — | — | 2 | μA | V _{CC} = 5.5 V, V _{out} = 5.5/0.4 V |
| Standby V _{CC} current | I _{CC1} | — | — | 20 | μA | $\overline{CE} = V_{CC}$ |
| | I _{CC2} | — | — | 1 | mA | $\overline{CE} = V_{IH}$ |
| Operating V _{CC} current | I _{CC3} | — | — | 12 | mA | I _{out} = 0 mA, Duty = 100%, Cycle = 1 μs, V _{CC} = 5.5 V |
| | | — | — | 30 | mA | I _{out} = 0 mA, Duty = 100%, Cycle = 85 ns, V _{CC} = 5.5 V |
| Output low voltage | V _{OL} | — | — | 0.4 | V | I _{OL} = 2.1 mA |
| Output high voltage | V _{OH} | V _{CC} × 0.8 | — | — | V | I _{OH} = -400 μA |

Capacitance

(Ta = +25°C, f = 1 MHz)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------------------------|------------------|-----|-----|-----|------|------------------------|
| Input capacitance* ¹ | C _{in} | — | — | 6 | pF | V _{in} = 0 V |
| Output capacitance* ¹ | C _{out} | — | — | 12 | pF | V _{out} = 0 V |

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics

(Ta = -40 to +85°C, V_{CC} = 5.0 V ±10%)

Test Conditions

- Input pulse levels: 0.4 V to 3.0 V
- Input rise and fall time: ≤ 5 ns
- Input timing reference levels: 0.8, 2.0 V
- Output load: 1TTL Gate +100 pF
- Output reference levels: 1.5 V, 1.5 V

Read Cycle

| Parameter | Symbol | HN58C256API/AFPI/ATI | | | | Unit | Test conditions |
|---|------------------|----------------------|-----|-----|-----|------|--|
| | | -85 | | -10 | | | |
| | | Min | Max | Min | Max | | |
| Address to output delay | t _{ACC} | — | 85 | — | 100 | ns | $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ |
| \overline{CE} to output delay | t _{CE} | — | 85 | — | 100 | ns | $\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ |
| \overline{OE} to output delay | t _{OE} | 10 | 40 | 10 | 50 | ns | $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$ |
| Address to output hold | t _{OH} | 0 | — | 0 | — | ns | $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ |
| \overline{OE} (CE) high to output float* ¹ | t _{DF} | 0 | 40 | 0 | 40 | ns | $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$ |

Write Cycle

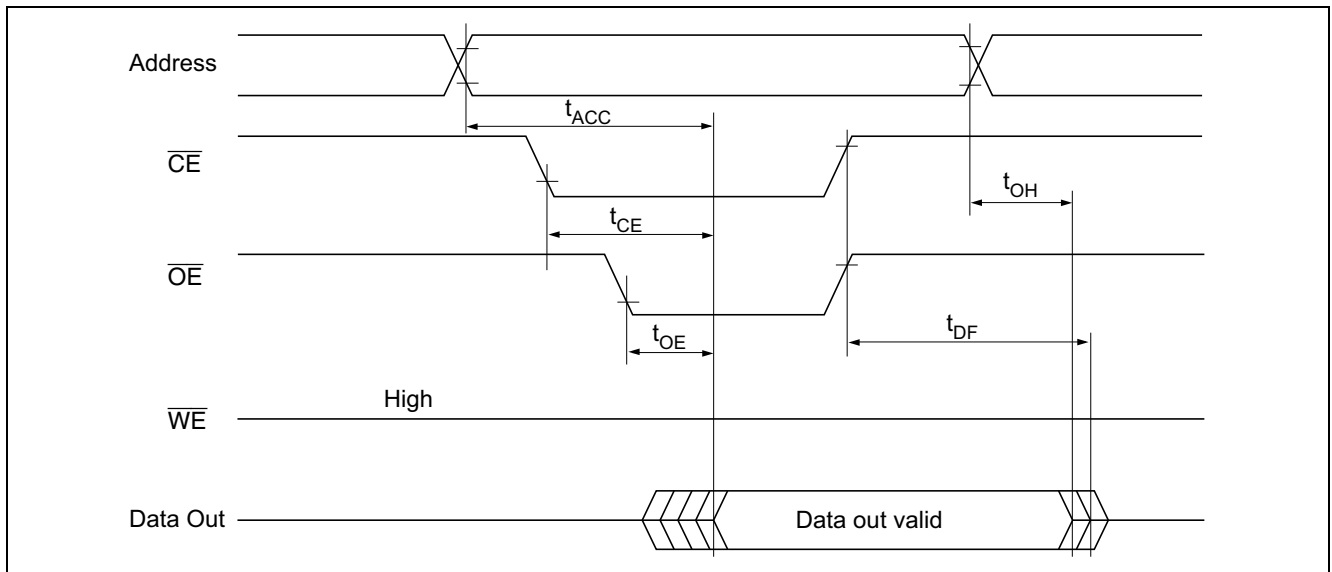
| Parameter | Symbol | Min* ² | Typ | Max | Unit | Test conditions |
|---|------------------|-------------------|-----|------------------|------|-----------------|
| Address setup time | t _{AS} | 0 | — | — | ns | |
| Address hold time | t _{AH} | 50 | — | — | ns | |
| \overline{CE} to write setup time (\overline{WE} controlled) | t _{CS} | 0 | — | — | ns | |
| \overline{CE} hold time (\overline{WE} controlled) | t _{CH} | 0 | — | — | ns | |
| \overline{WE} to write setup time (\overline{CE} controlled) | t _{WS} | 0 | — | — | ns | |
| \overline{WE} hold time (\overline{CE} controlled) | t _{WH} | 0 | — | — | ns | |
| \overline{OE} to write setup time | t _{OES} | 0 | — | — | ns | |
| \overline{OE} hold time | t _{OEH} | 0 | — | — | ns | |
| Data setup time | t _{DS} | 50 | — | — | ns | |
| Data hold time | t _{DH} | 0 | — | — | ns | |
| \overline{WE} pulse width (\overline{WE} controlled) | t _{WP} | 100 | — | — | ns | |
| \overline{CE} pulse width (\overline{CE} controlled) | t _{CW} | 100 | — | — | ns | |
| Data latch time | t _{DL} | 50 | — | — | ns | |
| Byte load cycle | t _{BLC} | 0.2 | — | 30 | μs | |
| Byte load window | t _{BL} | 100 | — | — | μs | |
| Write cycle time | t _{WC} | — | — | 10* ³ | ms | |
| Time to device busy | t _{DB} | 120 | — | — | ns | |
| Write start time | t _{DW} | 0* ⁴ | — | — | ns | |

Notes: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

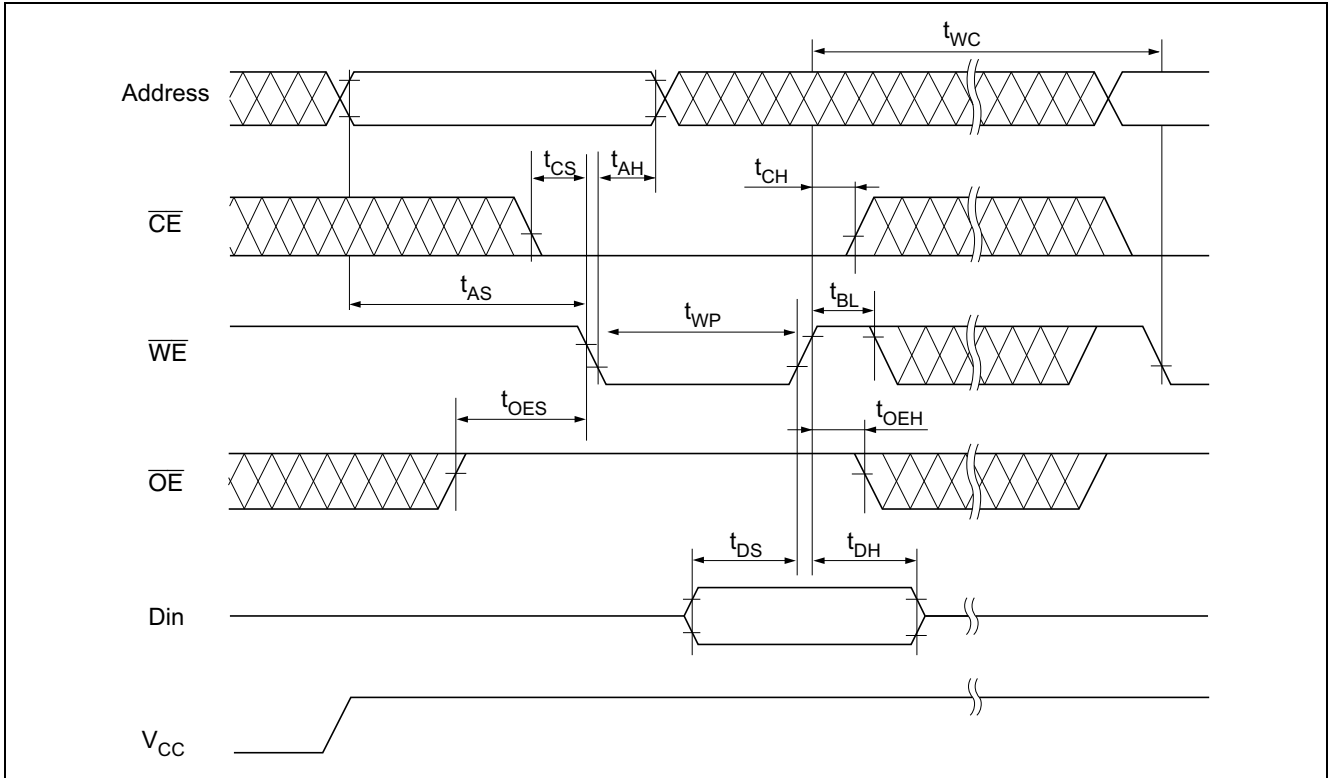
2. Use this device in longer cycle than this value.
3. t_{WC} must be longer than this value unless polling techniques are used. This device automatically completes the internal write operation within this value.
4. Next read or write operation can be initiated after t_{DW} if polling techniques are used.
5. A6 through A14 are page address and these addresses are latched at the first falling edge of \overline{WE} .
6. A6 through A14 are page address and these addresses are latched at the first falling edge of \overline{CE} .
7. See AC read characteristics.

Timing Waveforms

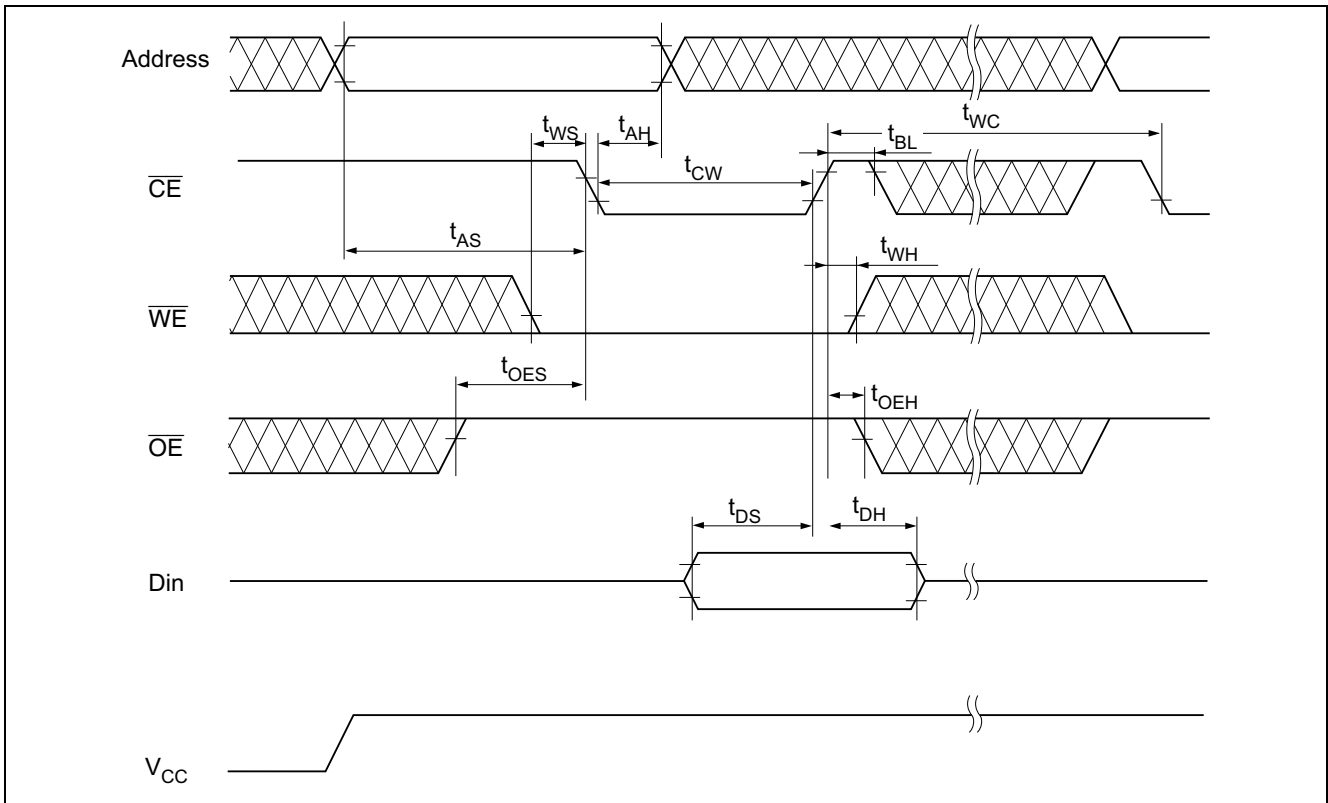
Read Timing Waveform



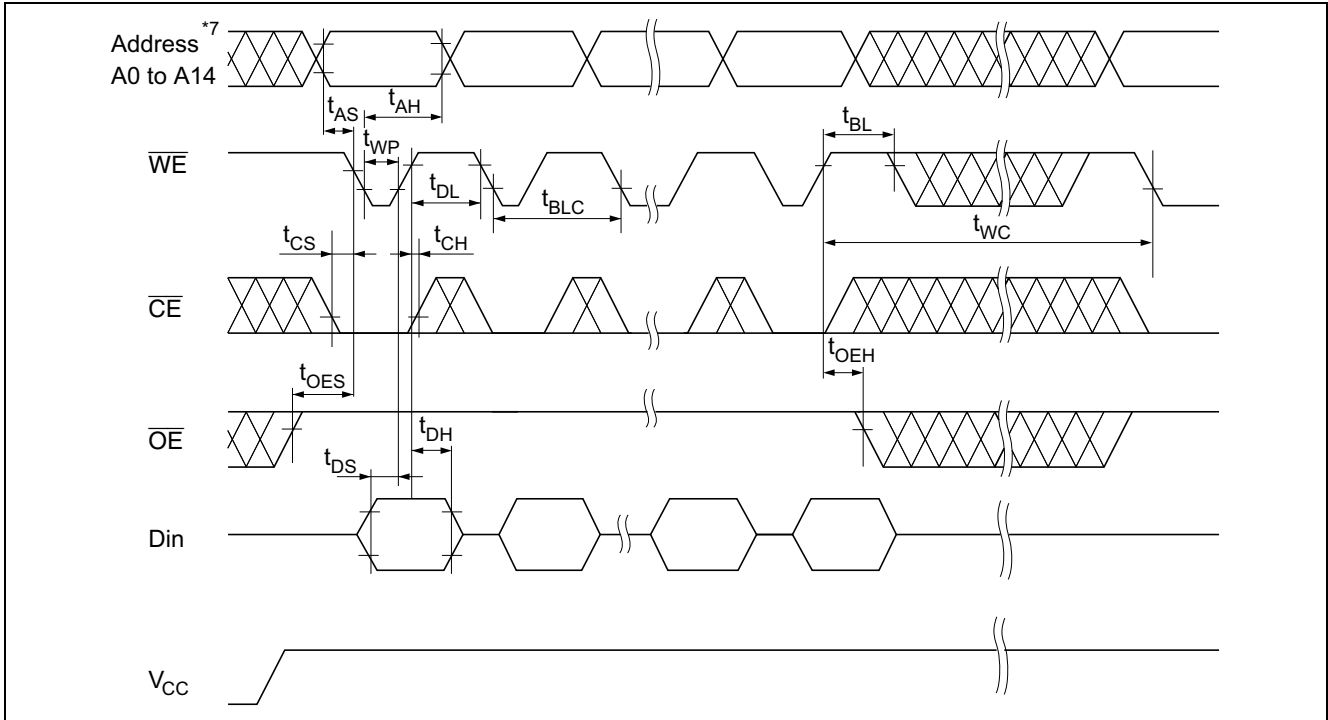
Byte Write Timing Waveform (1) (\overline{WE} Controlled)



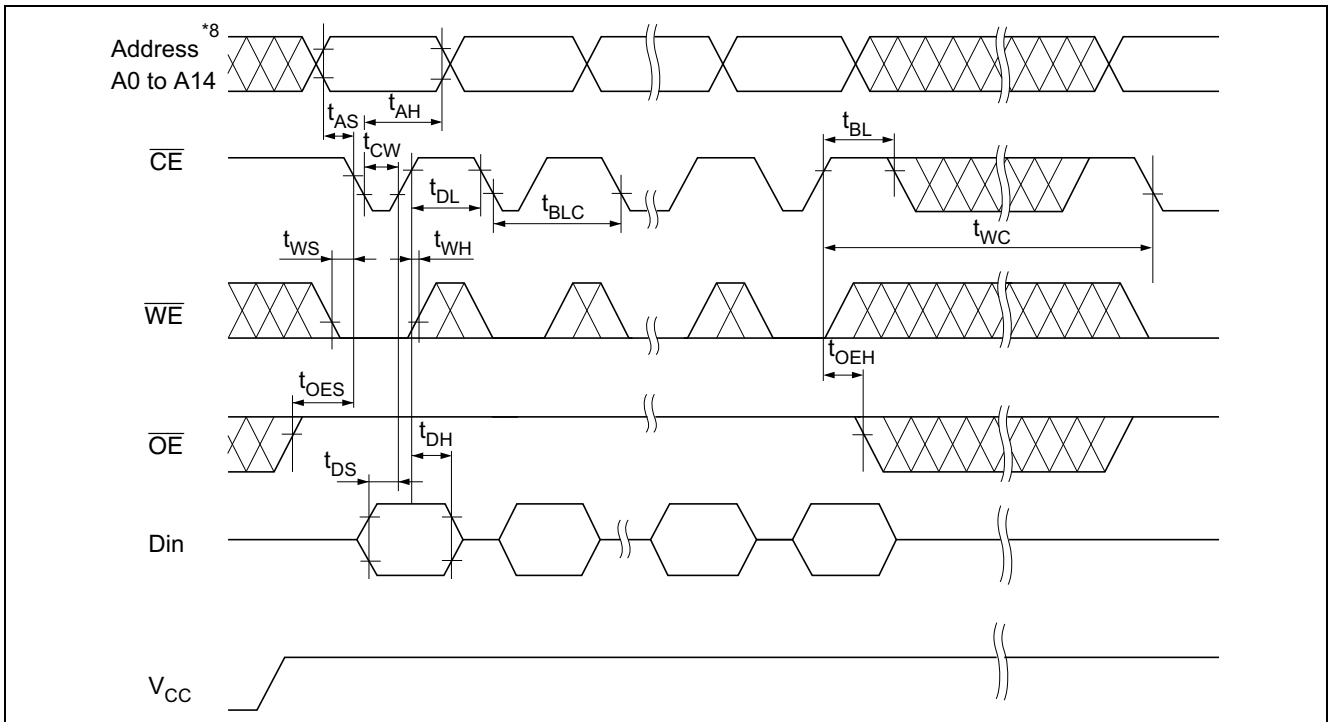
Byte Write Timing Waveform (2) (\overline{CE} Controlled)



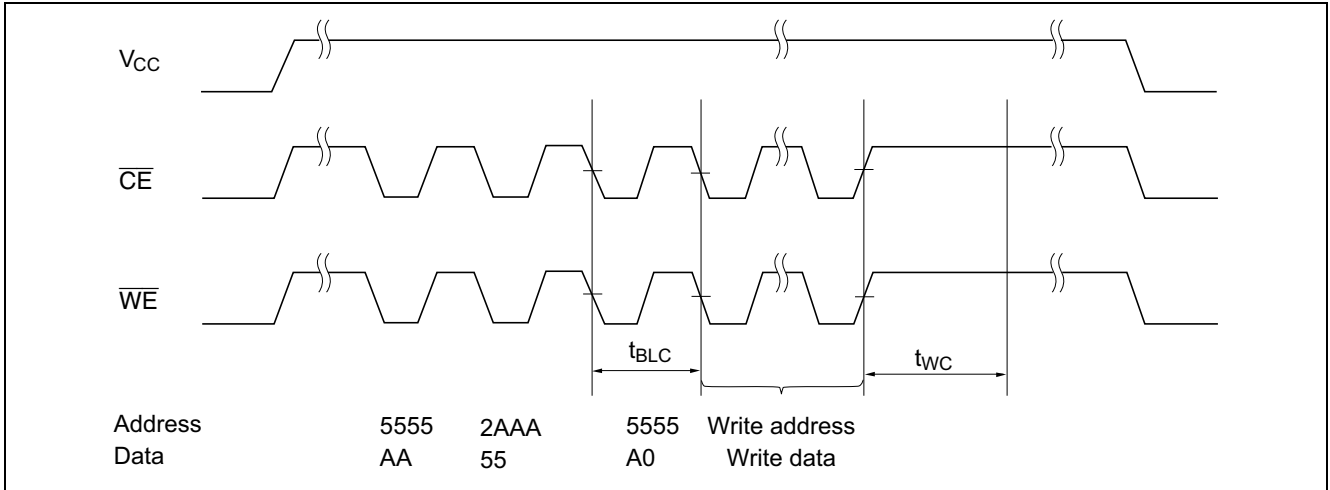
Page Write Timing Waveform (1) (\overline{WE} Controlled)



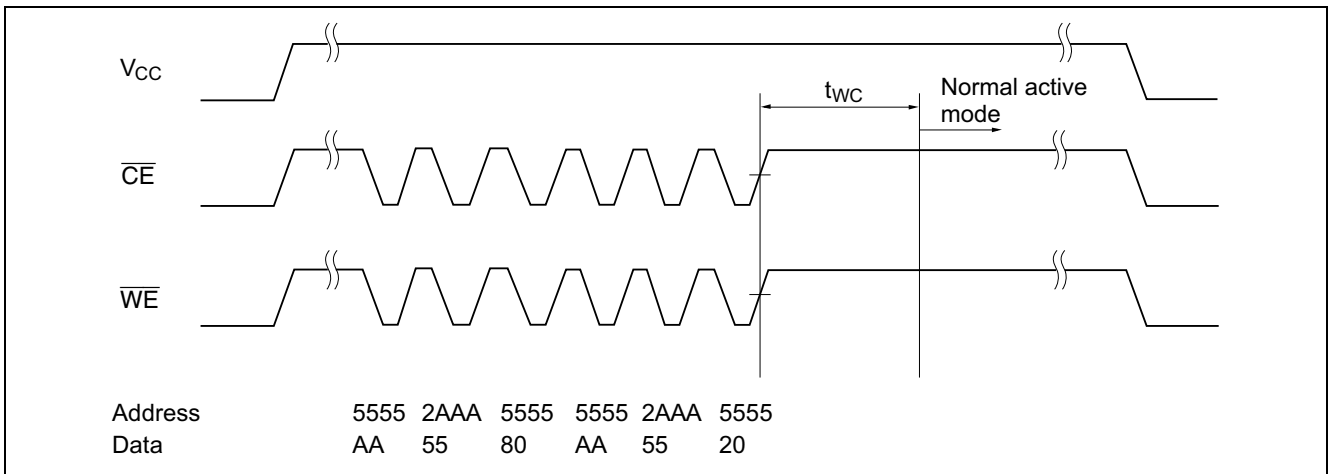
Page Write Timing Waveform (2) (\overline{CE} Controlled)



Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 μ s from the preceding falling edge of \overline{WE} or \overline{CE} . When \overline{CE} or \overline{WE} is high for 100 μ s after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

Data Polling

Data polling indicates the status that the EEPROM is in a write cycle or not. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data outputs from I/O7 to indicate that the EEPROM is performing a write operation.

\overline{WE} , \overline{CE} Pin Operation

During a write cycle, addresses are latched by the falling edge of \overline{WE} or \overline{CE} , and data is latched by the rising edge of \overline{WE} or \overline{CE} .

Write/Erase Endurance and Data Retention Time

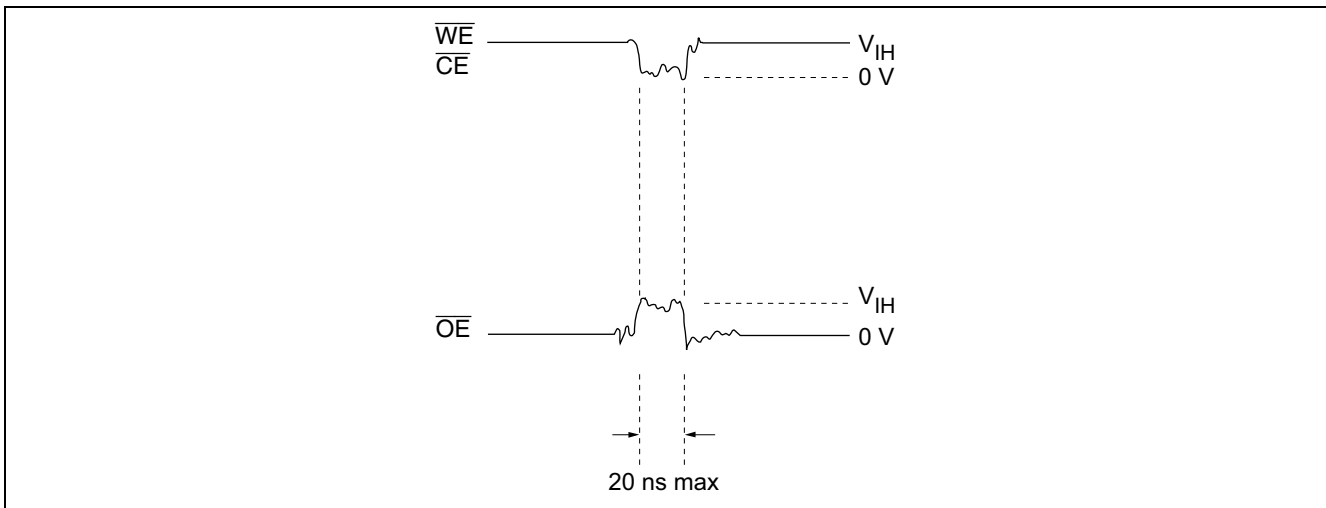
The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less.

1. Data Protection against Noise on Control Pins (\overline{CE} , \overline{OE} , \overline{WE}) during Operation

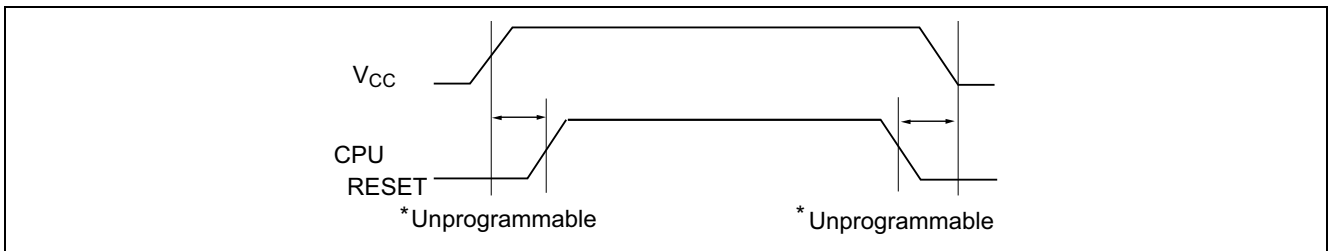
During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

Note: The EEPROM should be kept in unprogrammable state during VCC on/off by using CPU RESET signal.



2.1 Protection by \overline{CE} , \overline{OE} , \overline{WE}

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

| | | | |
|-----------------|-----------------|-----------------|-----------------|
| \overline{CE} | V _{CC} | × | × |
| \overline{OE} | × | V _{SS} | × |
| \overline{WE} | × | × | V _{CC} |

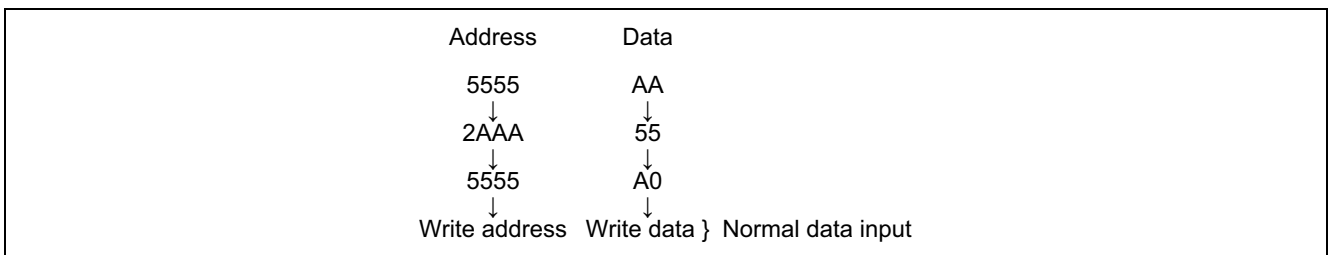
×: Don't care

V_{CC}: Pull-up to VCC level

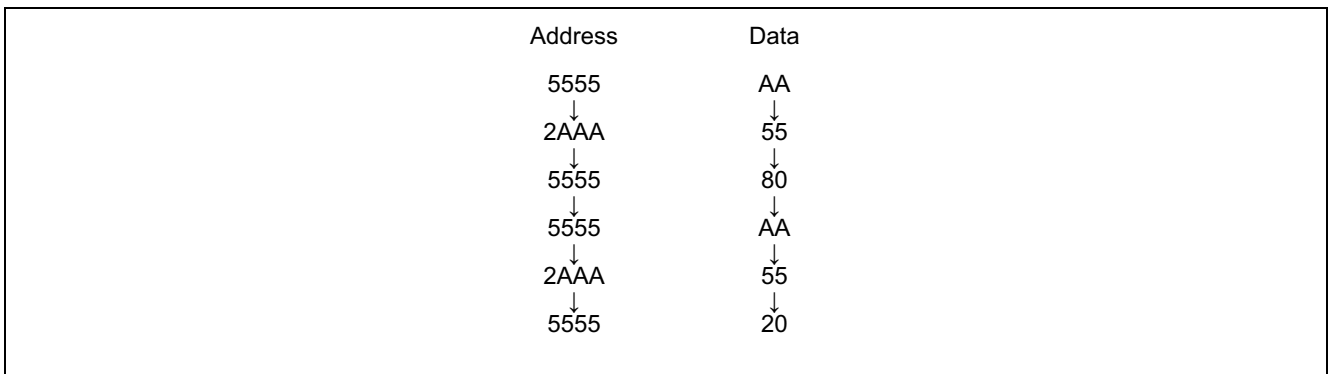
V_{SS}: Pull-down to VSS level

3. Software data protection

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the following 3 bytes code and write data. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data.



The SDP mode is disabled by inputting the following 6 bytes code. Note that, if data is input in the SDP disable cycle, data can not be written.

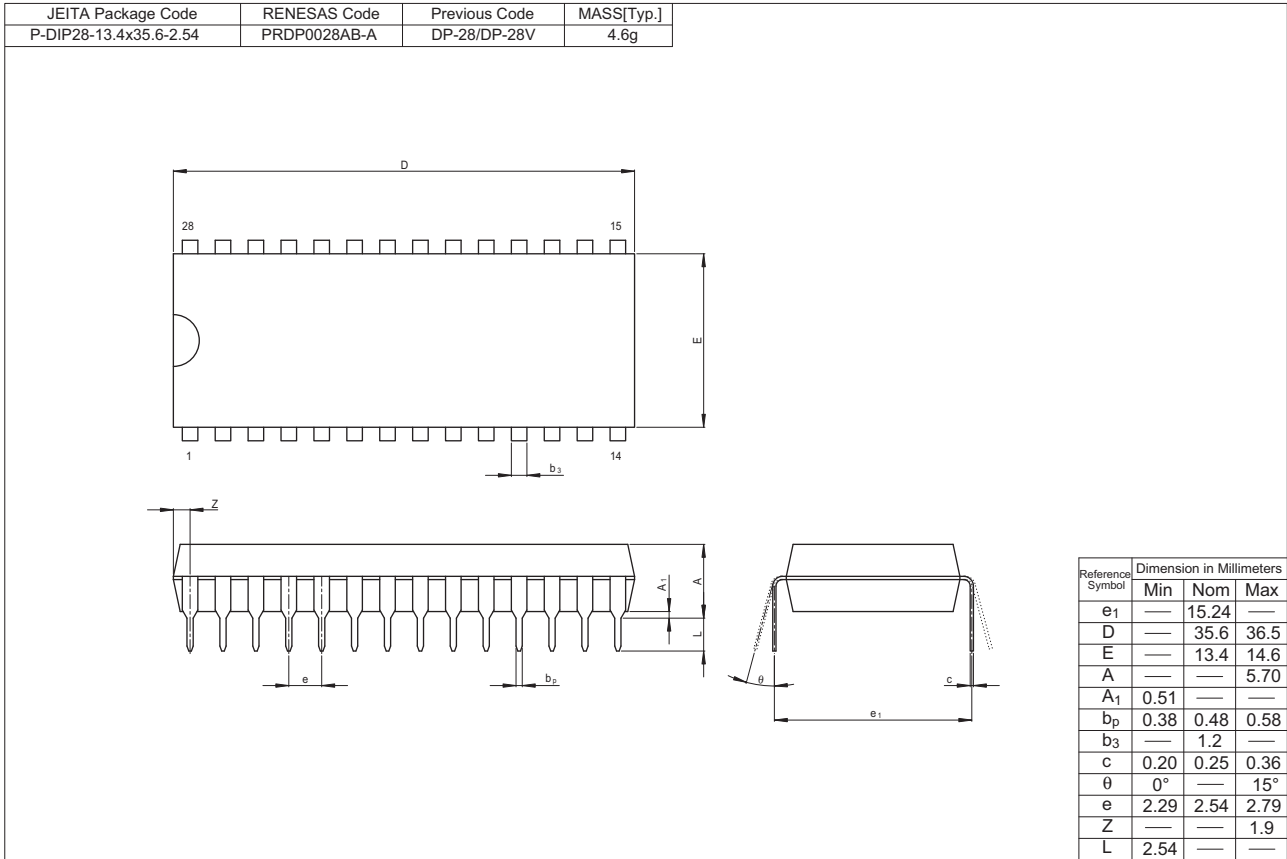


The software data protection is not enabled at the shipment.

Note: There are some differences between Renesas Electronics' and other company's for enable/disable sequence of software data protection. If there are any questions, please contact with Renesas Electronics' sales offices.

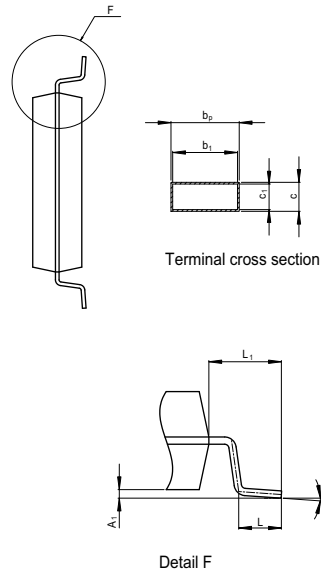
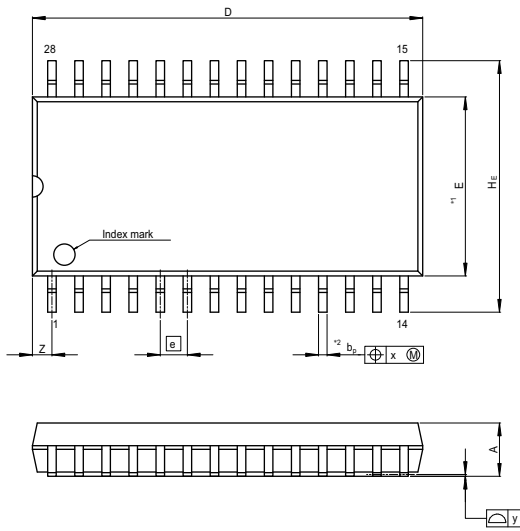
Package Dimensions

HN58C256API Series (PRDP0028AB-A / Previous Code: DP-28V)



HN58C256AFPI Series (PRSP0028DC-A / Previous Code: FP-28DV)

| | | | |
|-----------------------|--------------|---------------|------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
| P-SOP28-8.4x18.3-1.27 | PRSP0028DC-A | FP-28D | 0.7g |



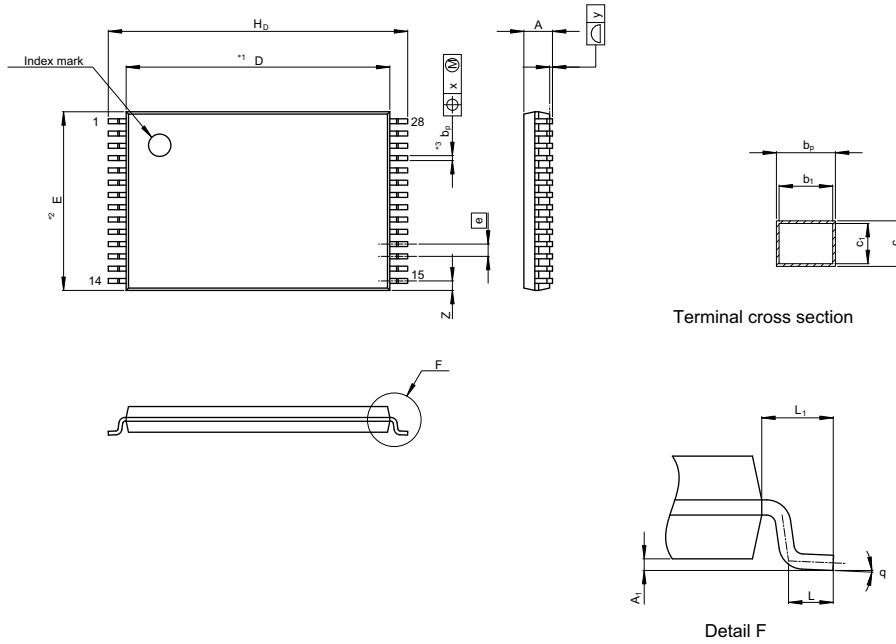
NOTE)
 1. DIMENSION*1* DOES NOT INCLUDE MOLD FLASH.
 2. DIMENSION*2* DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|------|------|
| | Min | Nom | Max |
| D | — | 18.3 | 18.8 |
| E | — | 8.4 | — |
| A ₂ | — | — | — |
| A ₁ | 0.10 | 0.20 | 0.30 |
| A | — | — | 2.50 |
| b _D | 0.32 | 0.40 | 0.48 |
| b ₁ | — | 0.38 | — |
| c | 0.12 | 0.17 | 0.22 |
| c ₁ | — | 0.15 | — |
| θ | 0° | — | 8° |
| H _E | 11.5 | 11.8 | 12.1 |
| Ⓜ | — | 1.27 | — |
| x | — | — | 0.20 |
| y | — | — | 0.15 |
| Z | — | — | 1.12 |
| L | 0.8 | 1.0 | 1.2 |
| L ₁ | — | 1.7 | — |

HN58C256ATI Series (PTSA0028ZB-A / Previous Code: TFP-28DBV)

| | | | |
|-------------------------|--------------|--------------------|------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
| P-TSOP(1)28-8x11.8-0.55 | PTSA0028ZB-A | TFP-28DB/TFP-28DBV | 0.23g |

NOTE)
 1. DIMENSION**1*AND**2*(Nom)
 DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION**3*DOES NOT
 INCLUDE TRIM OFFSET.



| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|-------|-------|
| | Min | Nom | Max |
| D | — | 11.80 | — |
| E | — | 8.00 | 8.20 |
| A ₂ | — | — | — |
| A ₁ | 0.05 | 0.13 | 0.20 |
| A | — | — | 1.20 |
| b _p | 0.14 | 0.22 | 0.30 |
| b ₁ | — | 0.20 | — |
| c | 0.12 | 0.17 | 0.22 |
| c ₁ | — | 0.15 | — |
| θ | 0° | — | 5° |
| H _D | 13.10 | 13.40 | 13.70 |
| ⓐ | — | 0.55 | — |
| x | — | — | 0.10 |
| y | — | — | 0.10 |
| z | — | — | 0.45 |
| L | 0.40 | 0.50 | 0.60 |
| L ₁ | — | 0.80 | — |

| | |
|-------------------------|-------------------------------------|
| Revision History | HN58C256AI Series Data Sheet |
|-------------------------|-------------------------------------|

| Rev. | Date | Description | |
|----------|--------------|-------------|---------------|
| | | Page | Summary |
| Rev.1.00 | Oct 07, 2013 | — | Initial issue |
| | | | |

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