SGS-THOMSON MICROELECTRONICS

M54HC182
M74HC182

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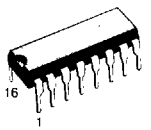
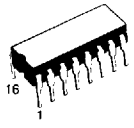
T-49-11-00

FUNCTION LOOK AHEAD CARRY GENERATOR

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (Max.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  with 54/74LS182



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HC182 F1
M74HC182 B1N
M74HC182 F1
M74HC182 M1
M74HC182 C1

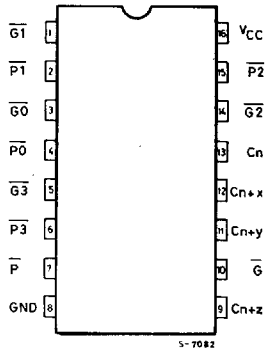
DESCRIPTION

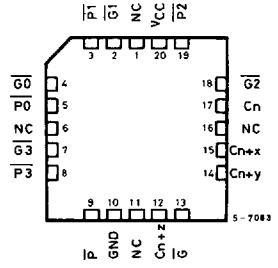
The M54/74HC182 is a high speed CMOS FUNCTION LOOK AHEAD CARRY GENERATOR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These circuit are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin connection table.

When used in conjunction with the HC181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretation of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION (top view)





NC = No Internal Connection

FUNCTION TABLES

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
ALL OTHER COMBINATIONS							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
ALL OTHER COMBINATIONS				H

FOR Cn+z OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+z
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
ALL OTHER COMBINATIONS							L

FOR Cn+x OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	Cn+x
L	X	X	H
X	L	H	H
ALL OTHER COMBINATIONS			L

FOR Cn+y OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+y
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
ALL OTHER COMBINATIONS					L

$$Cn+x = G0 + P0Cn$$

$$Cn+y = G1 + P1G0 + P1P0Cn$$

$$Cn+z = G2 + P2G1 + P2P1G0 + P2P1P0Cn$$

$$\overline{G} = G3 + P3G2 + P3P2G1 + P3P2P1G0$$

$$\overline{P} = P3P2P1P0$$

or

$$\overline{Cn+x} = \overline{Y0\,(X0 + Cn)}$$

$$\overline{Cn+y} = \overline{Y1\,[X1 + Y0(X0 + Cn)]}$$

$$\overline{Cn+z} = \overline{Y2\,\{X2 + Y1[X1 + Y0(X0 + Cn)]\}}$$

$$Y = Y3\,(X3 + Y2)\,(X3 + X2 + Y1)\,(X3 + X2 + X1 + Y0)$$

$$X = X3 + X2 + X1 + X0$$

LOGIC DIAGRAM

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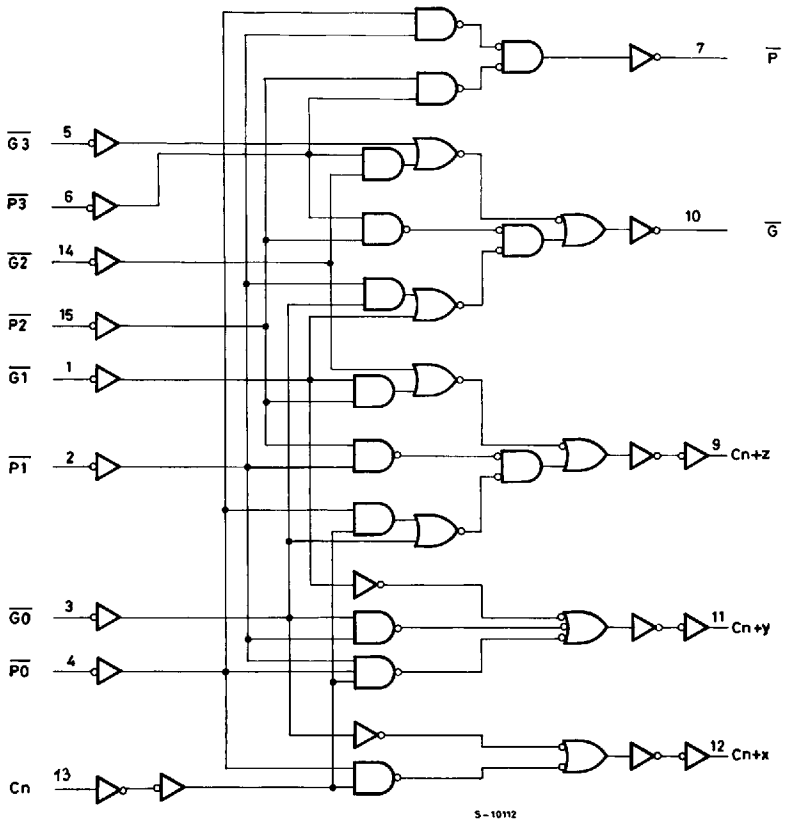

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) **500 mW**: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	−40 to 85 −55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V: 0 to 1000 V_{CC} = 4.5V: 0 to 500 V_{CC} = 6 V: 0 to 400	ns

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

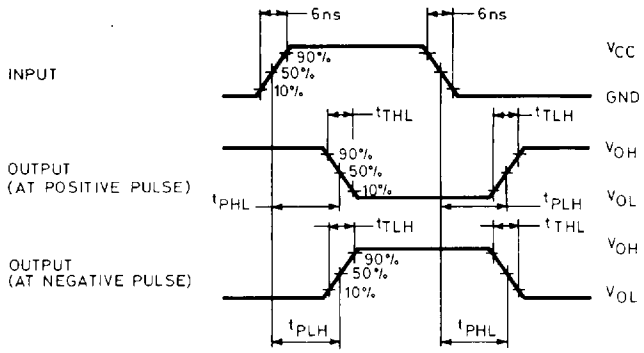
Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2}$, $\overline{P0},\overline{P1},\overline{P2}$ - Cn+x, Cn+y / Cn+Z)		15	25	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2},\overline{G3}$ / $\overline{P1},\overline{P2},\overline{P3}$ - $\overline{G}$)		18	28	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{P0},\overline{P1},\overline{P2},\overline{P3}$ - $\overline{P}$)		17	27	ns
t_{PLH} t_{PHL}	Propagation Delay Time Cu-Cn+x, Cn+y, Cn+z)		16	26	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95		110	ns
		4.5		—	8	15	—	19		22	
		6.0		—	7	13	—	16		19	
t_{PLH}	Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2}$, $\overline{P0},\overline{P1},\overline{P2}$ - Cn+x,Cn+y / Cn+2)	2.0		—	72	145	—	180		220	
		4.5		—	18	29	—	36	—	44	
		6.0		—	15	25	—	31	—	38	
t_{PLH}	Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2},\overline{G3}$, $\overline{P0},\overline{P1},\overline{P2}$ - $\overline{G}$)	2.0		—	84	165	—	205		250	
		4.5		—	21	33	—	41	—	50	
		6.0		—	18	28	—	35	—	43	
t_{PLH}	Propagation Delay Time ($\overline{P0},\overline{P1},\overline{P2},\overline{P3}$ - $\overline{P}$)	2.0		—	80	155	—	195		235	
		4.5		—	20	31	—	39	—	47	
		6.0		—	17	26	—	33	—	40	
t_{PHL}	Propagation Delay Time (Cu-Cn+x, Cn+y,Cn+z)	2.0		—	76	150	—	190		225	
		4.5		—	19	30	—	38	—	45	
		6.0		—	16	26	—	33	—	38	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD}(*)	Power Dissipation Capacitance			—	88	—	—	—	—	—	

ote (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current is: $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



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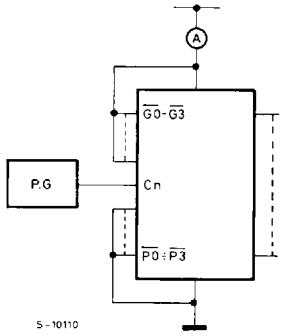
TEST CIRCUIT I_{CC} (Opr.)



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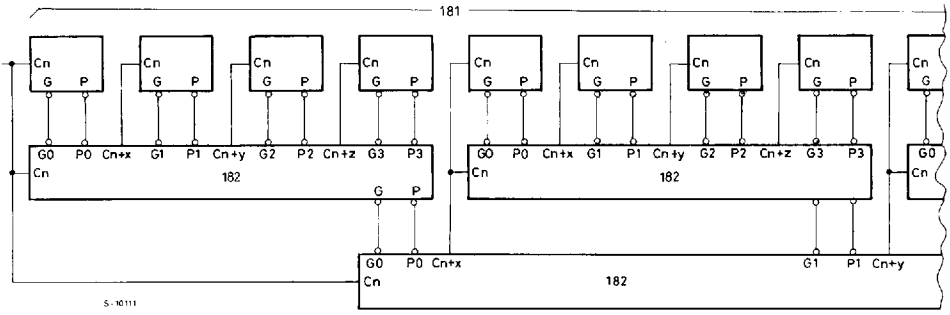
INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TYPICAL APPLICATION



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64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS