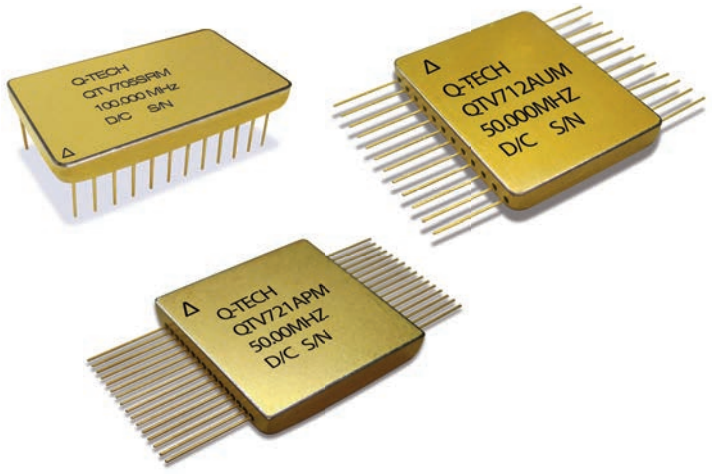
Description

Q-Tech QTV700 Series Space Qualified, 100kRad(Si) Tolerant Hybrid Oscillators are Class 2 Hybrids per MIL-PRF-55310. These CMOS and Sine Wave VCXOs are hermetically sealed in a 24 pin Double Dual In-Line, 24 pin Flat-Pack .975" x 1.275", or 32 pin Flat-Pack 1" SQR, and operate over a variety of voltages and temperature ranges.



Features

- Made in USA
- Hermetically sealed packages
- Supply voltage 3.3Vdc, 5.0Vdc, 12.0Vdc, and 15.0Vdc
- Temperature range -55°C to +125°C
- Screened and Quality Conformance Inspection to MIL-PRF-55310
- CMOS & Sine Wave outputs
- 100k(Si) Radiation tolerant
- Low phase noise and jitter
- NEW: Low Noise option for even lower phase noise on our Sine Wave output VCXOs.

Packaging Options

- Standard ESD packaging

EAR Destination Control Statement

This product and related technical data are subject to the EAR as promulgated and implemented by the U.S. Department of Commerce Bureau of Industry and Security. This product and related technical data are controlled under Export Control Classification Number (ECCN) 9A515.e.1 of the Commerce Control List (CCL), and may not be exported, re-exported, or re-transferred outside of the U.S. or released or disclosed to Foreign Persons, as defined by the EAR, without first complying with all applicable U.S. Export Regulations.

Ordering Information

(Sample part number)

QTV 701 ARM - 50.00MHz

QTV	7	0	1	A	R	M	-	50.000MHz

Package (*)

0	=	24 Pin Double DIP
1	=	24 Pin Flatpack
2	=	32 Pin Flatpack

Output & Supply Voltage

1	=	CMOS at 5V
2	=	CMOS at 3.3V
4	=	Sine at 5V (0 dBm)
5	=	Sine at 12V (+7 dBm)
6	=	Sine at 15V (+7 dBm)

Duty Cycle (CMOS Only)

A	=	60/40%
T	=	45/55%

Phase Noise (Sine Only)

S	=	Standard Noise
L	=	Low Noise

Frequency (**)

2MHz to 350MHz

Level

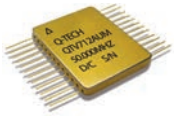
B	=	Breadboard Model
E	=	Engineering Model
M	=	Flight Model

Stability/Temperature Options (**)

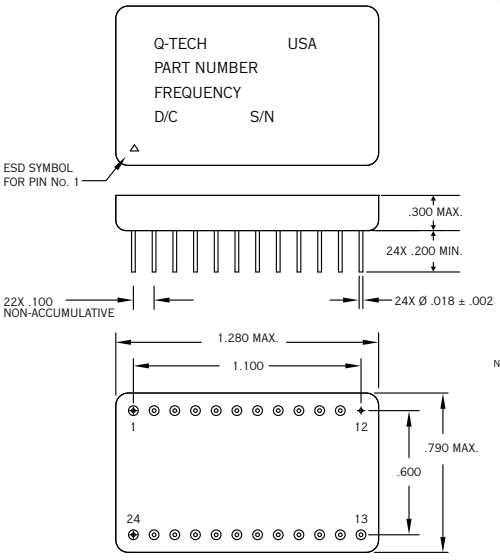
	Temperature Range	Max. Overall Stability	Min. Frequency Pulling	Vcontrol Range
N =	0 to +50ºC	±25 ppm	±50 ppm	0.5 to 6.0V
P =	0 to +70ºC	±35 ppm	±70 ppm	0.5 to 6.0V
Q =	-20 to +70ºC	±40 ppm	±80 ppm	0.5 to 6.0V
R =	-40 to +85ºC	±45 ppm	±90 ppm	0.5 to 6.0V
U =	-55 to +125ºC	±65 ppm	±130 ppm	0.5 to 6.0V

(*) See Page 2 for packages and output logic frequency ranges.

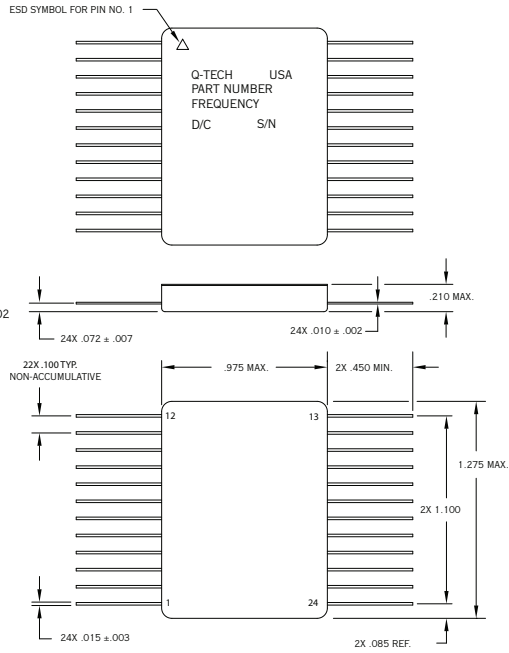
(**) Variations from standard specification are available, please contact factory. Consult factory for stability and pulling options for low noise option L.

Photo	Package	Product QT	Output Logic	Vdd (V)	Frequency Range
	Double Dual In-Line (24 Pin)	QTV701 QTV702 QTV704 QTV705 QTV706	CMOS CMOS Sine Sine Sine	5V 3.3V 5V 12V 15V	2MHz to 90MHz 2MHz to 90MHz 10MHz to 150MHz 10MHz to 150MHz 10MHz to 150MHz
	Flat Pack (24 Pin)	QTV711 QTV712 QTV714 QTV715 QTV716	CMOS CMOS Sine Sine Sine	5V 3.3V 5V 12V 15V	2MHz to 90MHz 2MHz to 90MHz 10MHz to 350MHz 10MHz to 350MHz 10MHz to 350MHz
	Flat Pack (32 Pin)	QTV721 QTV722 QTV724 QTV725 QTV726	CMOS CMOS Sine Sine Sine	5V 3.3V 5V 12V 15V	2MHz to 90MHz 2MHz to 90MHz 10MHz to 350MHz 10MHz to 350MHz 10MHz to 350MHz

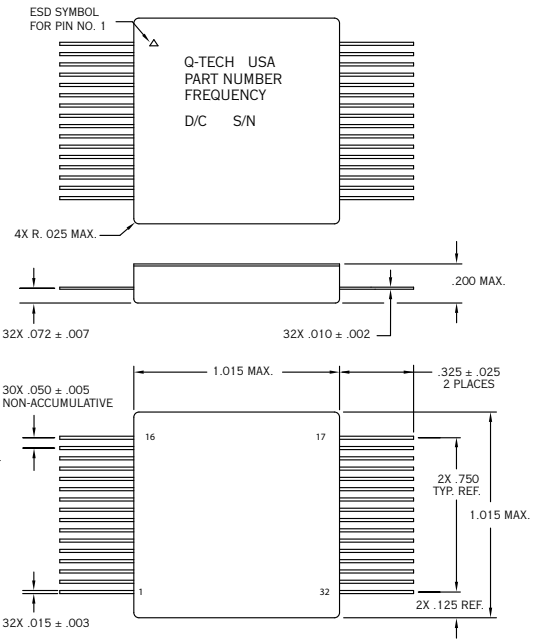
Double Dual In-Line



Flat Pack (24 Pin)



Flat Pack (32 Pin)



Package Dimensions are in Inches

Pin No.	Designation
1	Voltage Control
2 - 11	NC
12	GND/Case
13	RF Output
14 - 23	NC
24	Supply Voltage

Pin No.	Designation
1	Voltage Control
2 - 11	NC
12	GND/Case
13	RF Output
14 - 23	NC
24	Supply Voltage

Pin No.	Designation
1 - 3	NC
4	Voltage Control
5	GND/Case
6 - 10	NC
11	Supply Voltage
12	RF Output
13	Supply Voltage
14 - 32	NC

1 **PURPOSE**

1.1 The purpose of this Detail Specification Control Drawing (SCD) is to describe the specific quality and reliability requirements for a voltage controlled crystal oscillator (VCXO).

2 **SCOPE**

2.1 This specification establishes the minimum detail requirements for a low profile hybrid, hermetically sealed, Type 2, Class 2 (reference MIL-PRF-55310) VCXO.

3 **PART PROTECTION AND SAFETY**

3.1 These items are susceptible to breakdown damage resulting from electrostatic discharge. Every precaution shall be taken while handling, installing, and testing the parts to prevent static charge. Care should be exercised to not apply more than rated voltage or current to any terminal/pad during testing.

4 **PART NUMBER**

4.1 The Q-Tech Part Number shall be as specified in Ordering Information (Page 1).

5 **APPLICABLE DOCUMENTATION & REFERENCES**

5.1 The following documents form a part of this drawing to the extent specified or modified herein.

5.2 **Military & Industry**

5.2.1 MIL-PRF-55310, Oscillator, Crystal Controlled, General Specification for

5.2.2 MIL-PRF-38534, Microcircuit Manufacturing, General Specification for

5.2.3 MIL-PRF-38535, Integrated Circuits, (Microcircuits) Manufacturing, General Specification for

5.2.4 MIL-PRF-19500, Semiconductor Devices, General Specification for

5.2.5 MIL-STD-202, Test Methods for Electronic and Electrical Component Parts

5.2.6 MIL-STD-883, Test Methods and Procedures for Microelectronics

5.2.7 MIL-STD-1686, Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment

5.3 **Q-Tech**

5.3.1 Form F1221, Definitions for Hybrid Product Development Levels

5.4 **Application of Documents**

5.4.1 **Issue of Documents**

Document revisions in effect on the date of the customer purchase order form a part of this drawing except as modified herein.

5.4.2 **Order of Precedence**

In the event of conflict between this document and the references cited herein or other requirements, the precedence in which requirements shall govern, in descending order, is as follows:

a) Applicable Customer Purchase Order
b) Applicable Customer Detail SCD and/or Detail Drawing
c) Applicable Q-Tech Corporation Detail SCD/Drawing
d) Applicable Q-Tech Corporation General SCD
e) Other Specifications, Standards, and Documentation Referenced Above

5.4.3 **Customer Purchase Order Special Requirements**

Additional special requirements shall be specified in the applicable customer purchase order when additional requirements or modifications are needed for compliance to special programs or product line compliance. Unique identification of the items produced may be required.

5.4.4 **General Specification Control Drawing**

Any reference to the “general specification” or “general SCD” refers to the Q-Tech Corporation General Specification Control Drawing cited in the Applicable Documentation and References section, unless otherwise specified.

6 **REQUIREMENTS**

6.1 **General Definition**

The VCXO is a high reliability signal generator that provides a sine-wave or CMOS output. The VCXO has been designed to operate in a spaceflight environment with an expected lifetime in excess of 15 years. Life time is defined as the sum of operational and storage environments

6.2 **Electrical Characteristics**

The electrical characteristics shall be as specified in Table II and Table III.

6.3 **Absolute Maximum Rating**

The absolute maximum ratings shall be as specified in Table I.

6.4 **Physical Characteristics**

6.4.1 **Dimensions**

The VCXO outline dimensions and terminal connections shall be as shown on Page 2.

6.4.2 **Weight**

The VCXO shall weigh less than or equal to 25 grams.

6.4.3 **Materials**

The VCXO package body and lead finish shall be gold in accordance with MIL-PRF-38534.

6.5 **Design and Construction**

The design and construction of the crystal oscillator shall be as specified herein. As a minimum, the oscillators shall meet the design and construction requirements of MIL-PRF-55310, except element evaluation shall be as specified in 6.5.

6.5.1 All piece parts shall be derived from lots that meet the element evaluation requirements of MIL-PRF-38534, Class K, with the following exceptions:

6.5.1.1 Active elements

a) Visual Inspection of Silicon on Sapphire Microcircuits

Semicircular crack(s) or multiple adjacent cracks, not in the active area, starting and terminating at the edge of the die are acceptable. Attached (chip in place) sapphire is nonconductive material and shall not be considered as foreign material and will be considered as nonconductive material for all inspection criteria.

b) Subgroup 4, Scanning Electron Microscope (SEM) Inspection

The manufacturer may allow the die distributor, at his option, to select two (2) dice from a waffle pack (containing a maximum quantity of 100 die), visually inspect for the worst case metallization of the 2 dice, and take SEM photographs of the worst case.

c) Subgroup 5 Radiation Tests

Subgroup 5 radiation tests are not required unless otherwise specified in the detail purchase order.

6.5.2 **Processes**

Processes used for manufacturing the VCXO are selected on the basis of their ability to meet the quality requirements for space High Reliability manufacturing. Travelers or Process Cards are used in the manufacturing and testing of all of the VCXO Series, and might be available for customer review. Copies of these Travelers can be provided with the VCXOs at time of shipment if so specified on the purchase order.

6.5.3 **Interchangeability**

Each VCXO shall be interchangeable without using a special selection process.

6.5.4 **Product Marking**

Each unit shall be permanently marked with the manufacturer's name or symbol, part number, lot date code number, and serial number. The unit shall be marked with the outline of an equilateral triangle near pin 1 to show that it contains devices which are sensitive to electrostatic discharge.

6.6 **Parts Program**

Devices delivered to this specification represent the standardized Parts, Materials and Processes (PMP) Program developed, implemented and certified for advanced applications and extended environments.

6.6.1 **Quartz Crystal Resonator**

The crystal resonator used shall be constructed using a 4-point mount premium synthetic swept Quartz and procured to Q-TECH SCD. (For the Breadboard and Engineering models, non-swept quartz may be used. See Q-Tech Form F1221, Definitions for Hybrid Product Development Levels).

6.6.2 **Sine-Wave Active Devices**

Radiation testing is not performed at the oscillator level, but these VCXOs have been acceptable for use in environments up to 100k rads by analysis of the components used. ONLY Bipolar semiconductors are employed in the design. This device is specified to be radiation tolerant to 100 kRad(Si) total ionizing dose (TID).

6.6.3 **CMOS Active Devices**

Radiation testing is not performed at the oscillator level, but these VCXOs have been acceptable for use in environments up to 100k Rads by analysis of the components used. This device is specified to be radiation tolerant to 100 kRad(Si) total ionizing dose (TID). The microcircuit in this part shall use CMOS technology and shall be from a wafer proven to be radiation tolerant to 100kRad(Si) total ionizing dose.

6.6.3.1 **CMOS Microcircuit Usage**

For output frequencies below 14MHz, the output microcircuit shall be 54AC74, see DSCC SMD 5962-88520. For frequencies greater than or equal to 14MHz, the CMOS microcircuit shall be 54AC00, see DSCC SMD 5962-87549. These microcircuits are specified to be Single Event Latchup Free for LET up to 93 MeV-cm^2/mg. For QTV702, QTV712, and QTV722 devices above 70MHz, the manufacturer shall be National Semiconductor Corporation, otherwise the manufacturer shall be ST Microelectronics Corporation.

6.6.4 **Prohibited Materials**

Materials containing more than 97% tin and materials containing measurable amounts (by common nondestructive test methods) of selenium, cadmium, or mercury shall not be used as plating, coating or base materials in the construction of parts or components. Zinc is only acceptable as an alloying element and alloys containing zinc must be covered by suitable protective plating (e.g. nickel plating). Inert oxides of the above materials are allowed.

6.7 **Traceability Requirements**

Material, element and process traceability requirements shall be as specified by MIL-PRF-38534 for Class K hybrids.

6.8 **Data**

6.8.1 **Design Documentation**

When required by the purchase order, design, topography, process and flow charts for all assembly/inspection and test operation for devices to be supplied under this specification on the initial procurement shall be established and shall be available in-plant for review by the procuring activity upon request. This design documentation shall be sufficient to depict the physical and electrical construction of the devices supplied under the specification and shall be traceable to the specific parts, drawings or part type numbers to which it applies, and to the production lot(s) and inspection lot codes under which devices are manufactured and tested so that revisions can be identified.

6.8.2 **Technical Data Package**

When required by the purchase order, the following design documentation and information is deliverable 30 days prior to the start of production. The Technical Data Package shall consist of the following:

a) Assembly drawing(s).

b) All electrical schematics and drawings not considered proprietary.

c) The assembly and screening travelers to be used on-line to manufacture the devices supplied to this specification.

d) Parts and materials list.
e) Element evaluation data confirming compliance with MIL-PRF-38534, Class K, and Prohibited Materials paragraph 3.4.3

6.9 **Test Report**

6.9.1 A test report is supplied with each shipment of oscillators and includes the following information, as a minimum:
a) A Certificate of Conformance to all specifications and purchase order requirements. As a minimum, the Certificate of Conformance shall include the following information:
1) Purchase order number.
2) Applicable part number.
3) Manufacturers lot number.
4) Lot date code.
b) Parts and materials traceability information.
c) Certificate of crystal sweeping.
d) Manufacturing lot traveler.
e) Screening attributes and variables data as applicable.
f) Quality conformance inspection attributes and variables data as applicable.
g) Radiographic inspection negatives.

6.10 **Non-Flight Oscillators**

Unless otherwise specified in data sheet, the general requirements for non-flight hardware (Breadboard and Engineering models) shall be defined in F1221, Definitions for Hybrid Product Development Levels.

6.11 **Screening**

Screening tests shall be in accordance with Table IV.

6.12 **Quality Conformance Inspection (QCI)**

Quality conformance shall be as specified herein. All records shall be traceable to the lot number and unit serial number. Samples used for Group A that pass all tests may be delivered on contract.

6.12.1 **Oscillator Group A Inspection**

Group A testing shall be in accordance with Table V. Group A inspection shall be performed on units that have passed the screening tests. All electrical performance tests of this specification shall be performed during Group A with the exception of any tests performed as part of the final electrical testing during 100 percent screening.

6.12.2 **Oscillator Group B Inspection**

Group B inspection shall be in accordance with Table VI.

6.12.3 **Oscillator Group C Inspection**

Group C inspection shall be in accordance with Table VII.

6.13 **Destructive Physical Analysis (DPA)**

A DPA may be performed on each lot of devices in accordance with MIL-STD-883, Method 5009. The DPA shall be performed by the customer.

TABLE I - MAXIMUM RATINGS

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNITS
Supply Voltage (QTV7X1, 7X2, & 7X4)	Vs	0	6	V
Supply Voltage (QTV7X5 or QTV7X6)	Vs	0	16.5	V
Operating Temperature Range	Tc	-55	+125	ºC
Storage Temperature	Tstg	-65	+125	ºC
Lead Solder Temperature/Time			+250/10	ºC/s
Package Thermal Resistance	θ_{JC}		50	ºC/W

TABLE II - ELECTRICAL PERFORMANCE CHARACTERISTICS (CMOS)

ELECTRICAL PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS			
			MIN.	TYP.	MAX.	UNIT
Frequency, Nominal	fo		3		90	MHz
Supply Voltage, Nominal	Vdd		3.135 4.75	3.3 5	3.465 5.25	V
Input Current	Is	Nominal Vdd, No Load	-	-	50	mA
Frequency/Temperature Stability	Δf/fc (Ta)		See Temp. Codes on Pg. 1			
Frequency Adjustment Range	Δf/fo		See Temp. Codes on Pg. 1			
Frequency/Vdd	Δf/fc (Vdd)	±5 % Vdd @ +25ºC	-	-	±1.2	ppm
Load			-	15	-	pF
Output Voltage, High	VOH		Vcc x 0.9	-	-	V
Output Voltage, Low	VOL		-	-	Vcc x 0.1	V
Output Waveform			SQUARE			
Output Rise Time	Tr	10% to 90% of Vdd	-	-	5	ns
Output Fall Time	Tf	90% to 10% of Vdd	-	-	5	ns
Duty Cycle	DC	Code A Code T	60/40 45/55			%
Frequency/Load Stability	Δf/fc (Load)	Load ±5%, Vdd Nom. @ +25ºC	-	-	±0.3	ppm
Aging, Max. **(Note 1)**	Δf/fo	Over 18 Years	-	-	±4	ppm
Frequency Stability vs. Vacuum	Δf/fo	Guaranteed by Design, Not Tested	-	-	±0.2	ppm
Phase Noise @ Frequency Offset	£ (Δf)	Δf = 10Hz Δf = 100Hz Δf = 1kHz Δf = 10kHz Δf = 100kHz	-	-	-70 -100 -130 -140 -140	dBc/Hz

Note 1: Consult with factory for better Aging performance.

TABLE III - ELECTRICAL PERFORMANCE CHARACTERISTICS (SINE-WAVE)

ELECTRICAL PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS			
			MIN.	TYP.	MAX.	UNIT
Frequency, Nominal	fo		10		350	MHz
Supply Voltage, Nominal	Vdd		4.75 11.4 14.25	5 12 15	5.25 12.6 15.75	V
Input Current, QTV7X4	Is	Nominal Vdd	-	-	55	mA
Input Current, QTV7X5 or 7X6	Is	Nominal Vdd	-	-	30	mA
Frequency/Temperature Stability	Δf/fc (Ta)		See Temp. Codes on Pg. 1			ppm
Frequency Adjustment Range	Δf/fo		See Temp. Codes on Pg. 1			ppm
Frequency/Vdd, QTV7X4	Δf/fc (Vdd)	±5 % Vdd @ +25ºC	-	-	±1.2	ppm
Frequency/Vdd, QTV7X5 or 7X6	Δf/fc (Vdd)	±5 % Vdd @ +25ºC	-	-	±0.6	ppm
Load			47.5	50	52.5	Ω
Frequency/Load Stability	Δf/fc (Load)	Load ±5%, Vdd Nom. @ +25ºC	-	-	±0.3	ppm
Aging, Max. **(Note 1)**	Δf/fo	Over 18 Years			±4	ppm
Frequency Stability vs. Vacuum	Δf/fo	Guaranteed by Design, Not Tested	-	-	±0.2	ppm
Output Level, QTV7X4			0	-	-	dBm
Output Level, QTV7X5 or 7X6			+7	-	-	dBm
Harmonics			-	-	-20	dBc
Sub-Harmonics, Fo > 70MHz			-	-	-20	dBc
Spurious			-	-	-70	dBc
PHASE NOISE	**SYMBOL**	**TEST CONDITIONS**	**(S Option) MAX.**		**(L Option) TYP. (NOTE 2)**	**UNIT**
Phase Noise @ Frequency Offset fo ≤ 75MHz	£ (Δf)	Δf = 10Hz Δf = 100Hz Δf = 1kHz Δf = 10kHz Δf = 100kHz	-80 -110 -135 -155 -155	-	-103 -133 -153 -163 -166	dBc/Hz
Phase Noise @ Frequency Offset 75MHz < fo ≤ 150MHz Note: Uses 2x Multiplication from lower frequency.	£ (Δf)	Δf = 10Hz Δf = 100Hz Δf = 1kHz Δf = 10kHz Δf = 100kHz	-70 -100 -125 -145 -145	-	-96 -126 -146 -156 -159	dBc/Hz
Phase Noise @ Frequency Offset fo > 150MHz Note: Uses 3x Multiplication from lower frequency.	£ (Δf)	Δf = 10Hz Δf = 100Hz Δf = 1kHz Δf = 10kHz Δf = 100kHz	-65 -95 -120 -140 -140	-	-92 -122 -142 -152 -155	dBc/Hz

Note 1: Consult with factory for better Aging performance.
Note 2: Typical phase noise figures for 5V Supply option shall be 2 - 3 dB higher.

TYPICAL PHASE NOISE FOR 50MHZ VCXO (SINE WAVE - OPTION L)

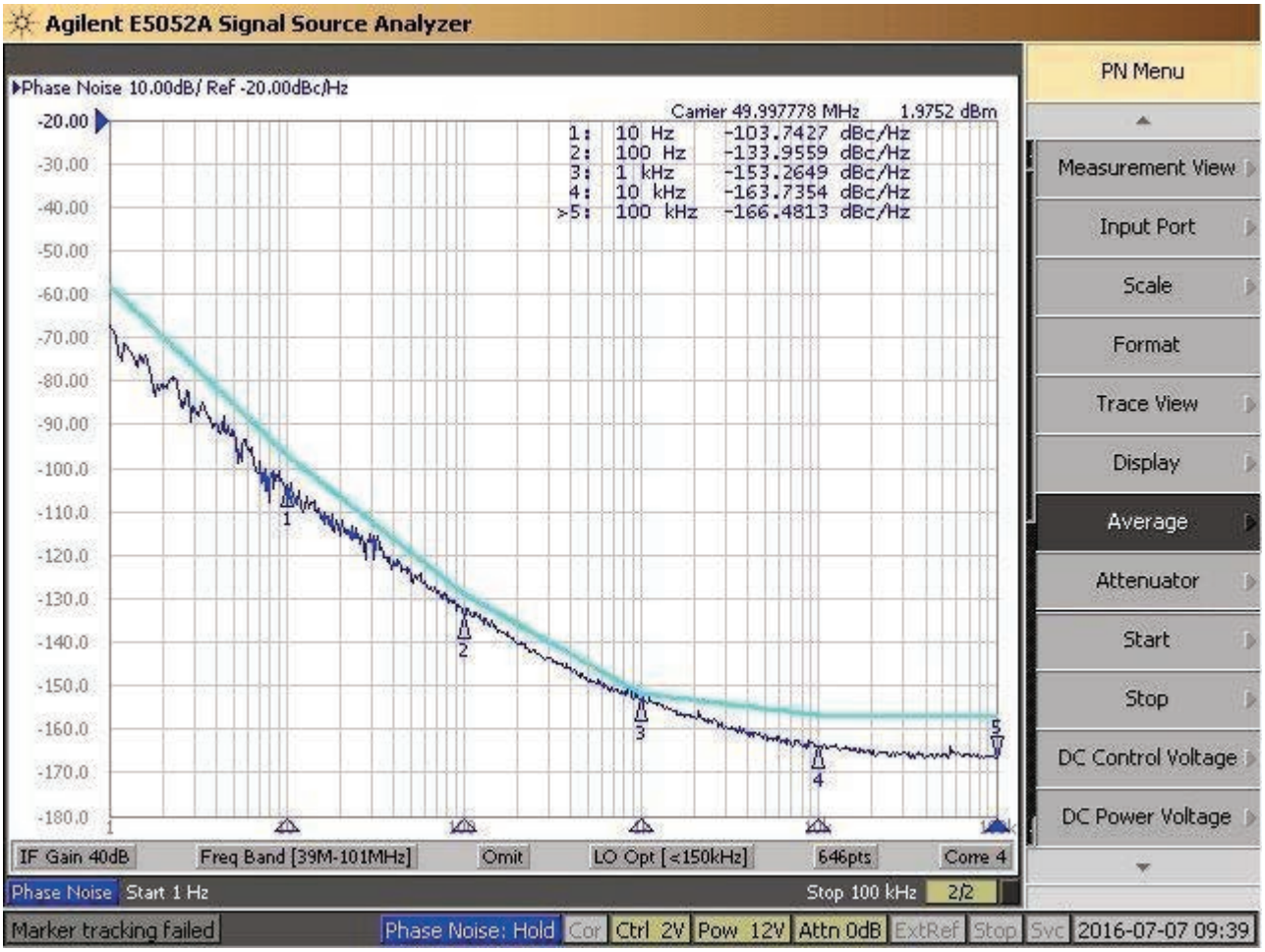


TABLE IV - SCREENING TESTS

TEST DESCRIPTION	STANDARD	METHOD	CONDITION	COMMENTS
Nondestructive Bond Pull	883	2023		2.4-Gram Pull
Internal Visual	883	2017	K	Class S
Stabilization Bake	883	1008	B, 48 Hours at +150°C	
Thermal Shock	883	1011	A	
Temperature Cycling	883	1010	B	
Constant Acceleration	883	2001	A (5000gs, Y1 Axis Only)	
Particle Impact Noise Detection (PIND)	883	2020	B	5 Passes Note 1
Electrical Test (CMOS)	Frequency, VOH, VOL, Tr, Tf, DC, Input Current @ +25ºC			
Electrical Test (Sine)	Frequency, Output Levels, Input Current @ +25ºC			
Burn-In	883	1015	+125°C for 240 hours	Note 2
Seal; Fine Leak	883	1014	A1 or B1	
Seal; Gross Leak	883	1014	C or B2	
Electrical Test (CMOS)	Frequency, VOH, VOL, Tr, Tf, DC, Input Current @ +25ºC and Temperature Extremes Listed on Electrical Specification			
Electrical Test (Sine)	Frequency, Output Levels, Input Current @ +25ºC and Temperature Extremes Listed on Electrical Specification			
Radiographic Inspection	883	2012		Class S
External Visual	883	2009		

NOTES
1. PIND testing shall be performed using five (5) independent passes and all failures found at the end of each pass are rejected. The survivors of the last pass are acceptable.
2. Burn-in shall be under the specified load and nominal voltage conditions.

TABLE V - GROUP A INSPECTION (NOTE 1)

TEST DESCRIPTION	CONDITION
Frequency-Temperature Stability	Measured at constant Vcontrol set to F nominal at 25ºC.
Frequency Pulling	Measured at minimum and maximum tuning voltage.
APR	Frequency Pulling - Stability - Aging
Tuning Ko	Measured every 0.25 Volts from minimum to maximum tuning voltage.
Input Current	Vdd nominal, Over specified operating temperature extremes.
Output Voltage, High (CMOS)	
Output Voltage, Low (CMOS)	
Output Waveform (CMOS)	
Duty Cycle (CMOS)	
Output Rise And Fall Times (CMOS)	
Output Level (Sine)	Vdd nominal, and ±5%, 25ºC and operating temperature extremes
Harmonics/Sub-Harmonics (Sine)	Vdd nominal, 25ºC
Phase Noise	
Frequency Adjustment Range	
External Visual	MIL-STD-883, Method 2009

NOTES
1. Group A inspection shall be performed on units that have passed the screening tests. All electrical performance tests of this specification shall be performed during Group A with the exception of any tests performed as part of the final electrical testing during 100 percent screening.

TABLE VI - GROUP B INSPECTION

SUBGROUP	TEST DESCRIPTION	CONDITION
1	Frequency Aging (Note 1)	MIL-PRF-55310, Para 3.6.34.2
2	Hermetic Seal (Note 2)	Fine Leak - MIL-STD-883, Method 1014, Condition A1 or B1 Gross Leak - MIL-STD-883, Method 1014, Condition C or B2
3	Electrical (Functional) (Note 2)	Vdd nominal, 25ºC

NOTES
1. Long term aging projections are performed per MIL-O-55310.
2. Shall be performed after completion of frequency aging and before parts are shipped.

TABLE VII - GROUP C INSPECTION

(Note 1)

SUBGROUP	TEST DESCRIPTION	CONDITION	QUANTITY (ACCEPT NO.)
1	Vibration (Random)	MIL-STD-202, Method 214 Condition I-K: 46Grms for 3 Minutes in Each Plane.	4 (0 Failures)
	Shock	MIL-STD-202, Method 213 Condition F: 1500g, 0.5ms Half-Sine Pulse, 3 Blows Each Direction of Three Axes (18 Shocks Total)	
	Electrical Test	Frequency, Output Levels (Sine), Waveform (CMOS), Input Current @ +25°C	
	Hermetic Seal	Fine Leak – MIL-STD-883, Method 1014, Condition A1 or B1 Gross Leak – MIL-STD-883, Method 1014, Condition C or B2	
	Electrical Test	Frequency, Output Levels (Sine), Waveform (CMOS), Input Current @ +25°C	
	Temperature Cycling	MIL-STD 883, Method 1010, Condition B: 100 Cycles	
	Electrical Test	Frequency, Output Levels (Sine), Waveform (CMOS), Input Current @ +25°C	
	Ambient Pressure (Non-Operating)	MIL-PRF-55310 Para. 4.8.46.1	
	Electrical Test	Frequency, Output Levels (Sine), Waveform (CMOS), Input Current @ +25°C	
	Storage Temperature	Low Temperature of -55°C (+0, -5) High Temperature of +150°C (+5,-0)	
	Hermetic Seal	Fine Leak – MIL-STD-883, Method 1014, Condition A1 or B1 Gross Leak – MIL-STD-883, Method 1014, Condition C or B2	
	Electrical Test	Frequency, Output Levels (Sine), Waveform (CMOS), Input Current @ +25°C and Temperature Extremes Listed on Electrical Specification	
3	Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition B	1 (0 Failures)
	Hermetic Seal	Fine Leak – MIL-STD-883, Method 1014, Condition A1 or B1 Gross Leak – MIL-STD-883, Method 1014, Condition C or B2	
	Moisture Resistance	MIL-STD-202, Method 106	
4	Terminal Strength (Lead Integrity)	MIL-STD-202, Method 211, Condition B	1 (0 Failures)
	Visual Inspection	MIL-STD-883, Method 2009	
	Hermetic Seal	Fine Leak – MIL-STD-883, Method 1014, Condition A1 or B1 Gross Leak – MIL-STD-883, Method 1014, Condition C or B2	
	Resistance To Solvents	MIL-STD 202 Method 215	

NOTES

1. Samples from Subgroup 1 may be divided and used for subgroups 3 and 4 inspections.

DCO	REV	REVISION SUMMARY	PAGE	DATE
7509	-	Initial Release	All	02/23/2018