FAIRCHILD
A Schlumberger Company

F100158
8-Bit Shift Matrix

F100K ECL Product

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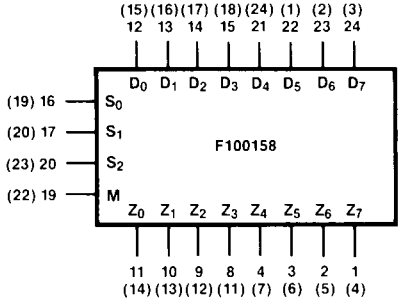
Description

The F100158 contains a combinatorial network which performs the function of an 8-bit shift matrix. Three control lines (S_n) are internally decoded and define the number of places which an 8-bit word present at the inputs (D_n) is shifted to the left and presented at the outputs (Z_n). A Mode Control input (M) is provided which, if LOW, forces LOW all outputs to the right of the one that contains D_7. This operation is sometimes referred to as *LOW backfill.* If M is HIGH, an end-around shift is performed such that D_0 appears at the output to the right of the one that contains D_7. This operation is commonly referred to as *barrel shifting.*

Pin Names

D_0-D_7	Data Inputs
S_0-S_2	Select Inputs
M	Mode Control Input
Z_0-Z_7	Data Outputs

Logic Symbol



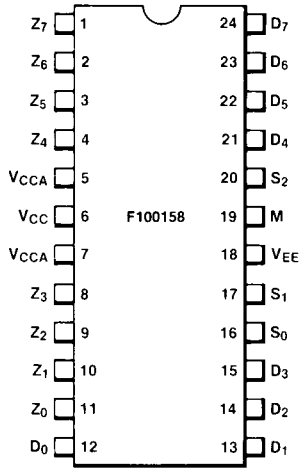
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 5 (8), 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Ordering Information

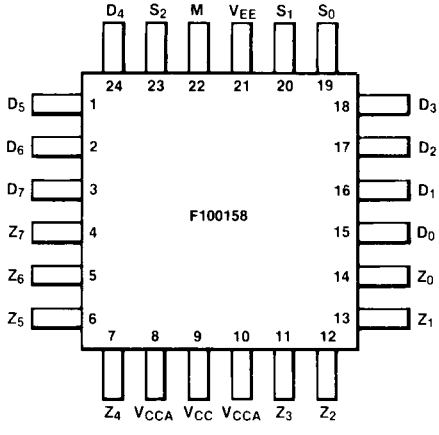
Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4Q	FC

Connection Diagrams

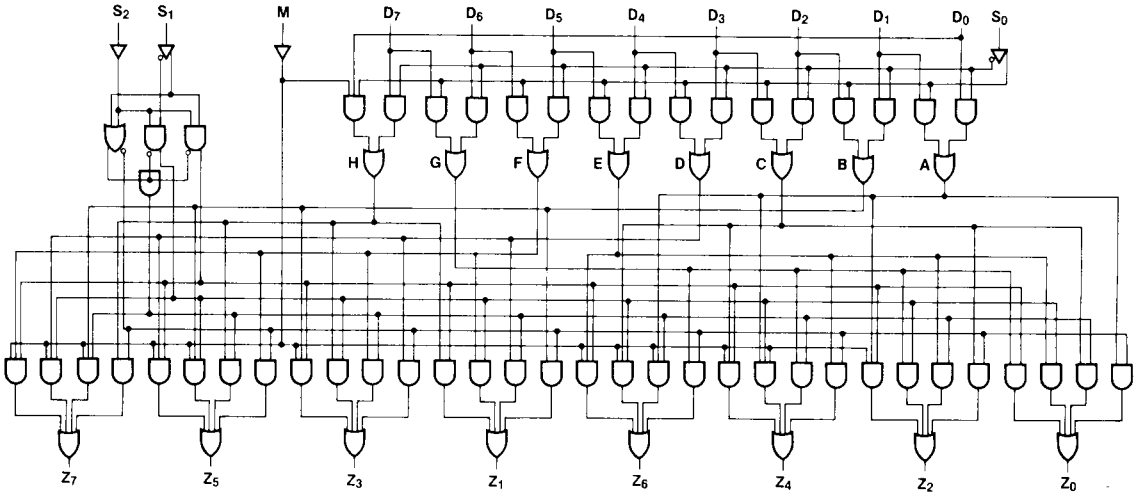
24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Logic Diagram



Truth Table

Inputs				Outputs							
M	**S_0**	**S_1**	**S_2**	**Z_0**	**Z_1**	**Z_2**	**Z_3**	**Z_4**	**Z_5**	**Z_6**	**Z_7**
X	L	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
L	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L
L	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	L	L
L	H	H	L	D_3	D_4	D_5	D_6	D_7	L	L	L
L	L	L	H	D_4	D_5	D_6	D_7	L	L	L	L
L	H	L	H	D_5	D_6	D_7	L	L	L	L	L
L	L	H	H	D_6	D_7	L	L	L	L	L	L
L	H	H	H	D_7	L	L	L	L	L	L	L
H	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0
H	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1
H	H	H	L	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2
H	L	L	H	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3
H	H	L	H	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4
H	L	H	H	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5
H	H	H	H	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC Characteristics: V_{EE} = −4.2 V to −4.8 V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C*

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current All Inputs			220	μA	$V_{IN} = V_{IH(max)}$
I_{EE}	Power Supply Current	−205	−140	−95	mA	Inputs Open

Ceramic Dual In-line Package AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

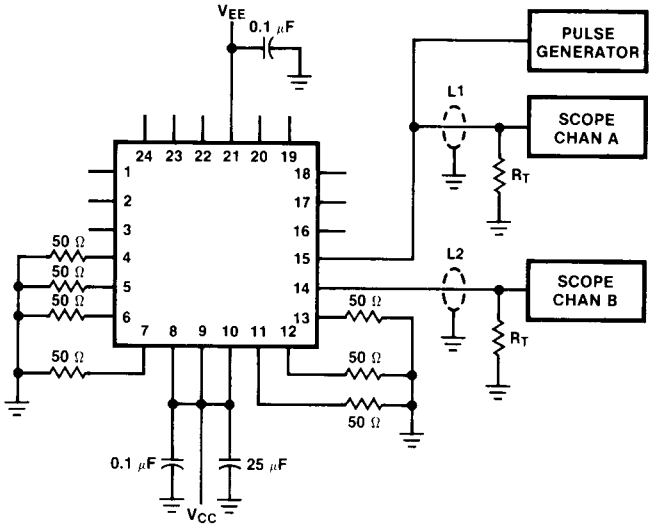
		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	1.10	2.80	1.10	2.70	1.10	2.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.15	4.20	1.25	4.20	1.15	4.20	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to Output	1.70	4.20	1.70	4.20	1.70	4.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.30	0.50	2.30	0.50	2.30	ns	

Flatpak AC Characteristics: V_{EE} = −4.2 V to −4.8 V, V_{CC} = V_{CCA} = GND

		T_C = 0°C		T_C = +25°C		T_C = +85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	1.10	2.60	1.10	2.50	1.10	2.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.15	4.00	1.25	4.00	1.15	4.00	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to Output	1.70	4.00	1.70	4.00	1.70	4.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.20	0.50	2.20	0.50	2.20	ns	

*See Family Characteristics for other dc specifications.

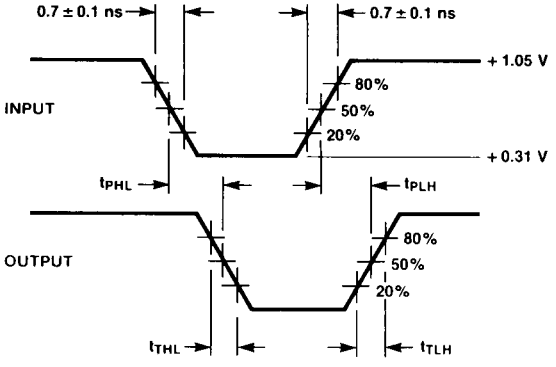
Fig. 1 AC Test Circuit



Notes

V_{CC}, V_{CCA} = +2 V, V_{EE} = -2.5 V
L1 and L2 = equal length 50 Ω impedance lines
R_T = 50 Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50 Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak, for DIP refer to logic symbol

Fig. 2 Propagation Delay and Transition Times



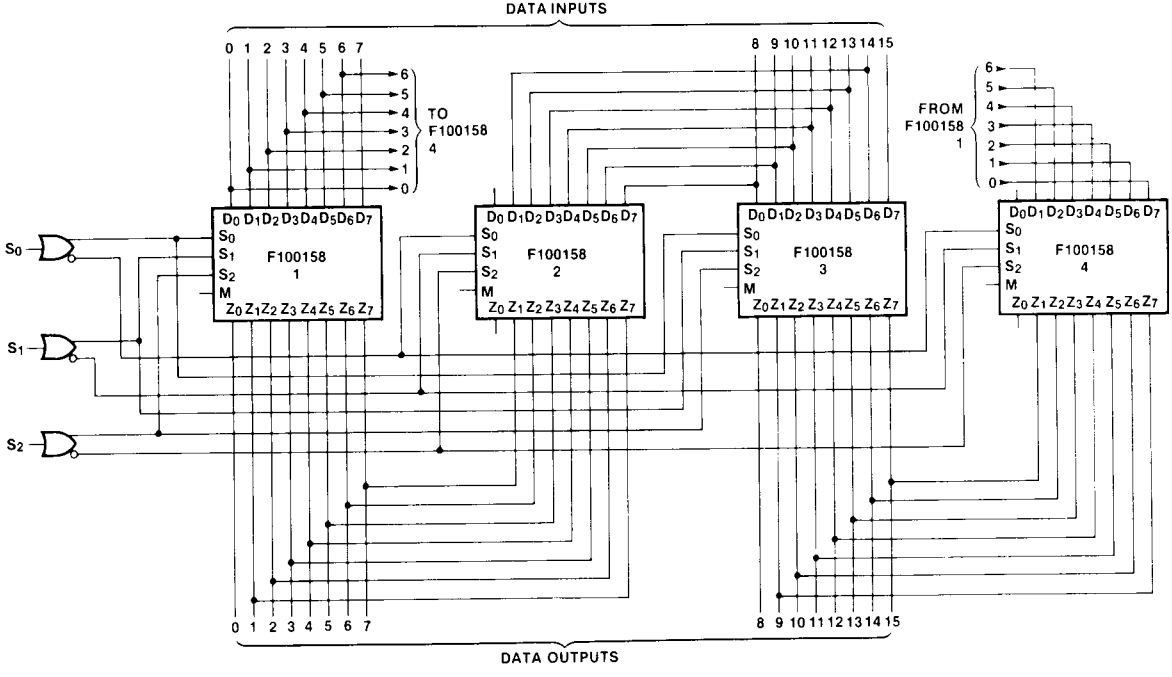
Applications

The following technique uses two ranks of F100158s to shift a 64-bit word from 0 to 63 places. Although two stage delays are required (one for each rank), the total shift takes only about 4 ns. This technique performs a bit shift on each 8-bit byte in the first rank and then a modulo-8 byte shift on the 64 bit word in the second rank.

Basic 16-Bit 0-7 Place Shifter

Figure 3 shows the basic 0-7 place shift technique which can be expanded to accommodate any word length. Each 8-bit byte requires a pair of F100158s operating in the LOW backfill mode. The address lines for each pair of ICs are driven out of phase by three OR gates. Inputs for the two ICs are taken from two bytes transposed in order; outputs are transposed and emitter-OR tied. One device shifts right from location 0 and the other shifts left from location 7. The bits shifted off one pair are picked up by the next pair of F100158s or — in the case of the last one in the rank — returned to the first device. The net result is a 0-7 place shift of the entire word.

Fig. 3 Basic 16-Bit 0-7 Place Shifter



Expanding to 64-Bit Word and 64-Place Shift

The basic 0-7 place shift technique can be expanded to accommodate a 64-bit word shifted from 0 to 63 places, however, two ranks of F100158s are required *(Figure 4)*. The first rank is identical to the one illustrated in *Figure 3* except it contains a total of 16 devices. The second rank consists of eight additional F100158s connected in the modulo-8 configuration shown in *Figure 5*.

The modulo-8 rank is used to simulate an 8-bit simultaneous shift since the F100158 cannot shift in 8-bit jumps. The modulo-8 configuration is achieved by wiring the first rank and the output device to the second rank as illustrated in *Figure 5*. The LSB of each output byte in the first rank is wired to one of the eight inputs of the first F100158 in the second rank. The next least significant bit of each first-rank F100158 pair, however, is connected to the inputs of the second F100158 in the second rank. The other first-ranked outputs are connected in a similar fashion to the remainder of the second-rank inputs. Ultimately, the outputs of the second rank must then be connected to reform the final usable 64-bit word so that the bits are again ordered from 0-63.

The effect is that each single-location shift in the second rank appears to be an eight place shift in the final word due to the way the inputs and outputs of the second rank are connected. The combination of the two ranks produces the 64-place shift of the entire word.

Fig. 4 64-Bit 0 — Place Barrel Shifter

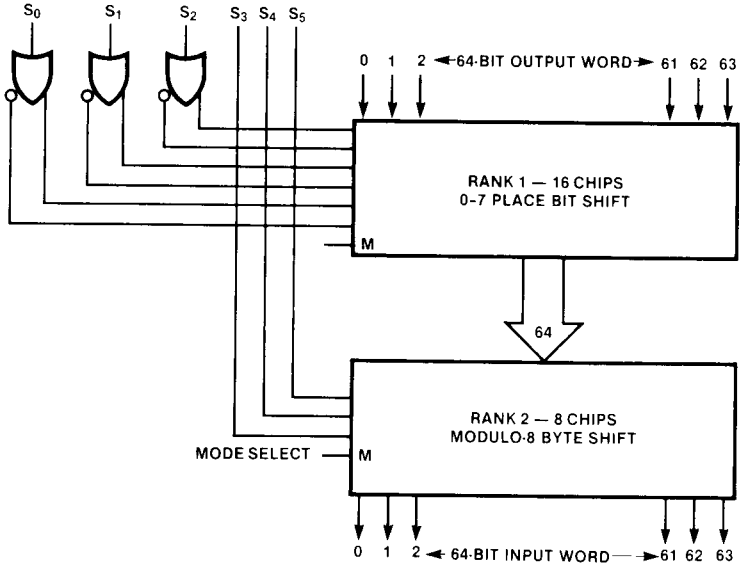


Fig. 5 Modulo-8 Shift