FUJITSU

CMOS 256K-BIT OTP ROM CARD

MB98621RC

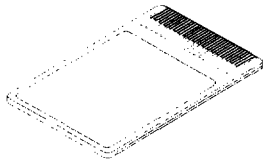
February 1988
Edition 1.0

CMOS 256K (262,144)-BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY CARD

The MB98621 is a memory card which is composed of one MBM27C256AP PROM organized as 32,768 words x 8 bits housed in 38-pin plastic package. This card has TTL compatible Input/Output and three state output level with fully static operation and a single +5V power supply is required.

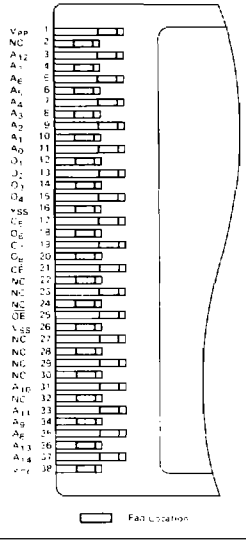
Dimensions of the card are Fujitsu standard.

- Card size: 2.216 width x 3.370 length x 0.081 height (inches)
- Organization: 32,768 words x 8 bits
- Access time: 250 ns max.
- Programming voltage: 12.5V
- Full static operation: No clock required
- Three state output
- TTL compatible Input/Output
- Single +5V power supply
- Power dissipation: 158mW max. (Active)
  5.25mW max. (Standby, TTL input level)
  0.53mW max. (Standby, CMOS input level)
- Fujitsu's original recessed edge connector helps to prevent chip damage from static electricity.
- On-chip series resistors for further protection from Electro-Static Discharge



PLASTIC CARD
CRD-38P-M03

PIN ASSIGNMENT
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.6 to +7.0	V
V_{PP} Voltage	V_{PP}	−0.6 to +14.0	V
All Inputs/Outputs Voltage	V_{IN}, V_{OUT}	−0.6 to V_{CC}+0.3	V
Voltage on A_9	V_{A9}	−0.6 to +13.5	V
Temperature under Bias	T_{BIAS}	−10 to +60	°C
Storage Temperature	T_{STG}	−30 to +70	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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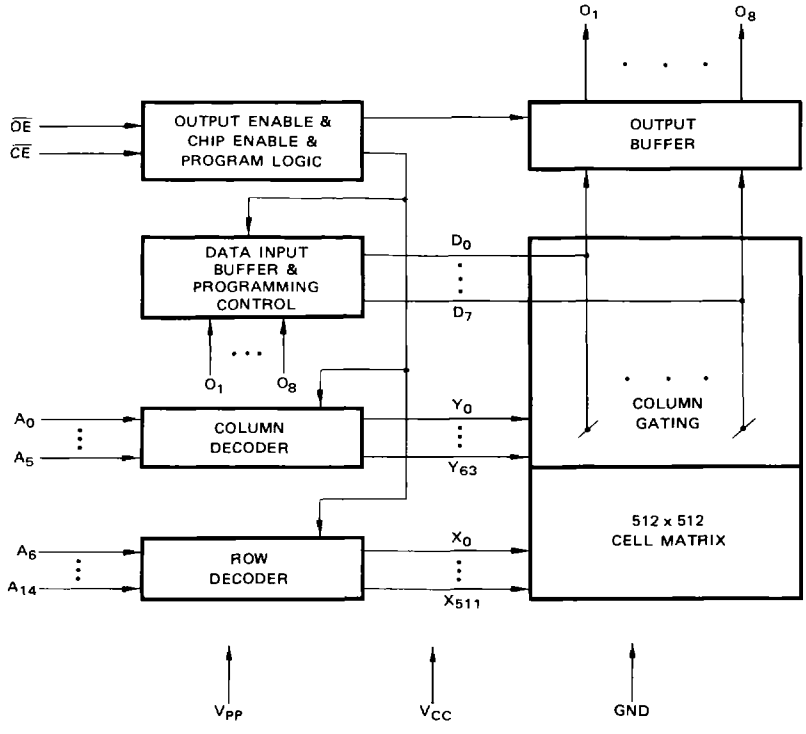
BLOCK DIAGRAM



PIN DESCRIPTION

Symbol	Pin Number	Parameter
A_0 to A_{14}	3, 4, 5, 6, 7, 8, 9, 10, 11, 31, 33, 34, 35, 36, 37	*Address Input*
O_1 to O_8	12, 13, 14, 15, 17, 18, 19, 20	Data I/O
$\overline{CE}$	21	Chip Enable
$\overline{OE}$	25	Output Enable
V_{CC}	38	Supply Voltage (+5V)
V_{PP}	1	Programming Supply Voltage
V_{SS}	16, 26	Ground
NC	2, 22, 23, 24, 27, 28, 29, 30, 32	Non Connection

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}	–	15	20	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	–	15	20	pF

FUNCTIONAL TRUTH TABLE

Function / Mode	Address Input	Data I/O	$\overline{CE}$	$\overline{OE}$	V_{CC}	V_{PP}	V_{SS}
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	+5V	+5V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	+5V	+5V	GND
Standby	Don't Care	High-Z	V_{IH}	Don't Care	+5V	+5V	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	+6V	+12.5V	GND
Program Verify	A_{IN}	D_{OUT}	Don't Care	V_{IL}	+6V	+12.5V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	V_{IH}	+6V	+12.5V	GND

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RECOMMENDED OPERATING CONDITIONS

(Reference to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
V_{CC} Supply Voltage*	V_{CC}	4.75	5.0	5.25	V
V_{PP} Supply Voltage	V_{PP}	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Ambient Temperature	T_A	0		50	°C

Note: * V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC CHARACTERISTICS

READ MODE (Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Value			Unit
			Min	Typ	Max	
V_{CC} Active Current	$\overline{CE} = V_{IL}$	I_{CC1}			30	mA
	f = 4MHz, I_{OUT} = 0mA	I_{CC2}			30	mA
V_{PP} Supply Current	$V_{PP} = V_{CC} \pm 0.6V$	I_{PP}		1	100	μA
V_{CC} Standby Current	$\overline{CE} = V_{IH}$	I_{SB1}			1	mA
	$\overline{CE} = V_{CC} \pm 0.3V$, I_{OUT} = 0mA	I_{SB2}		1	100	μA
Input Leakage Current	V_{IN} = 5.25V	I_{LI}			10	μA
Output Leakage Current	V_{OUT} = 5.25V	I_{LO}			10	μA
Output High Voltage	I_{OH} = −400μA	V_{OH}	2.4			V
Output Low Voltage	I_{OL} = 2.1mA	V_{OL}			0.45	V

PROGRAMMING MODE ($T_A = 25 \pm 5°C$, V_{CC}*1 = 6 ± 0.25V, V_{PP}*2 = 12.5 ± 0.3V)

Parameter	Test Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Leakage Current	V_{IN} = 6.25V/0.45V	I_{LI}			10	μA
V_{CC} Supply Current		I_{CC}			30	mA
V_{PP} Supply Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	I_{PP2}			50	mA
	$\overline{OE} = V_{IL}$	I_{PP3}			5	mA
Input High Level		V_{IH}	2.2		V_{CC}+0.3	V
Input Low Level		V_{IL}	−1.0		0.8	V
Output High Voltage during Verify	I_{OH} = −400μA	V_{OH}	2.4			V
Output Low Voltage during Verify	I_{OL} = 2.1mA	V_{OL}			0.45	V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts. Also, during $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

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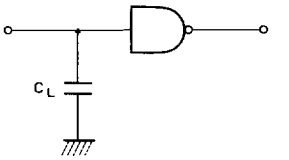
AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Level	:	0.8 to 2.2V
Input Pulse Rise/Fall Time	:	$t_T \leq 20$ns
Timing Reference Levels		
Input	:	V_{IL} = 1.0V, V_{IH} = 2.2V
Output	:	V_{OL} = 0.8V, V_{OH} = 2.0V
Output Load	:	1TTL gate and 100pF



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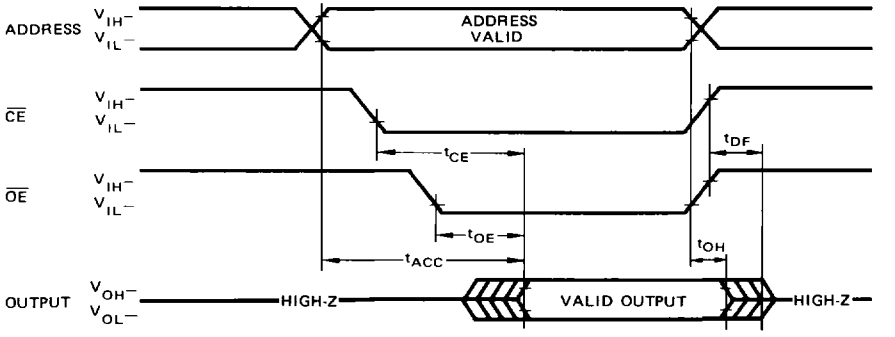
AC CHARACTERISTICS

READ MODE (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit
		Min	Max	
Address Access Time*1	t_{ACC}		250	ns
Chip Enable Access Time	t_{CE}		250	ns
Output Enable Access Time*1	t_{OE}		100	ns
Output Disable Time*2	t_{DF}	0	60	ns
Output Hold Time	t_{OH}	0		ns

Note: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

READ WAVEFORM

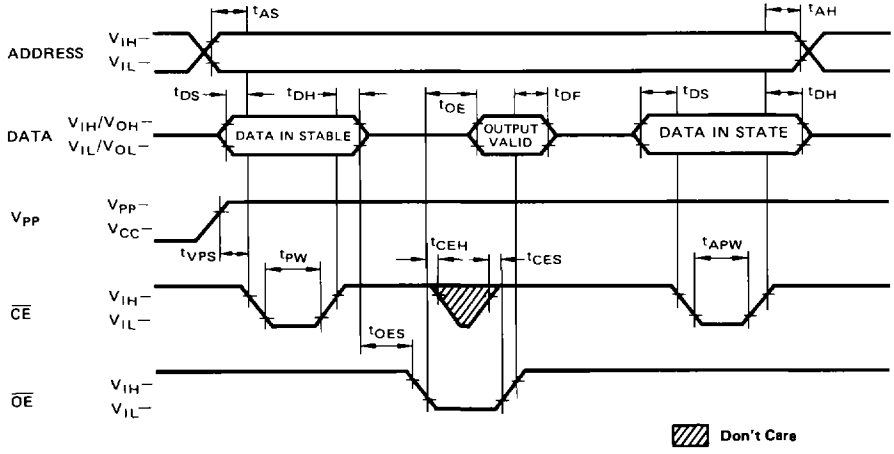


AC CHARACTERISTICS (continued)

PROGRAMMING MODE (T_A = 25 ± 5°C, V_{CC} = 6 ± 0.25V, V_{PP} = 12.5 ± 0.3V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{AS}	2			μs
Data Setup Time	t_{DS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
V_{PP} Setup Time	t_{VPS}	2			μs
Output Setup Time	t_{OES}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Chip Enable Hold Time	t_{CEH}	2			μs
Output Enable to Output Valid	t_{OE}			120	ns
Output Disable to Output Float Delay	t_{DF}			105	ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Additional Programming Pulse Width	t_{APW}	2.85		78.75	ms
Programming Pulse Times	–	1		25	times

PROGRAMMING WAVEFORM



PROGRAMMING INFORMATION

PROGRAMMING

Upon delivery from Fujitsu, the MB98621 has all 262,144 bits in the "1", or high state. "0's" are loaded into the MB98621 through the procedure of programming.

The MB98621 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{CE}$ and $\overline{OE}$ are V_{IH}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1ms programming pulse is applied to $\overline{CE}$ and after that one additional pulse which is 3 times as wide as previous pulse is applied to $\overline{CE}$ to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flowchart).

1) Set the start address (=G) at the address pins.
2) Set V_{CC}=6V, V_{PP}=12.5V and $\overline{CE}$=V_{IH}.
3) Clear the programming pulse counter (X←0).
4) Input data to respective pins.
5) Apply one programming pulse (t_{PW}=1ms Typ) to $\overline{CE}$.
6) Increment the counter (X←X+1).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X=25 and programmed data is not verified, the device fails. If X<25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{CE}$ (3Xms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G←G+1) and then go to the step 3) for the next address.
10) Set V_{CC}=V_{PP}=5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP}=12.5V, V_{CC}=6V and $\overline{OE}$=V_{IH}) because it is required that one programming pulse width does not exceed 78.75ms at each address.

ELECTRONIC SIGNATURE

The MB98621 has electronic signature mode which is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

The electronic signature is activated when +12V is applied to address line A_9 (pin 34) of the MB98621. Two identifier bytes are readed out from the outputs by toggling address line A_0 (pin 11) from V_{IL} to V_{IH}. The address lines from A_1 to A_{13} must be hold at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	0	1	0	0	0	1	1	0	Device

Note: A_9 = 12 ± 0.5V
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}
A_{14} = Either V_{IL} or V_{IH}

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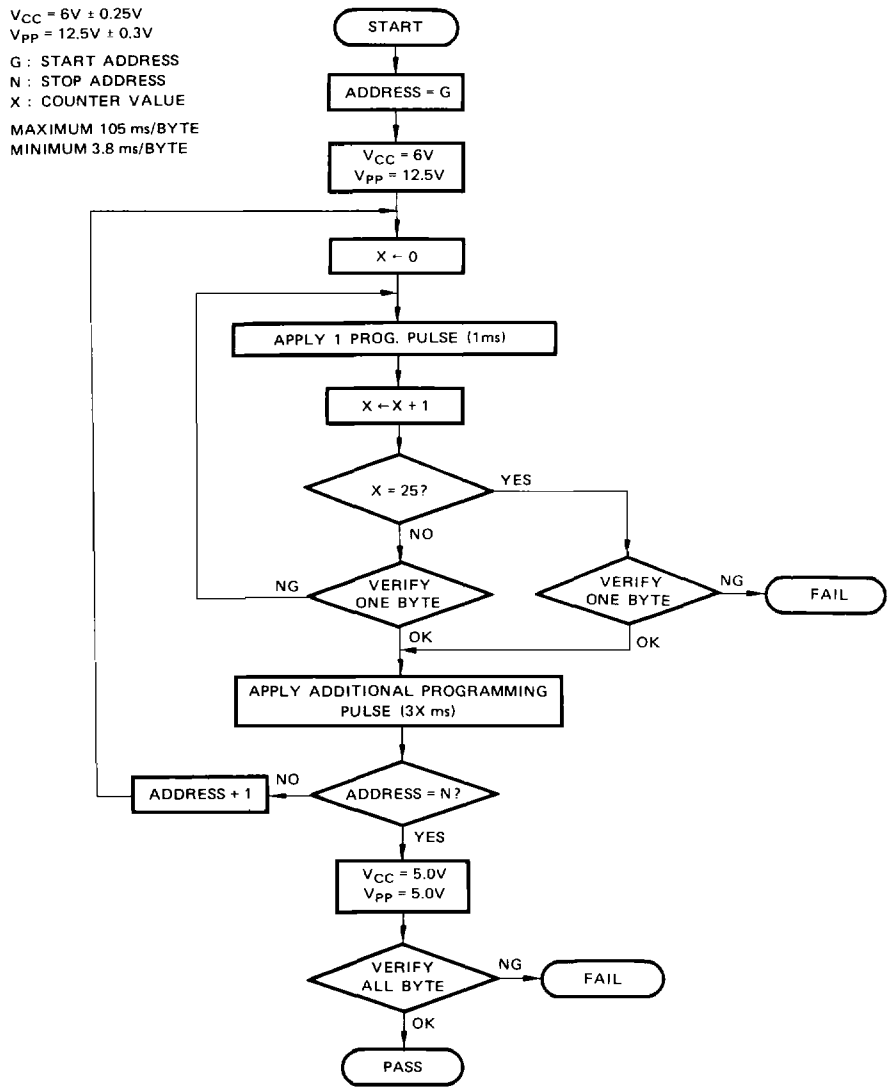
PROGRAMMING INFORMATION (continued)

PROGRAMMING FLOW CHART FOR Quick Pro™



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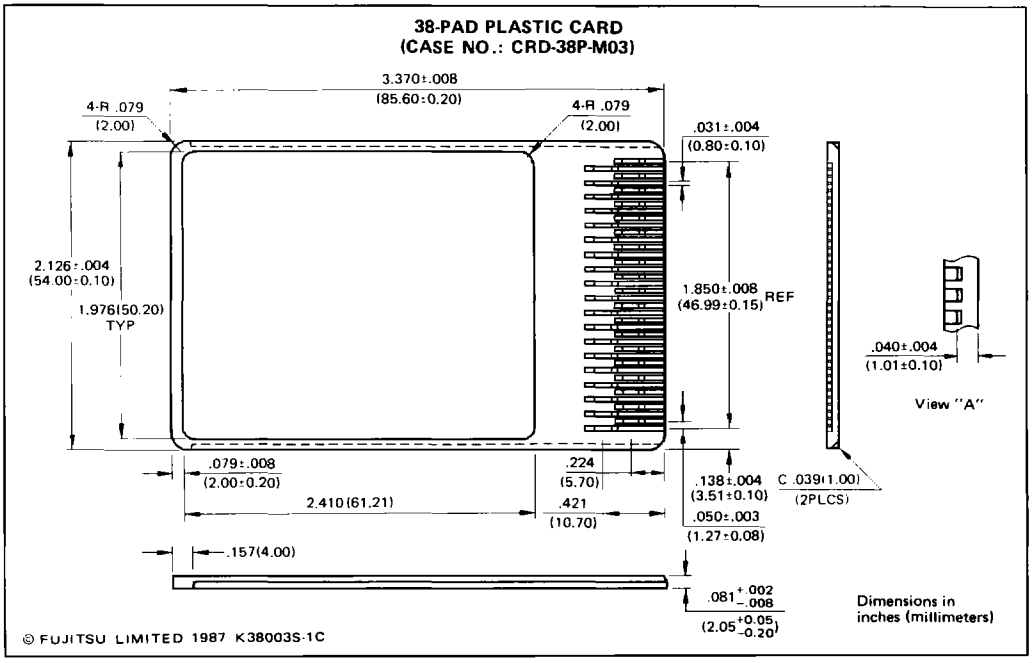
PACKAGE DIMENSIONS



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Memory Card Use Notice

- When not in use, it is recommended that the memory card be stored in its anti-static vinyl bag to prevent damage from static electricity.
- The card should be inserted before power-on to avoid possible data conflicts between the card and equipment. If the card is inserted or extracted with power-on, data may be output on the data pins even though $\overline{CE}$ and $\overline{OE}$ is at an "H".