HS-1412RH

Radiation Hardened, Quad, High Speed, Low Power, Video Closed Loop Buffer

FN4230
Rev 1.00
August 1999

The HS-1412RH is a radiation hardened quad closed loop buffer featuring user programmable gain and high speed performance. Manufactured on Intersil's proprietary complementary bipolar UHF-1 (DI bonded wafer) process, this device offers wide -3dB bandwidth of 340MHz, very fast slew rate, excellent gain flatness and high output current. These devices are QML approved and are processed and screened in full compliance with MIL-PRF-38535.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-96834. A "hot-link" is provided on our homepage for downloading.
www.intersil.com/spacedefense/space.asp

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^{o}C)
5962F9683401VCA	HS1-1412RH-Q	-55 to 125
5962F9683401VCC	HS1B-1412RH-Q	-55 to 125

Features

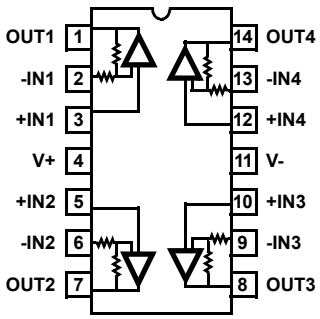
- Electrically Screened to SMD # 5962-96834
- QML Qualified per MIL-PRF-38535 Requirements
- MIL-PRF-38535 Class V Compliant
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Standard Operational Amplifier Pinout
- Low Supply Current . . . . . 5.9mA/Op Amp (Typ)
- Excellent Gain Accuracy . . . . . .0.99V/V (Typ)
- Wide -3dB Bandwidth. . . . . 340MHz (Typ)
- Fast Slew Rate. . . . . .1155V/μs (Typ)
- High Input Impedance . . . . . 1MΩ (Typ)
- Excellent Gain Flatness (to 50MHz). . . . . $\pm$0.02dB (Typ)
- Fast Overdrive Recovery . . . . . <10ns (Typ)
- Total Gamma Dose . . . . . 300kRAD(Si)
- Latch Up. . . . . None (DI Technology)

Applications

- Flash A/D Driver
- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Imaging Systems

Pinout

HS-1412RH (CERDIP) GDIP1-T14
OR
HS-1412RH (SBDIP) CDIP2-T14
TOP VIEW



Application Information

HS-1412RH Advantages

The HS-1412RH features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space. Implementing a quad, gain of 2, cable driver with this IC eliminates the eight gain setting resistors, which frees up board space for termination resistors.

Like most newer high performance amplifiers, the HS-1412RH is a current feedback amplifier (CFA). CFAs offer high bandwidth and slew rate at low supply currents, but can be difficult to use because of their sensitivity to feedback capacitance and parasitics on the inverting input (summing node). The HS-1412RH eliminates these concerns by bringing the gain setting resistors on-chip. This yields the optimum placement and value of the feedback resistor, while minimizing feedback and summing node parasitics. Because there is no access to the summing node, the PCB parasitics do not impact performance at gains of +2 or -1 (see “Unity Gain Considerations” for discussion of parasitic impact on unity gain performance).

The HS-1412RH’s closed loop gain implementation provides better gain accuracy, lower offset and output impedance, and better distortion compared with open loop buffers.

Closed Loop Gain Selection

This “buffer” operates in closed loop gains of -1, +1, or +2, with gain selection accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1 (see next section for layout caveats), while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded through a 50Ω resistor.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT	-INPUT
-1	50Ω to GND	Input
+1	Input	NC (Floating)
+2	Input	GND

Unity Gain Considerations

Unity gain selection is accomplished by floating the -Input of the HS-1412RH. Anything that tends to short the -Input to GND, such as stray capacitance at high frequencies, will cause the amplifier gain to increase toward a gain of +2. The result is excessive high frequency peaking, and possible instability. Even the minimal amount of capacitance associated with attaching the -Input lead to the PCB results in approximately 6dB of gain peaking. At a minimum this requires due care to ensure the minimum capacitance at the -Input connection.

Table 1 lists five alternate methods for configuring the HS-1412RH as a unity gain buffer, and the corresponding performance. The implementations vary in complexity and involve performance trade-offs. The easiest approach to implement is simply shorting the two input pins together, and applying the input signal to this common node. The amplifier bandwidth decreases from 550MHz to 370MHz, but excellent gain flatness is the benefit. A drawback to this approach is that the amplifier input noise voltage and input offset voltage terms see a gain of +2, resulting in higher noise and output offset voltages. Alternately, a 100pF capacitor between the inputs shorts them only at high frequencies, which prevents the increased output offset voltage but delivers less gain flatness.

Another straightforward approach is to add a 620Ω resistor in series with the amplifier’s positive input. This resistor and the HS-1412RH input capacitance form a low pass filter which rolls off the signal bandwidth before gain peaking occurs. This configuration was employed to obtain the data sheet AC and transient parameters for a gain of +1.

Pulse Overshoot

The HS-1412RH utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased overshoot on the negative portion of the output waveform (see Figure 5, Figure 7, and Figure 9). This overshoot isn’t present for small bipolar signals (see Figure 4, Figure 6, and Figure 8) or large positive signals. Figure 28 through Figure 31 illustrate the amplifier’s overshoot dependency on input transition time, and signal polarity.

TABLE 1. UNITY GAIN PERFORMANCE FOR VARIOUS IMPLEMENTATIONS

APPROACH	PEAKING (dB)	BW (MHz)	SR (V/μs)	±0.1dB GAIN FLATNESS (MHz)
Remove -IN Pin	5.0	550	1300	18
$+R_S$ = 620Ω	1.0	230	1000	25
$+R_S$ = 620Ω and Remove -IN Pin	0.7	225	1000	28
Short +IN to -IN (e.g., Pins 2 and 3)	0.1	370	500	170
100pF Capacitor Between +IN and -IN	0.3	380	550	130

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board (PCB). **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

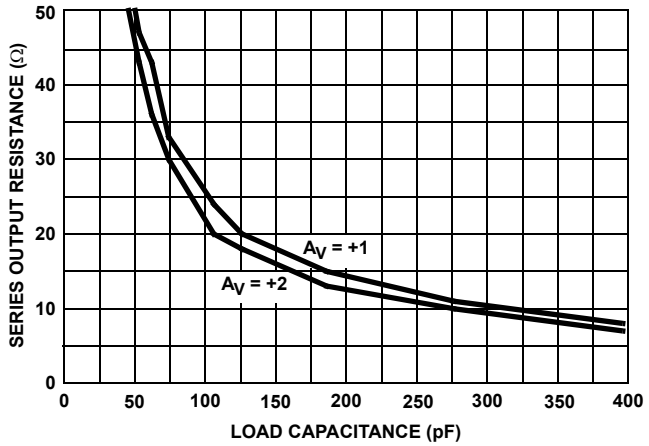


FIGURE 1. RECOMMENDED SERIES RESISTOR vs LOAD CAPACITANCE

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 350MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth decreases as the load capacitance increases. For example, at A_V = +2, R_S = 22Ω, C_L = 100pF, the overall bandwidth is 125MHz, and bandwidth drops to 100MHz at R_S = 12Ω, C_L = 220pF.

Evaluation Board

The performance of the HS-1412RH may be evaluated using the HA5025 Evaluation Board, slightly modified as follows:

1. Remove the four feedback resistors, and leave the connections open.
2. a. For A_V = +1 evaluation, remove the gain setting resistors (R_1), and leave pins 2, 6, 9, and 13 floating.
   b. For A_V = +2, replace the gain setting resistors (R_1) with 0Ω resistors to GND.

The modified schematic for amplifier 1, and the board layout are shown in Figures 2 and 3.

To order evaluation boards (part number HA5025EVAL), please contact your local sales office.

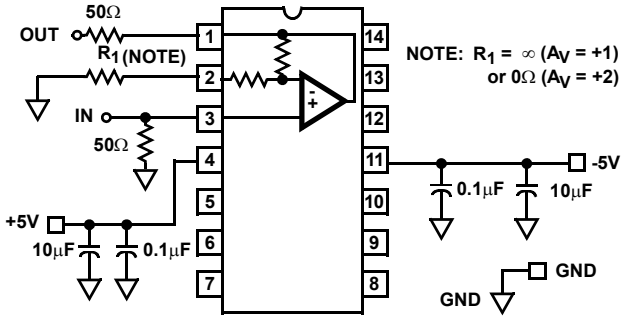


FIGURE 2. MODIFIED EVALUATION BOARD SCHEMATIC

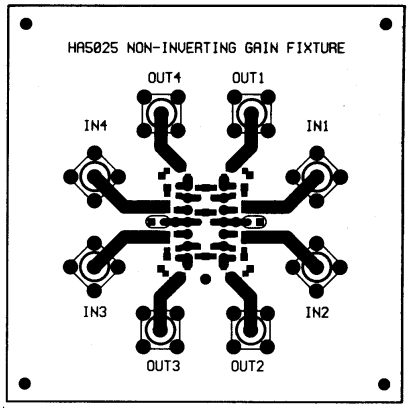


FIGURE 3A. TOP LAYOUT

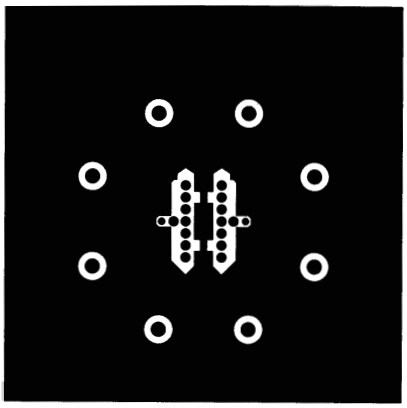


FIGURE 3B. BOTTOM LAYOUT

FIGURE 3. EVALUATION BOARD LAYOUT

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

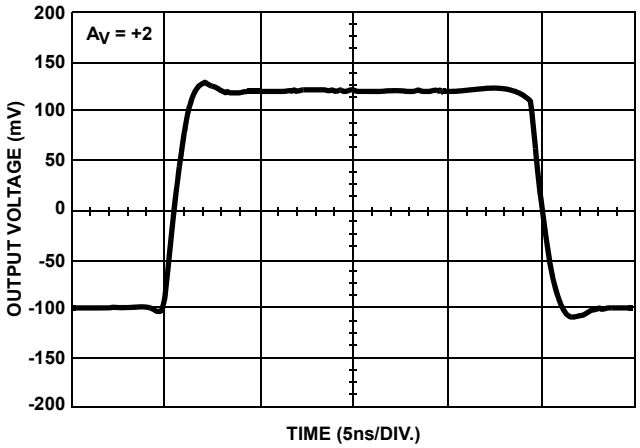


FIGURE 4. SMALL SIGNAL PULSE RESPONSE

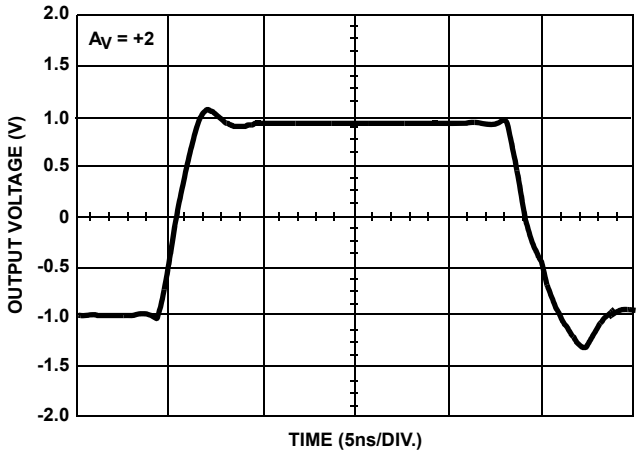


FIGURE 5. LARGE SIGNAL PULSE RESPONSE

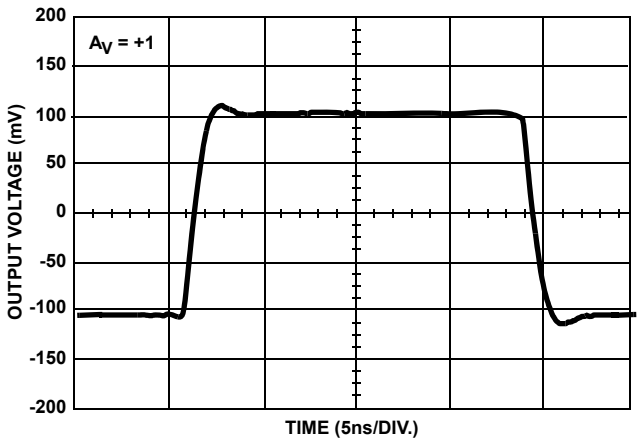


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

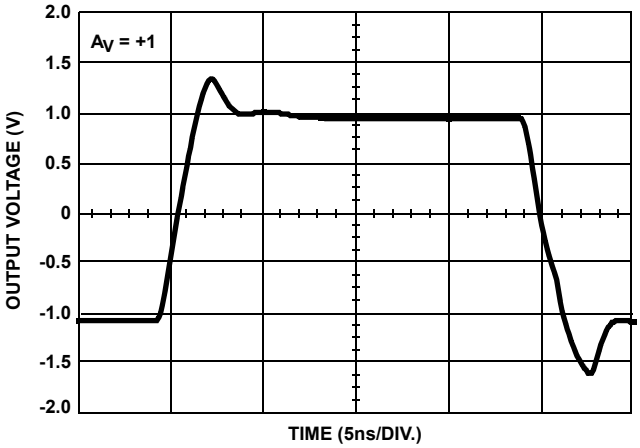


FIGURE 7. LARGE SIGNAL PULSE RESPONSE

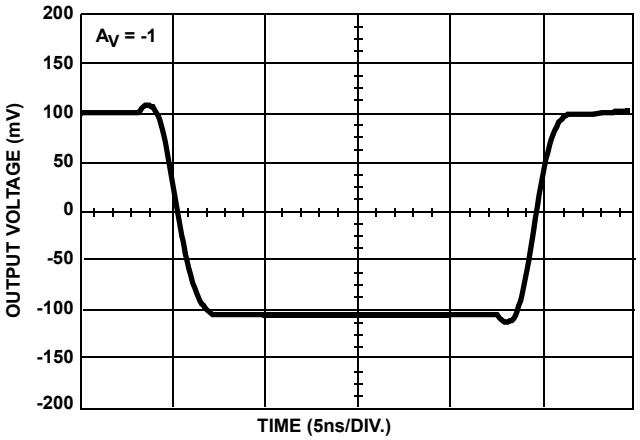


FIGURE 8. SMALL SIGNAL PULSE RESPONSE

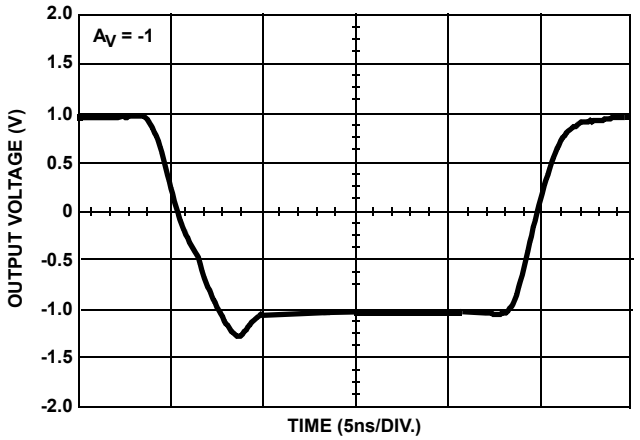


FIGURE 9. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

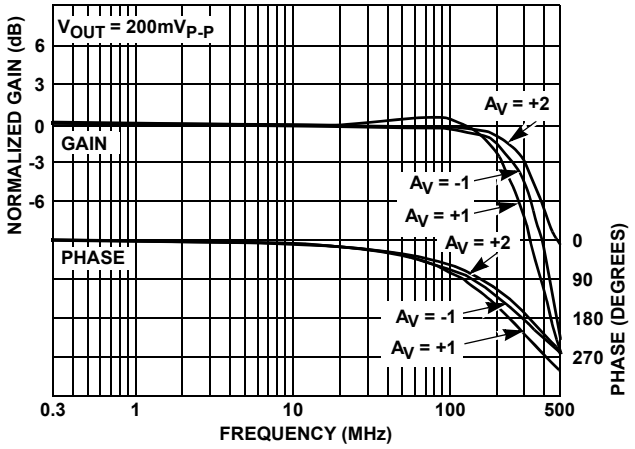


FIGURE 10. FREQUENCY RESPONSE

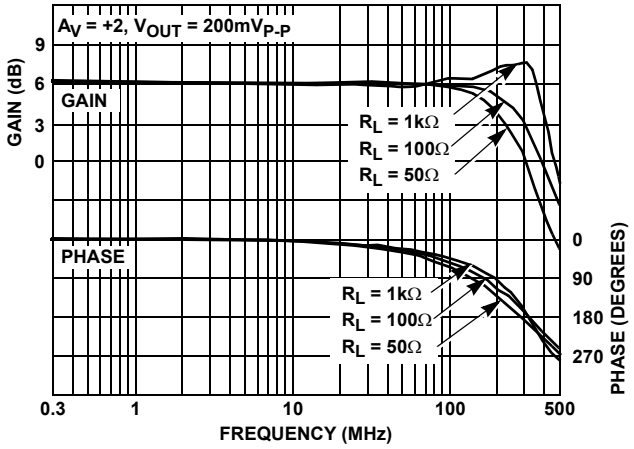


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

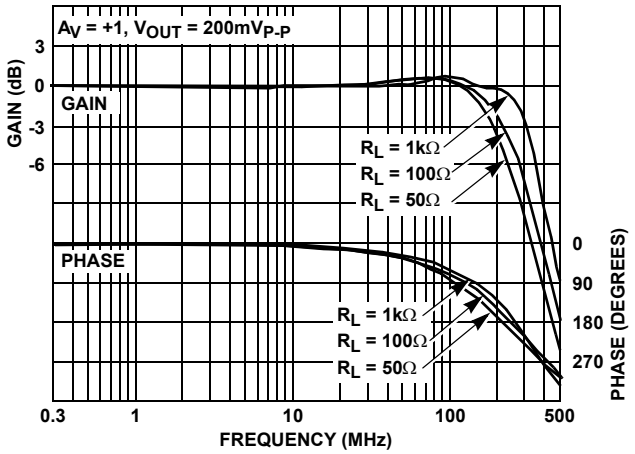


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

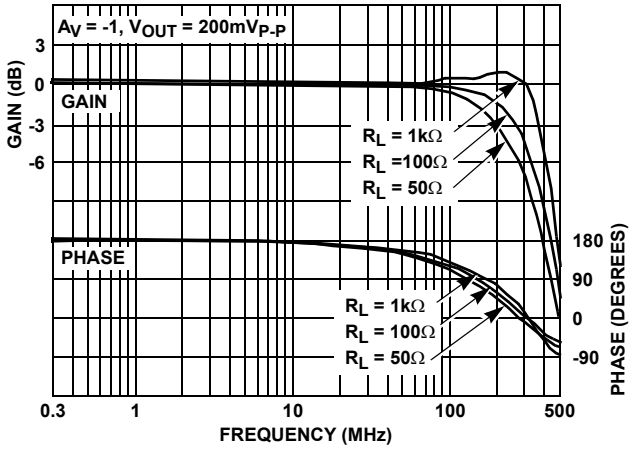


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

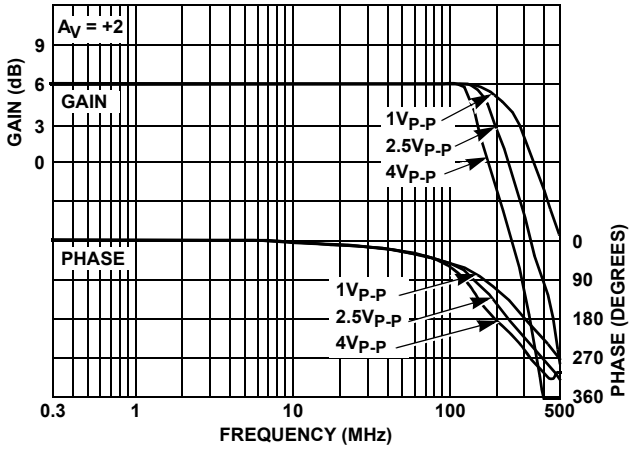


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

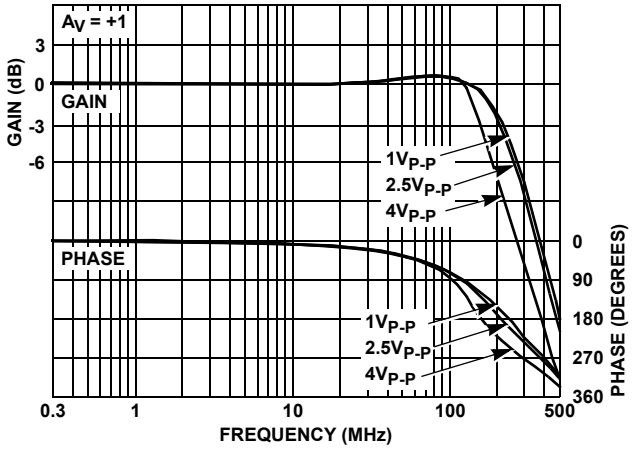


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

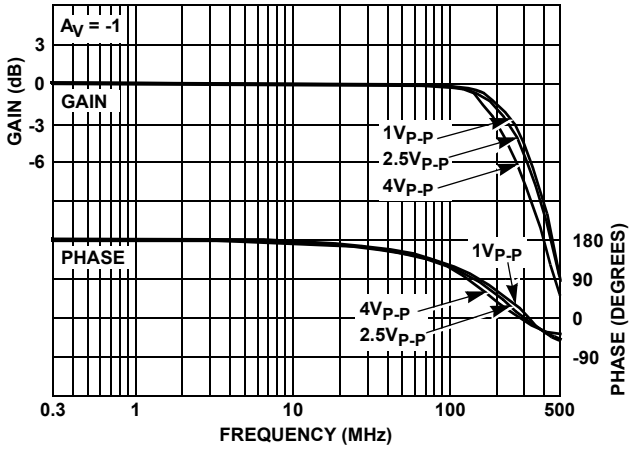


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

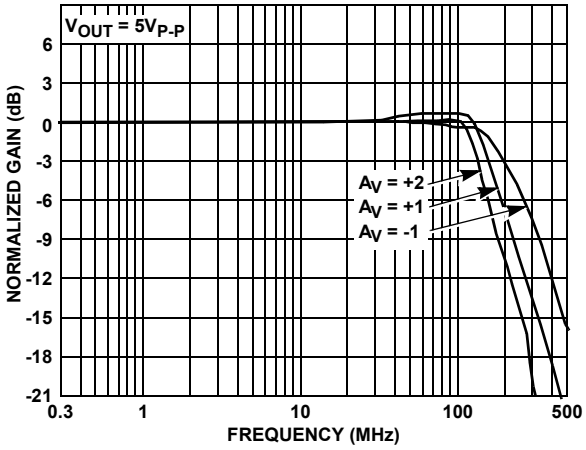


FIGURE 17. FULL POWER BANDWIDTH

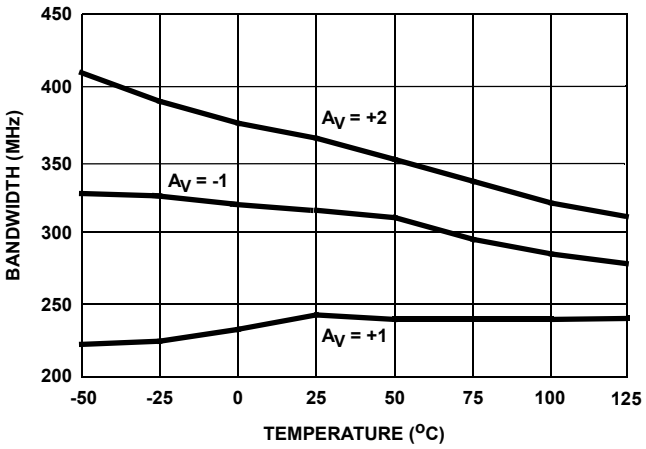


FIGURE 18. -3dB BANDWIDTH vs TEMPERATURE

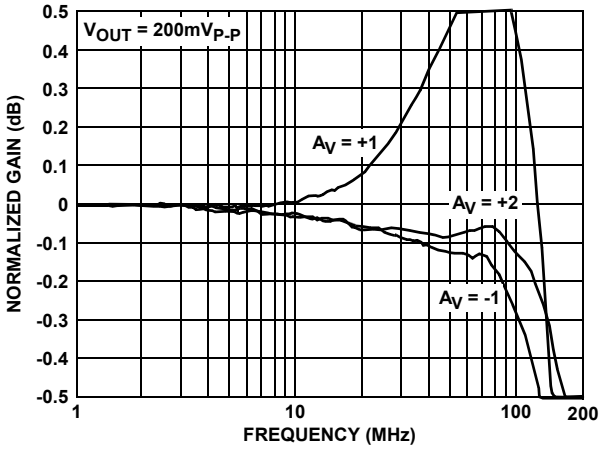


FIGURE 19. GAIN FLATNESS

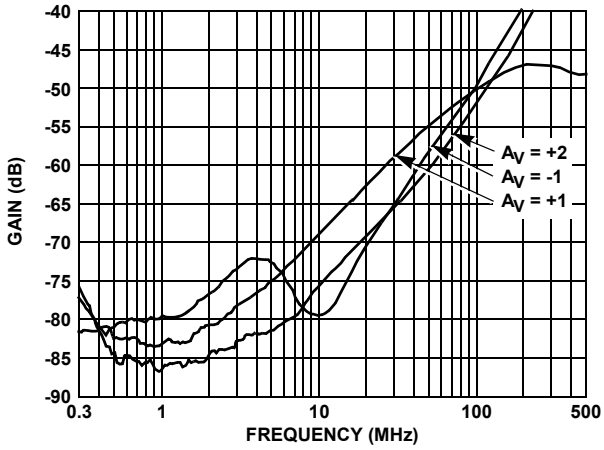


FIGURE 20. REVERSE ISOLATION (S_{12})

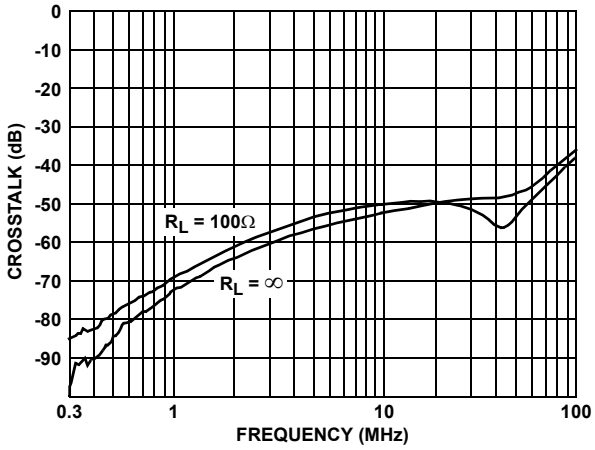


FIGURE 21. ALL HOSTILE CROSSTALK

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

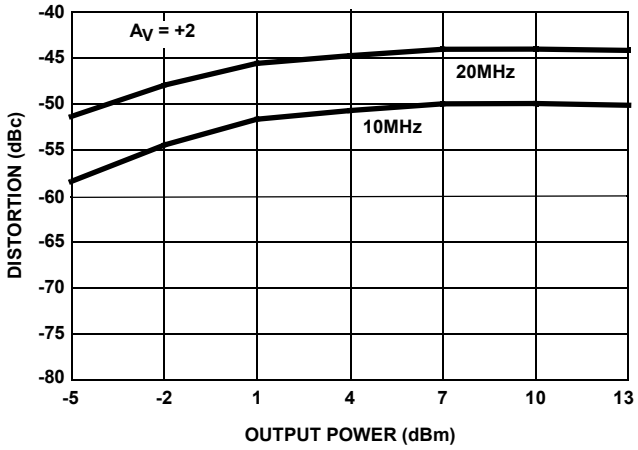


FIGURE 22. 2nd HARMONIC DISTORTION vs P_{OUT}

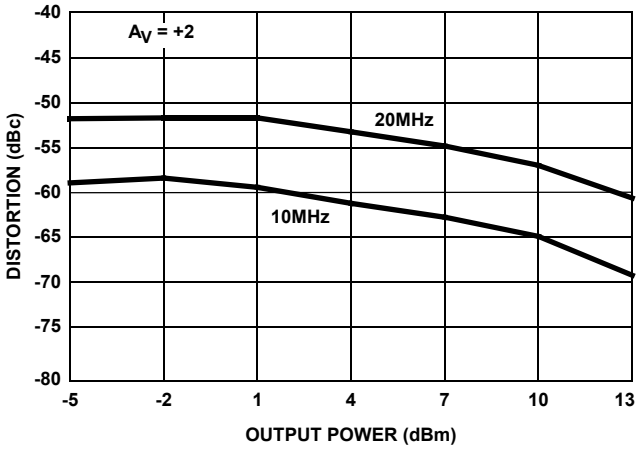


FIGURE 23. 3rd HARMONIC DISTORTION vs P_{OUT}

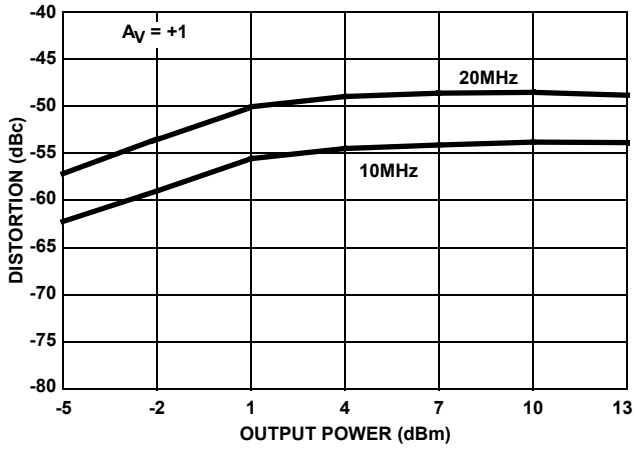


FIGURE 24. 2nd HARMONIC DISTORTION vs P_{OUT}

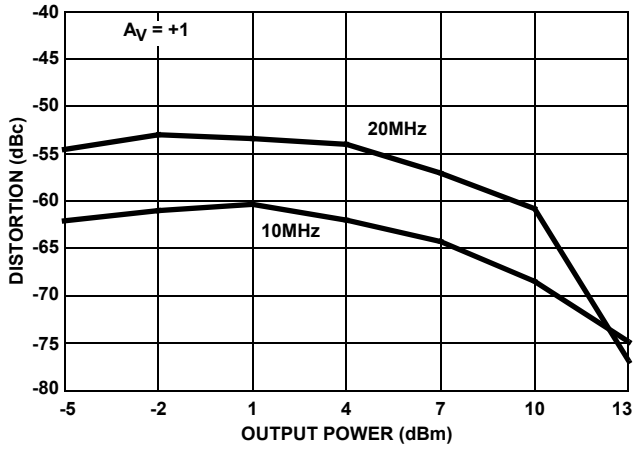


FIGURE 25. 3rd HARMONIC DISTORTION vs P_{OUT}

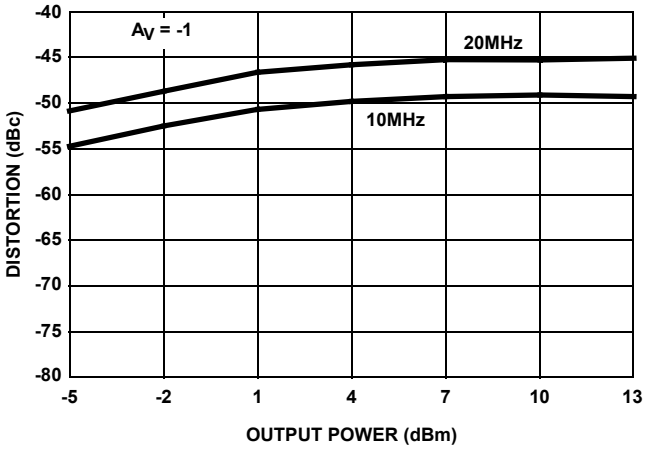


FIGURE 26. 2nd HARMONIC DISTORTION vs P_{OUT}

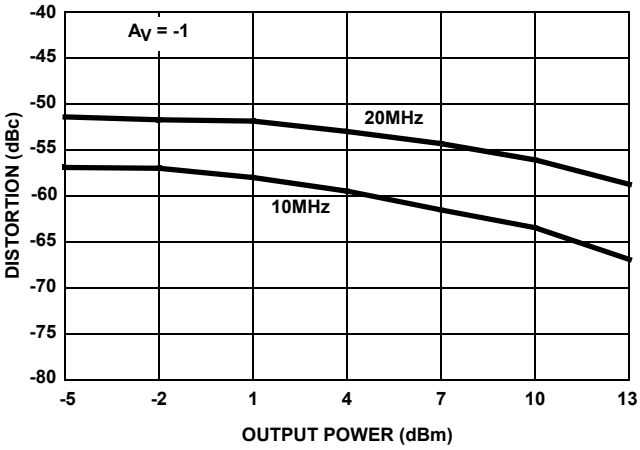


FIGURE 27. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

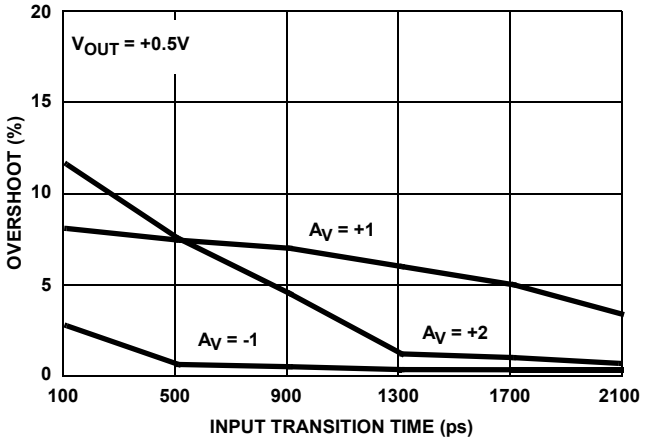


FIGURE 28. OVERSHOOT vs TRANSITION TIME

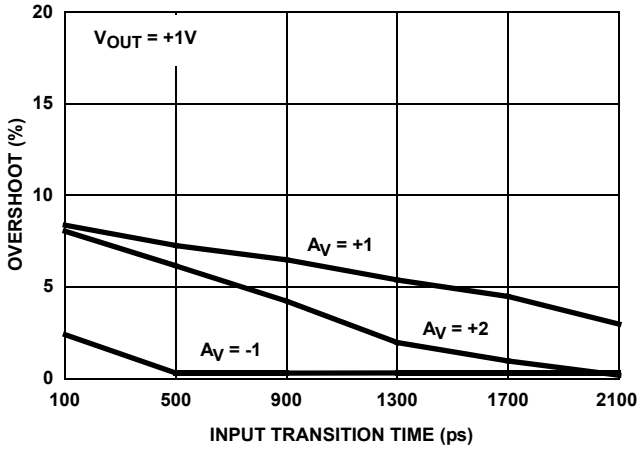


FIGURE 29. OVERSHOOT vs TRANSITION TIME

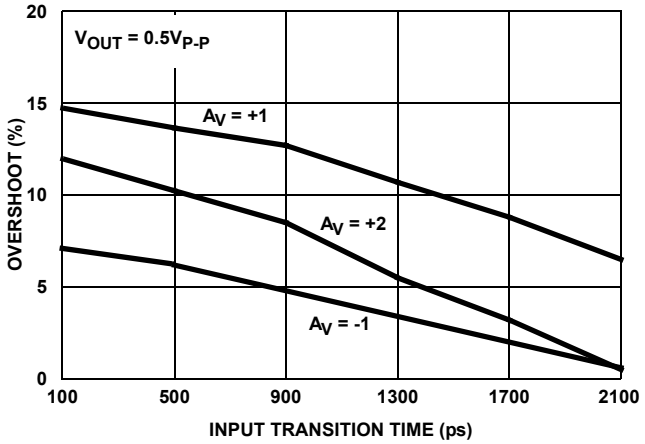


FIGURE 30. OVERSHOOT vs TRANSITION TIME

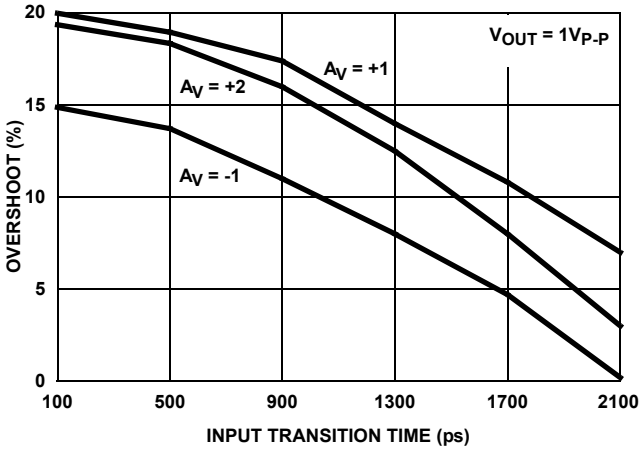


FIGURE 31. OVERSHOOT vs TRANSITION TIME

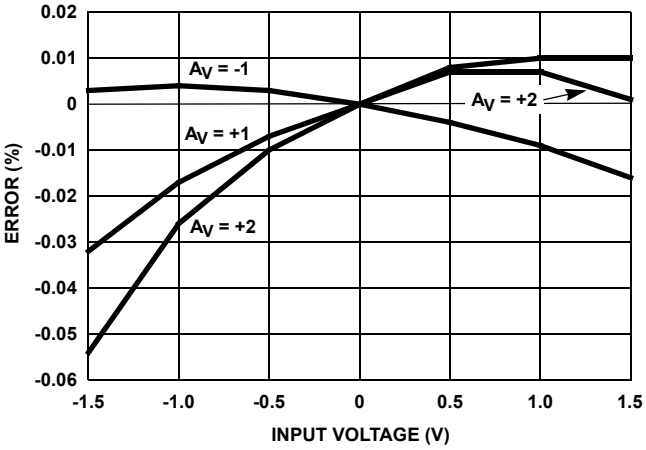


FIGURE 32. INTEGRAL LINEARITY ERROR

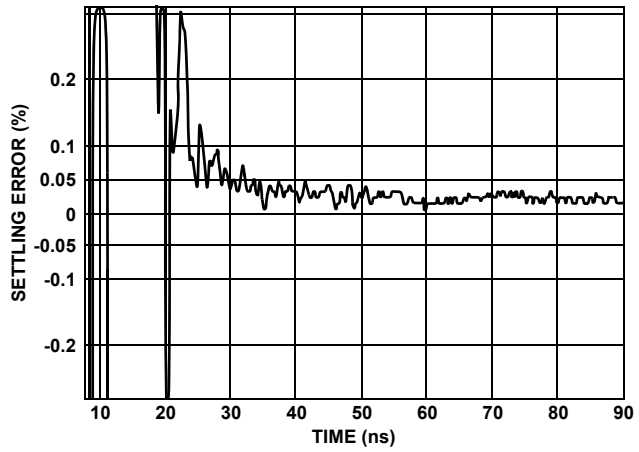


FIGURE 33. SETTLING RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

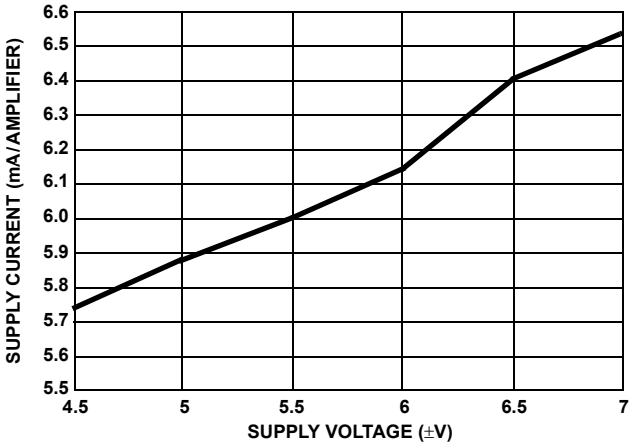


FIGURE 34. SUPPLY CURRENT vs SUPPLY VOLTAGE

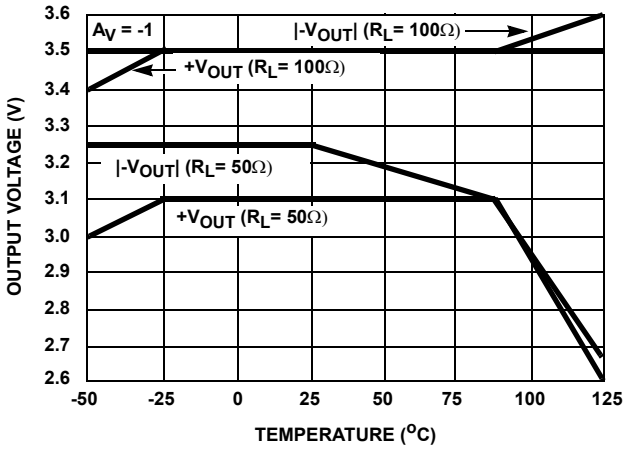


FIGURE 35. OUTPUT VOLTAGE vs TEMPERATURE

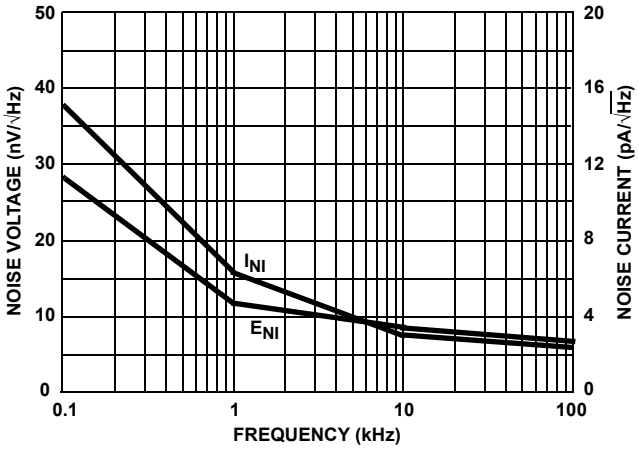
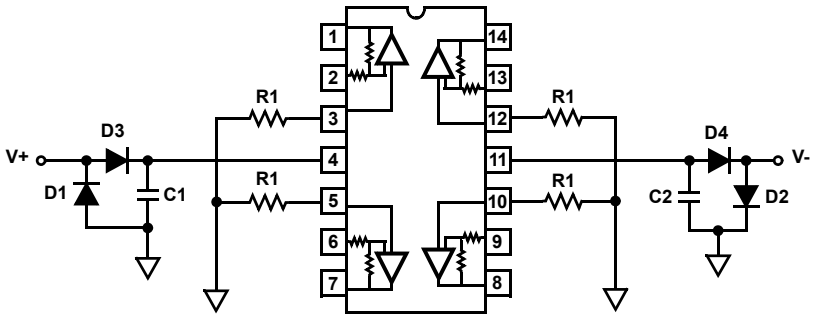


FIGURE 36. INPUT NOISE CHARACTERISTICS

Burn-In Circuit

HS-1412RH CERDIP

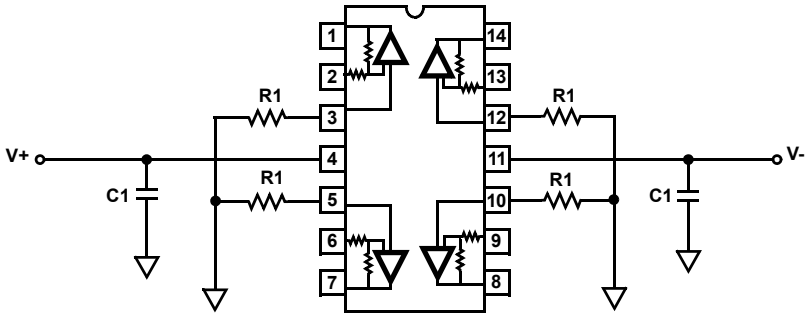


NOTES:

1. R1 = 1kΩ, ±5%, 1/4W [Per Socket].
2. C1 = C2 = 0.01μF [Per Socket] or 0.1μF (Per Row) Minimum.
3. D1 = D2 = 1N4002 or Equivalent [Per Board].
4. D3 = D4 = 1N4002 or Equivalent [Per Socket].
5. (-V) + (+V) = 11V ±1.0V.
6. 20mA < (I_{CC}, I_{EE}) < 32mA.
7. -50mV < V_{OUT} < +50mV.

Irradiation Circuit

HS-1412RH CERDIP



NOTES:

8. R1 = 1kΩ ±5%
9. C1 = 0.1μF
10. V+ = +5.0V ±0.5V
11. V- = -5.0V ±0.5V

Die Characteristics

DIE DIMENSIONS:

79 mils x 118 mils x 19 mils
(2000µm x 3000µm x 483µm)

INTERFACE MATERIALS:

Glassivation:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

Top Metallization:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Thickness: Metal 2: 16kÅ ±0.8kÅ

Substrate:

UHF-1X. Bonded Wafer, DI

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential (Powered Up)**:**

Floating (Recommend Connection to V-)

ADDITIONAL INFORMATION:

Transistor Count:

320

Metallization Mask Layout

HS-1412RH