XRT71D00

DS3/E3 JITTER ATTENUATOR IC

OCTOBER 1999 *REV. 1.0.6*

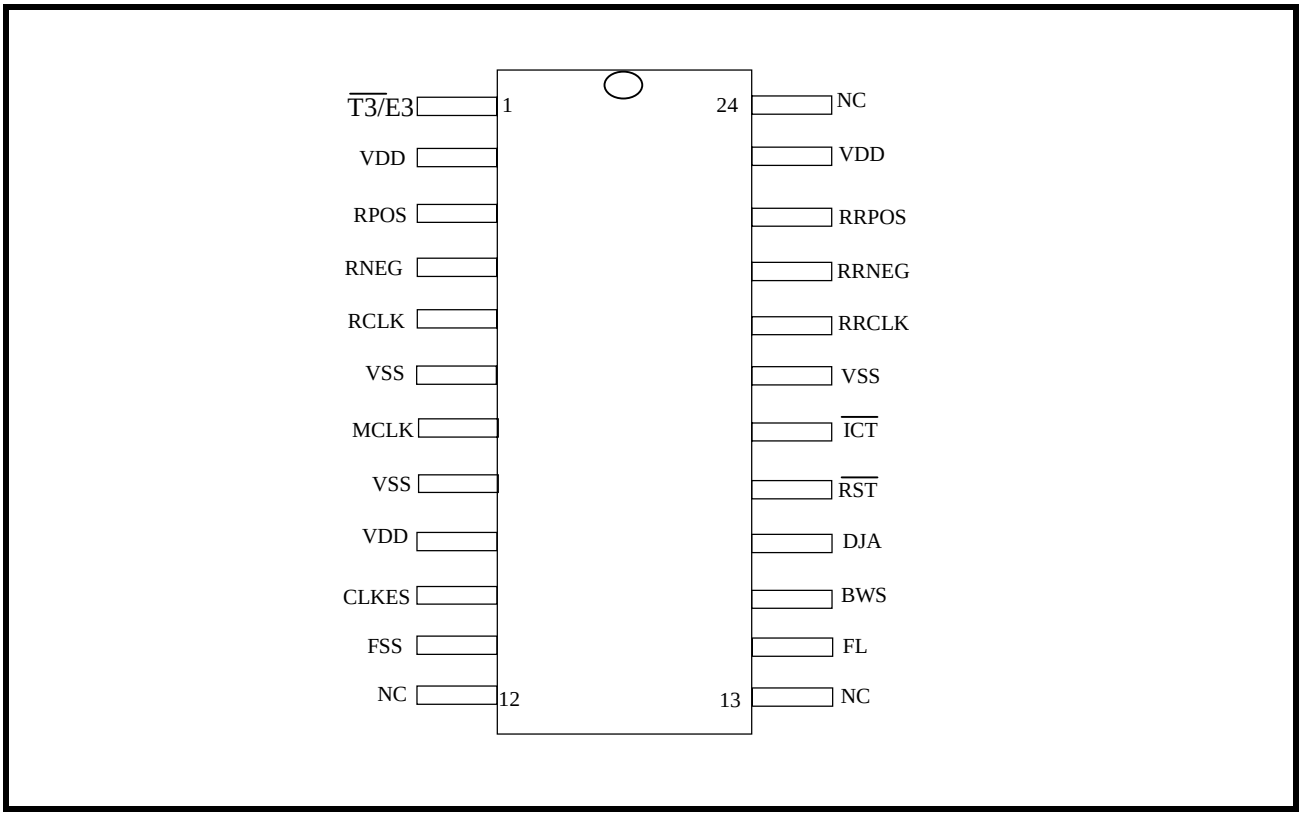
FEATURES

- A single-chip that does the following:
- Accepts “jittery” clock and data from an LIU IC
- Internally reduces the jitter of this clock and data signal.
- Outputs this “smoothed” data to the Terminal Equipment.
- Attenuates clock and data jitter present in DS3 or E3 systems
- No external component required
- Compliance with jitter transfer template outlined in ITU G.751, G.752, G.755
- and GR-499-CORE,1995 standards
- Meets output jitter generation requirement as specified by ETSI TBR24
- Selectable buffer size of 16 and 32 bits
- Jitter attenuator can be easily disabled
- Available in a 24 pin SOIC or 32 pin TQFP package.
- Single 3.3V or 5.0V supply.

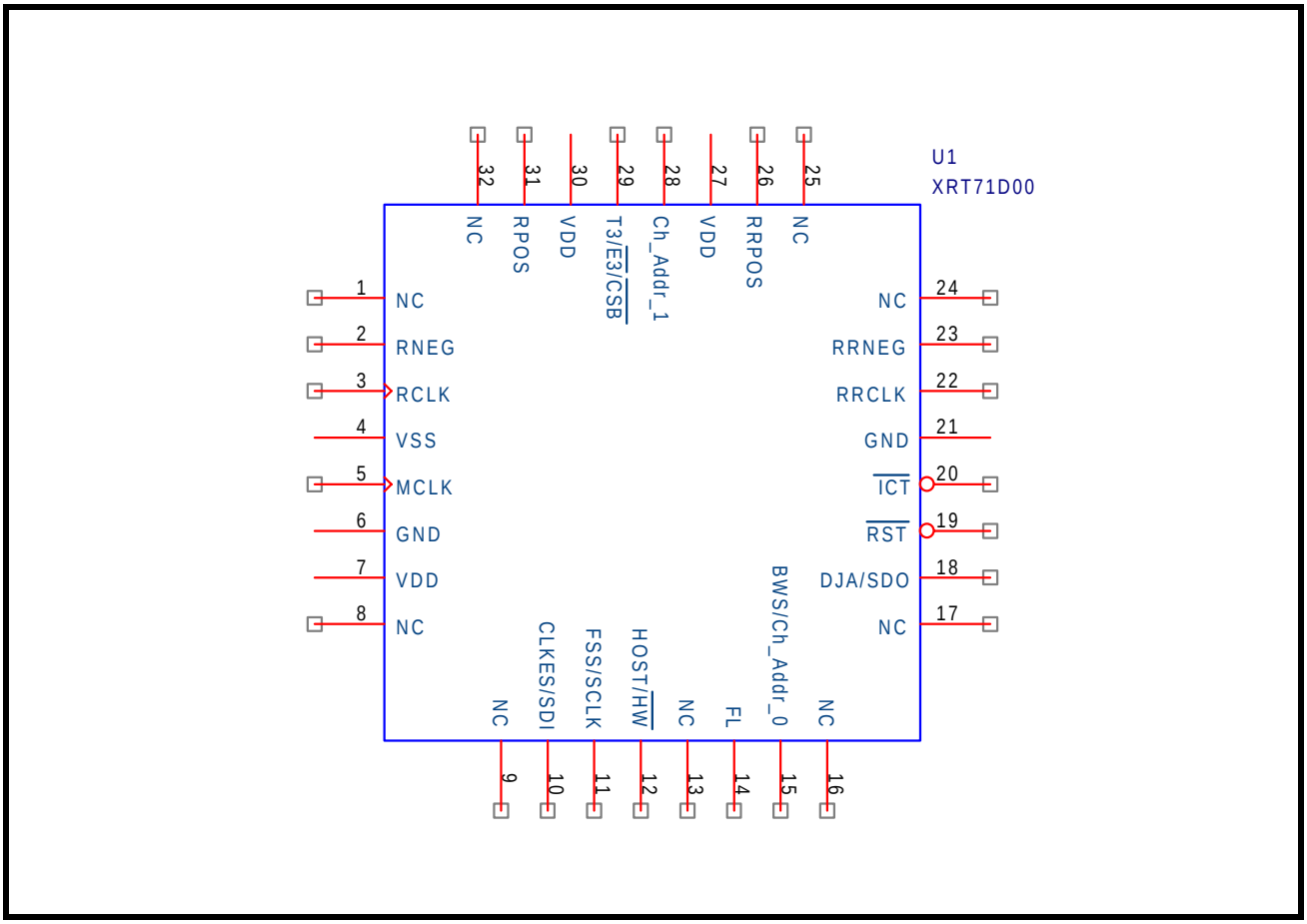
APPLICATIONS

- ETSI TBR24 34Mbit/s D34U and D34S system
- DS3/E3 Digital Multiplex and De-multiplex Equipment
- DS3 and E3 Line Interface
- PCM Test Equipment

PIN CONFIGURATION (for the 24 Pin SOIC Package)



PIN OUT CONFIGURATION (32 Pin TQFP)



PIN DESCRIPTION (24 Pin SOIC Package)

PIN #	SYMBOL	TYPE	DESCRIPTION
1	E3/DS3* (CSB*)	I	**T3/E3 Select Input/Chip Select Input:** The exact functionality of this input pin depends upon whether the XRT71D00 device has been configured to operate in the “Host” or “Hardware” Mode. **Hardware Mode—E3/DS3* Select Input:** Connect this pin low to select T3 and high to select E3 operation. **HOST Mode—Chip Select Input:** The Local Microprocessor must assert this pin (e.g., set it to “0”) in order to enable communication with the XRT7300, via the Microprocessor Serial Interface. (Note: This pin is internally pulled “high”.)
2	VDD	—	**Digital Positive Supply.** 3.3V or 5.0V +/-5%

PIN DESCRIPTION (24 Pin SOIC Package) (Cont'd)

PIN #	SYMBOL	TYPE	DESCRIPTION
3	RPOS	I	**Receive Positive Data (Jittery) Input.** Data that is input on this pin is sampled on either the rising or falling edge of RCLK depending on the setting of the **CLKES** pin (pin 10). If CLKES is "high", then RPOS will be sampled on the falling edge of RCLK. If CLKES is "low", then RPOS will be sampled on the rising edge of RCLK. This pin is typically tied to the "RPOS" output pin of the LIU IC.
4	RNEG	I	**Receive Negative Data (Jittery) Input.** Data that is input on this pin is sampled on either the rising or falling edge of RCLK depending on the setting of the **CLKES** pin (pin 10). If CLKES is "high", then RNEG will be sampled on the falling edge of RCLK. If CLKES is "low", then RPOS will be sampled on the rising edge of RCLK. This pin is typically tied to the "RNEG" output pin of the LIU IC.
5	RCLK	I	**Receive Clock (Jittery) Input.** This is input that the user should route the "jittery" 44.736MHz or 34.368MHz clock signal (from the LIU IC). This pin is typically tied to the "RCLK" output pin of the LIU IC.
6	VSS	—	**Digital Ground.** 0.0V
7	MCLK	I	**Master Clock Input.** Reference clock for internal PLL. 44.736MHz+/-20ppm or 34.368MHz+/-20ppm. This clock must be continuous and jitter free with duty cycle between 30 to 70%. **Note:** It is permissible to use either the EXCLK signal or TCLK signals (which are applied to the XRT7300 LIU IC).
8	VSS	—	**Analog Ground.** 0.0V
9	VDD	—	**Analog Positive Supply.** 3.3V or 5.0V +/-5%
10	CLKES/ SDI	I	**Clock Edge Select Input/Serial Data Input Pin.** The exact functionality of this input pin depends upon whether the XRT71D00 device is configured to operate in the "HOST" or "Hardware" Mode. **Hardware Mode—Clock Edge Select Input** The status of this pin determines the sampling edge on **RCLK** to **RPOS/RNEG** and **RRPOS/RRNEG** data update on **RRCLK** edge. When high: **RPOS/RNEG** is sampled on falling edge of **RCLK** and **RRPOS/RRNEG** is updated on rising edge of **RRCLK**. When low: **RPOS/RNEG** is sampled on rising edge of **RCLK** and **RRPOS/RRNEG** is updated on falling edge of **RRCLK**. **Host Mode—Serial Data Input** Whenever the user wishes to read or write data into the Command Registers, over the Microprocessor Serial Interface; the user is expected to apply the "Read/Write" bit, the Address Values (of the Command Registers) and Data Value to be written (during "Write" Operations) to this pin. This input will be sampled on the rising edge of the SCLK pin (pin 11).

PIN DESCRIPTION (24 Pin SOIC Package) (Cont'd)

PIN #	SYMBOL	TYPE	DESCRIPTION
11	FSS/ SCLK	I	**Fifo Size Select Input/Serial Clock Input.** The exact functionality of this input pin depends upon whether the XRT71D00 device is operating in the Hardware of the Host Mode. **Hardware Mode—FIFO Size Select Input** When high: Selects 32 bits FIFO. When low: Selects 16 bits FIFO. **Host Mode—Microprocessor Serial Interface Clock Signal** This signal will be used to (1) sample the data, on the SDI pin, on the rising edge of this signal. Additionally, during "Read" operations, the Microprocessor Serial Interface will update the SDO output on the falling edge of this signal.
12	HOST/HW*	—	**Host/HW* Mode Select:** This input pin permits the user to enable or disable the Microprocessor Serial Interface (e.g., consisting of the SDI, SDO, SCLK, CSB and REG_RESET* pins). Setting this input pin "high" enables the Microprocessor Serial Interface (or configures the XRT71D00 device to operate in the "Host" Mode). In this mode, the user is expected to configure the XRT71D00 device by writing data into the "on-chip" Command Register via the Microprocessor Serial Interface. As a consequence, when the XRT71D00 is operating in the "Host" Mode, then it will ignore the states of many of the discrete input pins. Setting this input pin "low" disables the Microprocessor Serial Interface (e.g., configures the XRT71D00 device to operate in the "Hardware" Mode). In this mode, many of the external input control pins will be functional.
13	NC	—	**No Connect.**
14	FL	O	**FIFO Full/Empty Alarm Output indicator.** This output pin is driven high whenever the internal FIFO comes within two-bits of either being completely empty or completely full. Whenever the "FIFO Full" or "FIFO Empty" alarm occurs, then the bandwidth of the PLL will open up and Jitter Attenuation (within the chip) will be disabled The purpose of this feature is to prevent the loss of data. When this output pin is asserted, it will be driven "high" for at least 1 RRCLK cycle wide.
15	BWS/ (Ch_Addr_0)	I	**Bandwidth Select Input/Channel Addr_0 Assignment Input.** The exact functionality of this input pin depends upon whether the XRT71D00 device is operating in the Hardware Mode or in the "Host Mode". **Hardware Mode—Bandwidth Select Input:** Connect this pin high to select wide jitter transfer bandwidth, and connect low to select narrow jitter transfer bandwidth. **Note:** The exact jitter transfer bandwidths (that will be configured for either of these settings), will be defined in the next revision of this data sheet. **Host Mode—Channel_Addr_0 Assignment Input:** This input pin, along with pin 24 permits the user to assign a "Channel Address" to the XRT71D00 device.

PIN DESCRIPTION (24 Pin SOIC Package) (Cont'd)

PIN #	SYMBOL	TYPE	DESCRIPTION
16	DJA (SDO)	I(O)	**Disable Jitter Attenuator Input/Serial Data Output pin:** The exact functionality of this input pin depends upon whether the XRT71D00 device is operating in the "Hardware" or "Host" Mode. **Hardware Mode—Disable Jitter Attenuator Input pin:** This input permits the user to enable or disable the Jitter Attenuator IC. When this input pin "high", the data and clock signals, that enter the chip via the RPOS/RRNEG and RCLK input pins are passed directly to RRPOS,RRNEG and RRCLK, without any jitter attenuation. **Host Mode—Serial Data Output pin:** This pin will serially output the contents of the specified Command Register, during "Read" Operations. The data, on this pin, will be updated on the falling edge of the SCLK input signal. This pin will be tri-stated upon completion of data transfer. **Note:** The user is advised to tie this pin to GND, if the XRT71D00 device has been configured to operate in the "HOST" Mode.
17	RST	I	**Reset Input. (Active-Low)** A high-low transition will re-center the internal FIFO, and will clear the Command Registers (for Host Mode operation). Reset this pin may corrupt data within the device. **Note:** For normal operation, the user should pull this pin to VDD.
18	ICT	I	**In Circuit Testing Input.** Active low. With this pin tied to ground, all output pins will be in high impedance mode for in-circuit-testing. For normal operation this input pin should be tied to VDD.
19	VSS	—	**Digital Ground.** 0.0V
20	RRCLK	O	**Receive Output (De-jittered) Clock.** This is the pin, that the "smoothed" (e.g., de-jittered) 44.736MHz or 34.368MHz clock signal will be output from. Further, this clock signal is also used to clock out the contents of the "Recovered" data (via the RRPOS and RRNEG output pins). If CLKES is "low", then the XRT71D00 device will output data, via the RRPOS and RRNEG output pin, upon the falling edge of this clock signal. If CLKES is "high", then the XRT71D00 device will output data, via the RRPOS and RRNEG output pin, upon the rising edge of this clock signal.
21	RRNEG	O	**Receive Negative Data (De-Jittered) Output.** De-jittered negative data output. Updated on the rising or falling edge of RRCLK(see pin 9), depending upon the state of the CLKES input pin (or bit-field setting). If CLKES is "low", then the XRT71D00 device will output data via this pin, upon the falling edge of the RRCLK clock signal. If CLKES is "high", then the XRT71D00 device will output data via the pin, upon the rising edge of the RRCLK clock signal.
22	RRPOS	O	**Receive Positive Data (De-Jittered) Output.** De-jittered positive data output. Updated on the rising or falling edge of RRCLK(see pin 9), depending upon the state of the CLKES input pin (or bit-field setting). If CLKES is "low", then the XRT71D00 device will output data via this pin, upon the falling edge of the RRCLK clock signal. If CLKES is "high",. then the XRT71D00 device will output data via this pin, upon the rising edge of the RRCLK clock signal.

PIN DESCRIPTION (24 Pin SOIC Package) (Cont'd)

PIN #	SYMBOL	TYPE	DESCRIPTION
23	VDD	—	**Digital Positive Supply.** 3.3V or 5.0V +/-5%
24	NC (Ch_Addr_1)	—	**Channel Addr_1 Assignment Input.** This input pin, along with pin 15 permits the user to assign a "Channel Address" to the XRT71D00 device.

PIN DESCRIPTION (32 Pin TQFP Package)

PIN #	SYMBOL	TYPE	DESCRIPTION
1	NC	***	**Not Bonded Out**
2	RNEG	I	**Receive Negative Data (Jittery) Input.** Data that is input on this pin is sampled on either the rising or falling edge of RCLK depending on the setting of the CLKES pin (pin 10). If CLKES is "high", then RNEG will be sampled on the falling edge of RCLK. If CLKES is "low", then RPOS will be sampled on the rising edge of RCLK. This pin is typically tied to the "RNEG" output pin of the LIU IC.
3	RCLK	I	**Receive Clock (Jittery) Input.** This is input that the user should route the "jittery" 44.736MHz or 34.368MHz clock signal (from the LIU IC). This pin is typically tied to the "RCLK" output pin of the LIU IC.
4	GND	***	
5	MCLK	I	**Master Clock Input.** Reference clock for internal PLL. 44.736MHz+/-20ppm or 34.368MHz+/-20ppm. This clock must be continuous and jitter free with duty cycle between 30 to 70%. **Note:** It is permissible to use either the EXCLK signal or TCLK signals (which are applied to the XRT7300 LIU IC).
6	GND	***	Analog Ground pin
7	VDD	***	Analog VDD Pin: 3.3V or 5.0V ± 5%
8	NC	***	**Not Bonded Out**
9	NC	***	**Not Bonded Out**

PIN DESCRIPTION (32 Pin TQFP Package) (Cont'd)

PIN #	SYMBOL	TYPE	DESCRIPTION
10	CLKES/(SDI)	I	**Clock Edge Select Input/Serial Data Input Pin.** The exact functionality of this input pin depends upon whether the XRT71D00 device is configured to operate in the "HOST" or "Hardware" Mode. **Hardware Mode—Clock Edge Select Input** The status of this pin determines the sampling edge on RCLK to RPOS/RNEG and RRPOS/RRNEG data update on RRCLK edge. When high: **RPOS/RNEG** is sampled on falling edge of **RCLK** and **RRPOS/RRNEG** is updated on rising edge of **RRCLK**. When low: **RPOS/RNEG** is sampled on rising edge of **RCLK** and **RRPOS/RRNEG** is updated on falling edge of **RRCLK**. **Host Mode—Serial Data Input** Whenever the user wishes to read or write data into the Command Registers, over the Microprocessor Serial Interface; the user is expected to apply the "Read/Write" bit, the Address Values (of the Command Registers) and Data Value to be written (during "Write" Operations) to this pin. This input will be sampled on the rising edge of the SCLK pin (pin 11).
11	FSS/(SCLK)	I	**Fifo Size Select Input/Serial Clock Input.** The exact functionality of this input pin depends upon whether the XRT71D00 device is operating in the Hardware of the Host Mode. **Hardware Mode—FIFO Size Select Input** When high: Selects 32 bits FIFO. When low: Selects 16 bits FIFO. **Host Mode—Microprocessor Serial Interface Clock Signal** This signal will be used to (1) sample the data, on the SDI pin, on the rising edge of this signal. Additionally, during "Read" operations, the Microprocessor Serial Interface will update the SDO output on the falling edge of this signal.
12	HOST/HW*		**Host/HW* Mode Select:** This input pin permits the user to enable or disable the Microprocessor Serial Interface (e.g., consisting of the SDI, SDO, SCLK, CSB and REG_RESET* pins). Setting this input pin "high" enables the Microprocessor Serial Interface (or configures the XRT71D00 device to operate in the "Host" Mode). In this mode, the user is expected to configure the XRT71D00 device by writing data into the "on-chip" Command Register via the Microprocessor Serial Interface. As a consequence, when the XRT71D00 is operating in the "Host" Mode, then it will ignore the states of many of the discrete input pins. Setting this input pin "low" disables the Microprocessor Serial Interface (e.g., configures the XRT71D00 device to operate in the "Hardware" Mode). In this mode, many of the external input control pins will be functional.
13	NC	***	**Not Bonded Out**
14	FL	O	**FIFO Full/Empty Alarm Output indicator.** This output pin is driven high whenever the internal FIFO comes within two-bits of either being completely empty or completely full. Whenever the "FIFO Full" or "FIFO Empty" alarm occurs, then the bandwidth of the PLL will open up and Jitter Attenuation (within the chip) will be disabled The purpose of this feature is to prevent the loss of data. When this output pin is asserted, it will be driven "high" for at least 1 RRCLK cycle wide.

PIN DESCRIPTION (32 Pin TQFP Package) (Cont'd)

PIN #	SYMBOL	TYPE	DESCRIPTION
15	BWS/ Ch_Add_0	I	**Bandwidth Select Input/Channel Addr_0 Assignment Input.** The exact functionality of this input pin depends upon whether the XRT71D00 device is operating in the Hardware Mode or in the "Host Mode". **Hardware Mode—Bandwidth Select Input:** Connect this pin high to select wide jitter transfer bandwidth, and connect low to select narrow jitter transfer bandwidth. **Note:** The exact jitter transfer bandwidths (that will be configured for either of these settings), will be defined in the next revision of this data sheet. **Host Mode—Channel_Addr_0 Assignment Input:** This input pin, along with pin 24 permits the user to assign a "Channel Address" to the XRT71D00 device.
16	NC	***	**Not Bonded Out**
17	NC	***	**Not Bonded Out**
18	DJA/ (SDO)	I/(O)	**Disable Jitter Attenuator Input/Serial Data Output pin:** The exact functionality of this input pin depends upon whether the XRT71D00 device is operating in the "Hardware" or "Host" Mode. **Hardware Mode—Disable Jitter Attenuator Input pin:** This input permits the user to enable or disable the Jitter Attenuator IC. When this input pin "high", the data and clock signals, that enter the chip via the RPOS/RRNEG and RCLK input pins are passed directly to RRPOS,RRNEG and RRCLK, without any jitter attenuation. **Host Mode—Serial Data Output pin:** This pin will serially output the contents of the specified Command Register, during "Read" Operations. The data, on this pin, will be updated on the falling edge of the SCLK input signal. This pin will be tri-stated upon completion of data transfer. **Note:** The user is advised to tie this pin to GND, if the XRT71D00 device has been configured to operate in the "HOST" Mode.
19	RST*	I	**Reset Input.** (Active-Low) A high-low transition will re-center the internal FIFO, and will clear the Command Registers (for Host Mode operation). Reset this pin may corrupt data within the device. **Note:** For normal operation, the user should pull this pin to VDD.
20	ICT*	I	**In Circuit Testing Input.** Active low. With this pin tied to ground, all output pins will be in high impedance mode for in-circuit-testing. For normal operation this input pin should be tied to VDD.
21	GND	***	
22	RRCLK	O	**Receive Output (De-jittered) Clock.** This is the pin, that the "smoothed" (e.g., de-jittered) 44.736MHz or 34.368MHz clock signal will be output from. Further, this clock signal is also used to clock out the contents of the "Recovered" data (via the RRPOS and RRNEG output pins). If CLKES is "low", then the XRT71D00 device will output data, via the RRPOS and RRNEG output pin, upon the falling edge of this clock signal. If CLKES is "high", then the XRT71D00 device will output data, via the RRPOS and RRNEG output pin, upon the rising edge of this clock signal.

PIN DESCRIPTION (32 Pin TQFP Package) (Cont'd)

PIN #	SYMBOL	TYPE	DESCRIPTION
23	RRNEG	O	**Receive Negative Data (De-Jittered) Output.** De-jittered negative data output. Updated on the rising or falling edge of RRCLK (see pin 9), depending upon the state of the CLKES input pin (or bit-field setting). If CLKES is "low", then the XRT71D00 device will output data via this pin, upon the falling edge of the RRCLK clock signal. If CLKES is "high", then the XRT71D00 device will output data via the pin, upon the rising edge of the RRCLK clock signal.
24	NC	***	**Not Bonded Out**
25	NC	***	**Not Bonded Out**
26	RRPOS	O	**Receive Positive Data (De-Jittered) Output.** De-jittered positive data output. Updated on the rising or falling edge of RRCLK (see pin 9), depending upon the state of the CLKES input pin (or bit-field setting). If CLKES is "low", then the XRT71D00 device will output data via this pin, upon the falling edge of the RRCLK clock signal. If CLKES is "high",. then the XRT71D00 device will output data via this pin, upon the rising edge of the RRCLK clock signal.
27	VDD	***	
28	Ch_Addr_1	I	**Channel Addr_1 Assignment Input.** This input pin, along with pin 15 permits the user to assign a "Channel Address" to the XRT71D00 device.
29	E3/DS3* (CSB)	I	**T3/E3 Select Input/Chip Select Input:** The exact functionality of this input pin depends upon whether the XRT71D00 device has been configured to operate in the "Host" or "Hardware" Mode. **Hardware Mode—E3/DS3* Select Input**: Connect this pin low to select T3 and high to select E3 operation. **HOST Mode—Chip Select Input:** The Local Microprocessor must assert this pin (e.g., set it to "0") in order to enable communication with the XRT7300, via the Microprocessor Serial Interface. (Note: This pin is internally pulled "high".)
30	VDD	***	
31	RPOS	I	**Receive Positive Data (Jittery) Input.** Data that is input on this pin is sampled on either the rising or falling edge of RCLK depending on the setting of the CLKES pin (pin 10). If CLKES is "high", then RPOS will be sampled on the falling edge of RCLK. If CLKES is "low", then RPOS will be sampled on the rising edge of RCLK. This pin is typically tied to the "RPOS" output pin of the LIU IC.
32	NC	***	**Not Bonded Out**

AC ELECTRICAL CHARACTERISTICS

Microprocessor Serial Interface Timing (see Figure 4)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS.
t_{21}	CSB Low to Rising Edge of SCLK Setup Time	50			ns
t_{22}	SCLK to CSB Hold Time	20			ns
t_{23}	SDI to Rising Edge of SCLK Setup Time	50			ns
t_{24}	SDI to Rising Edge of SCLK Hold Time	50			ns
t_{25}	SCLK “Low” Time	240			ns
t_{26}	SCLK “High” Time	240			ns
t_{27}	SCLK Period	500			ns
t_{28}	SCLK to CSB Hold Time	50			ns
t_{29}	CSB “Inactive” Time	250			ns
t_{30}	Falling Edge of SCLK to SDO Valid Time			200	ns
t_{31}	Falling Edge of SCLK to SDO Invalid Time			100	ns
t_{32}	Falling Edge of SCLK, or rising edge of CSB to High Z		100		ns
t_{33}	Rise/Fall time of SDO Output			40	ns

DC ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{DD}=5.0V±5%, unless otherwise specified).

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{DD}	3.135	5.0	5.25	V
Input High Voltage	V_{IH}	2.0	—	5.25	V
Input Low Voltage	V_{IL}	-0.5	—	0.8	V
Output High Voltage @ I_{OH}=-5mA	V_{OH}	2.4	—	—	V
Output Low Voltage @ I_{OL}=5mA	V_{OL}	—	—	0.4	V
Input Leakage Current(except Input pins with Pull-up resistor.	I_L	—	—	± 10	µA
Input Capacitance	C_I	—	5.0	—	pF
Output Load Capacitance	C_L	—	—	25	pF

ABSOLUTE MAXIMUM RATINGS

Storage Temperature.....-65°C to + 150°C

Operating Temperature..... -40°C to + 85°C

ESD Rating..... >2500V on all pins

Supply Voltage.....-0.5V to + 6.0V

SYSTEM OVERVIEW

The XRT71D00 is a fully integrated and self contained DS3/E3 jitter attenuator designed to attenuate jitter the incoming clock and data in PCM system. The XRT71D00 device was designed to attenuate the jitter (of the incoming clock and data) such that the following specifications could be met.

- ETSI TBR 24
- ITU-T G.751
- ITU-T G.752
- ITU-T G.755
- Bellcore GR-499-CORE Category I and II Equipment Jitter Requirements.

Additionally, the XRT71D00 device can also be used to reduce and limit the amount of jitter, in the recovered line clock signal, in order to support loop-timing applications.

Figure 1 presents a simple block diagram of the XRT71D00 device, (when it is configured to operate in the “Hardware” Mode); and Figure 2 presents a simple block diagram of the XRT71D00 device, (when it is configured to operate in the “Host” Mode.

FIGURE 1. SIMPLE ILLUSTRATION OF THE XRT71D00 DS3/E3 JITTER ATTENUATOR DEVICE (WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE “HARDWARE” MODE)

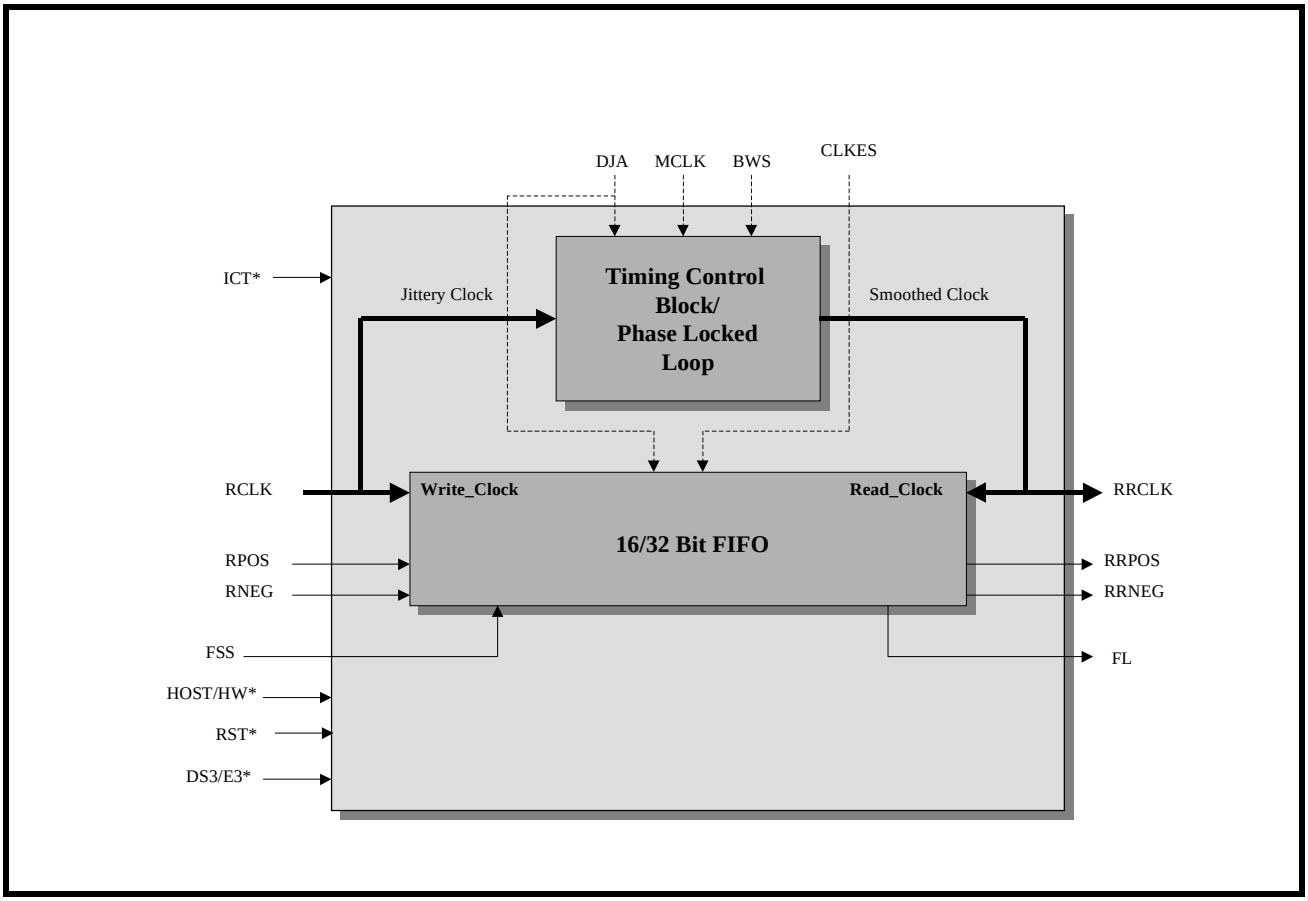
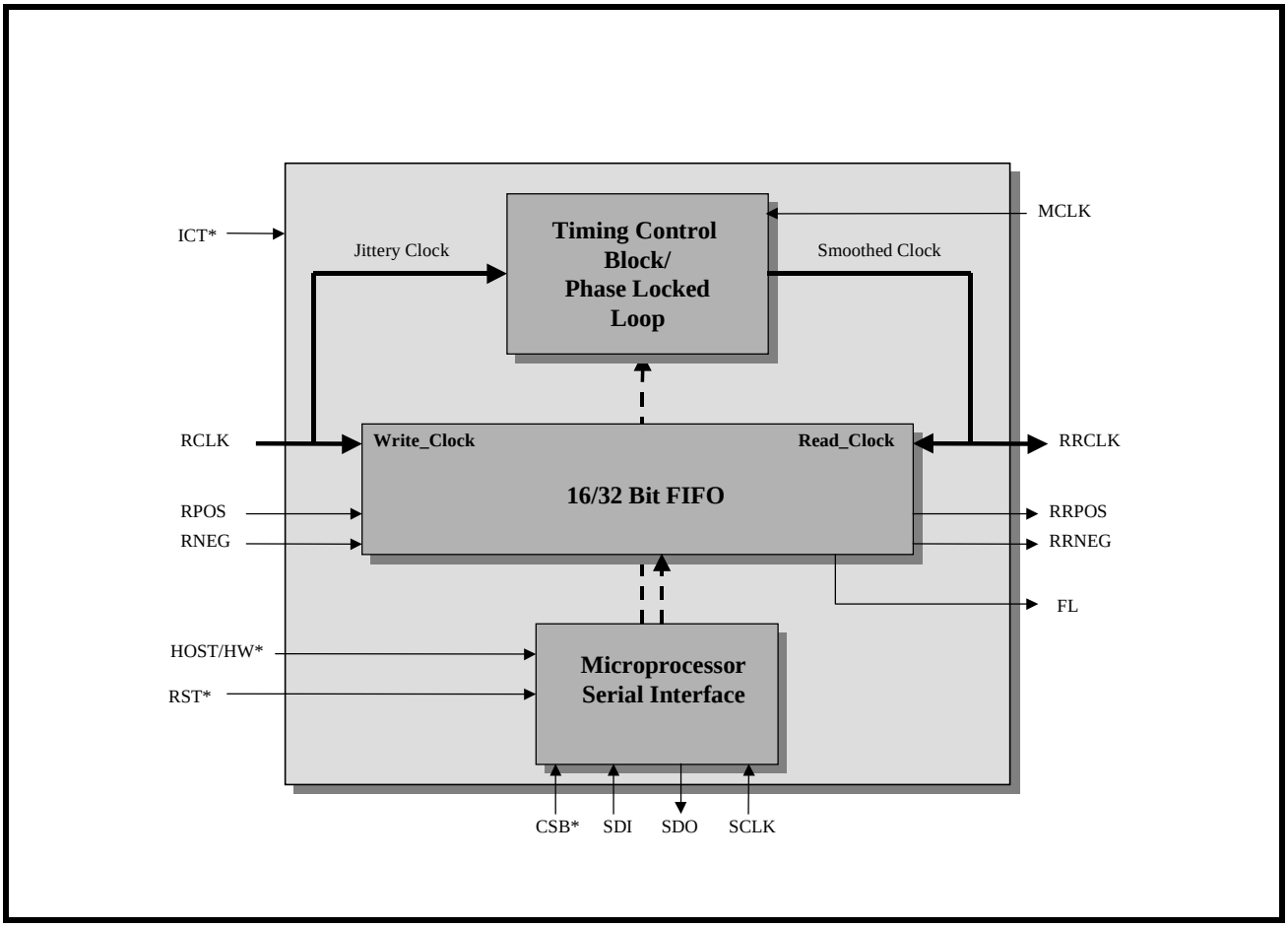


FIGURE 2. SIMPLE ILLUSTRATION OF THE XRT71D00 DS3/E3 JITTER ATTENUATOR DEVICE (WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE "HOST" MODE).



The XRT71D00 DS3/E3 Jitter Attenuator IC consists of the following functional blocks:

- Timing Control Block
- The "Jitter-Attenuator" PLL
- The "2-Channel 16/32 Bit FIFO".

Background Information

In PCM systems, jitter is defined as the instantaneous variation of data edges compared to a perfect clock. Jitter on incoming data can occur due to any of the following sources:

1. The pattern of the incoming line signal
2. Imperfect timing recovery circuit in the system.
3. Cross-talk Noise
4. Inter-Symbol Interference/Signal Distortion

Principle of Operation

The XRT71D00 DS3/E3 Jitter Attenuator accepts a "jittery" clock and data from an LIU IC; via the RCLK, RPOS and RNEG input pins. This "jittery" recovered data is clocked into the "16/32 bit FIFO" via the "jittery clock" signal (at the RCLK input pin). In parallel, this same jittery clock signal is also input into the "Jitter Attenuator PLL". The "Jitter Attenuator PLL" is a "Narrow-Band" PLL that is used to:

1. Track the jittery RCLK signal, (from the LIU IC); and
2. To regenerate this signal (with considerably less jitter).

In Figures 1 and 2, this "de-jittered" clock is labeled "Smoothed Clock". This "Smoothed Clock" is now used to "Read Out" the "Recovered Data" from the 16/32 bit FIFO. This "Smoothed Clock" will also be output (to the Terminal Equipment) via the "RRCLK"

output pin. Likewise, the “Smoothed Recovered Data” will output (to the Terminal Equipment) via the RRPOS and RRNEG output pins.

The XRT71D00 device is designed to work as a companion device with XRT7300 (STS-1/DS3/E3) Line Interface Unit.

In order to recover the data correctly by the receiver and to satisfy input jitter tolerance, the clock recovery circuit inside the Line Interface Unit such as XRT7300 must have enough bandwidth to truck the incoming data timing variation. As a result, the recovered.

clock will be jittery and is not suitable to be used as a transmit clock source in looped-time mode situation. In particular, with E3 system, TBR24 specifies the maximum output jitter must be no more than 0.4UIpp when measured between 100Hz to 800KHz. This means a jitter attenuator with bandwidth less than 100Hz is required to be compliance with the standard in looped-timing. ITU G.751 is another application where low bandwidth jitter attenuator is needed to smooth the gapped clock output in the de-multiplexer system.

The Microprocessor Serial Interface

The XRT71D00 device can be configured to operate in either the “Hardware” Mode or in the “Host” Mode. Each of these modes will be discussed below.

The Hardware Mode

The XRT71D00 device can be configured to operate in the “Hardware Mode” by tying the “Host/HW*” input pin (pin 12) to GND.

When the XRT71D00 device is operating in the “Hardware Mode”, then the following is true.

1. The Microprocessor Serial Interface block is disabled.
2. The XRT71D00 device is configured via input pin settings.

Each of the pins associated with the Microprocessor Serial Interface will take on their alternative role, as defined below.

TABLE 1: ROLE OF MICROPROCESSOR SERIAL INTERFACE PINS WHEN THE XRT71D00 DEVICE IS OPERATING IN THE “HARDWARE” MODE.

PIN NUMBER (32 PIN TQFP)	PIN NUMBER (24 PIN SOIC)	PIN NAME	FUNCTION, WHILE IN THE HARDWARE MODE
10	10	CLKES (SDI)	CLKES
11	11	FSS (SCLK)	FSS
15	15	BWS/Ch_Add_0	BWS
18	16	DJA/(SDO)	DJA
28	24	Ch_Addr_1	None
29	1	E3/DS3* (CSB)	E3/DS3*

The Host Mode

The XRT71D00 device can be configured to operate in the “Host” Mode by tying the “Host/HW*” input pin (pin 12) to VDD.

When the XRT71D00 is operating in the “Host Mode”, then the following is true.

1. The Microprocessor Serial Interface block is enabled. Many configuration selections are made by writing the appropriate data into on-chip command Registers via the Microprocessor Serial Interface.

The Microprocessor Serial Interface

The XRT71D00 DS3/E3 Jitter Attenuator IC permits the user to have access to the “on-chip” Command Registers. Through these Command Registers, the user can configure the XRT71D00 device into a wide-variety of modes. This section discusses the following:

1. The description of the Command Registers.
2. A description on how to use the Microprocessor Serial Interface.

Description of the Command Registers

A listing of these Command Registers, their Addresses, and their bit-formats are listed below in Table 2.

TABLE 2: ADDRESSES AND BIT FORMATS OF THE XRT71D00 COMMAND REGISTERS

					REGISTER BIT-FORMAT				
ADDRESS	COMMAND REGISTER	CH_ADDR_1	CH_ADDR_0	TYPE	D4	D3	D2	D1	D0
0x05	CR5	0	0	R/W	E3/DS3*	DJA	BWS	CLKES	FSS
0x0D	CR13	0	1	R/W	E3/DS3*	DJA	BWS	CLKES	FSS
0x15	CR21	1	0	R/W	E3/DS3*	DJA	BWS	CLKES	FSS

Some of the fields within Table 2 deserve some explanation. The Microprocessor Serial Interface was designed such that the XRT71D00 device could be operated in conjunction with other Exar LIU ICs, as described below.

- A Microprocessor can configure both the XRT7300 DS3/E3/STS-1 LIU IC and a single XRT71D00 device via a single CSB*, SDI, SDO and SCLK input and output pins.
- A Microprocessor can configure both the XRT7302 Dual Channel DS3/E3/STS-1 LIU IC and two XRT71D00 devices (one associated with each channel of the XRT7302 device) via a single CSB*, SDI, SDO and SCLK input and output pins.
- A Microprocessor can configure both the XRT73L03 Triple Channel DS3/E3/STS-1 LIU IC and three XRT71D00 devices (one associated with each channel of the XRT73L03 device) via a single CSB*, SDI, SDO and SCLK input and output pins.

Operating the Microprocessor Serial Interface.

The XRT7300 Serial Interface is a simple four-wire interface that is compatible with many of the microcontrollers available in the market. This interface consists of the following signals:

CSB—Chip Select (Active Low)

SCLK—Serial Clock

SDI—Serial Data Input

SDO—Serial Data Output

Using the Microprocessor Serial Interface

The following instructions, for using the Microprocessor Serial Interface, are best understood by referring to the diagram in Figure 3.

In order to use the Microprocessor Serial Interface the user must first provide a clock signal to the SCLK input pin. Afterwards, the user will initiate a “Read” or “Write” operation by asserting the “active-low” Chip Select input pin (CSB). It is important to assert the CSB pin (e.g., toggle it “low”) at least 50ns prior to the very first rising edge of the clock signal.

Once the CSB input pin has been asserted the type of operation and the target register address must now be specified by the user. The user provides this information to the Microprocessor Serial Interface by writing eight serial bits of data into the SDI input. Note: each of these bits will be “clocked” into the SDI input, on the rising edge of SCLK. These eight bits are identified and described below.

Bit 1—“R/W” (Read/Write) Bit

This bit will be clocked into the SDI input, on the first rising edge of SCLK (after CSB has been asserted). This bit indicates whether the current operation is a “Read” or “Write” operation. A “1” in this bit specifies a “Read” operation; whereas, a “0” in this bit specifies a “Write” operation.

Bits 2 through 5—The four (4) bit Address Values (labeled A0, A1, A2 and A3)

The next four rising edges of the SCLK signal will clock in the 4-bit address value for this particular Read (or Write) operation. The address selects the Command Register, within the XRT7300 device that the user will either be reading data from, or writing data to. The user must supply the address bits to the SDI input pin, in ascending order with the LSB (least significant bit) first.

Bits 6 and 7

The next two bits, A4 and A5 must be set to “0”, as shown in Figure 23.

Bit 8—A6

The value of “A6” is a “don’t care”.

Once these first 8 bits have been written into the Microprocessor Serial Interface, the subsequent action depends upon whether the current operation is a “Read” or “Write” operation.

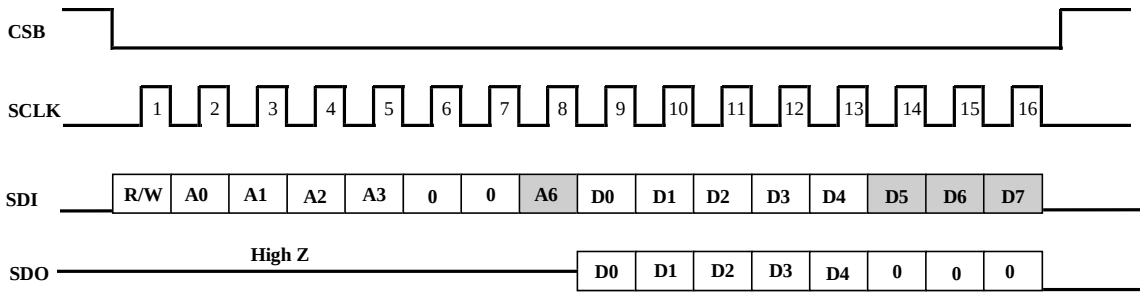
Read Operation

Once the last address bit (A3) has been clocked into the SDI input, the “Read” operation will proceed through an idle period, lasting three SCLK periods. On the falling edge of SCLK Cycle #8 (see Figure 3) the serial data output signal (SDO) becomes active. At this point the user can begin reading the data contents of the addressed Command Register (at Address [A3, A2, A1, A0]) via the SDO output pin. The Microprocessor Serial Interface will output this five bit data word (D0 through D4) in ascending order (with the LSB first), on the falling edges of the SCLK pin. As a consequence, the data (on the SDO output pin) will be sufficiently stable for reading (by the Microprocessor), on the very next rising edge of the SCLK pin.

Write Operation

Once the last address bit (A3) has been clocked into the SDI input, the “Write” operation will proceed through an idle period, lasting three SCLK periods. Prior to the rising edge of SCLK Cycle # 9 (see Figure 3) the user must begin to apply the eight bit data word, that he/she wishes to write to the Microprocessor Serial Interface, onto the SDI input pin. The Microprocessor Serial Interface will latch the value on the SDI input pin, on the rising edge of SCLK. The user must apply this word (D0 through D7) serially, in ascending order with the LSB first.

FIGURE 3. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



Note:

A4 and A5 are always “0”.

R/W = “1” for “Read” Operations

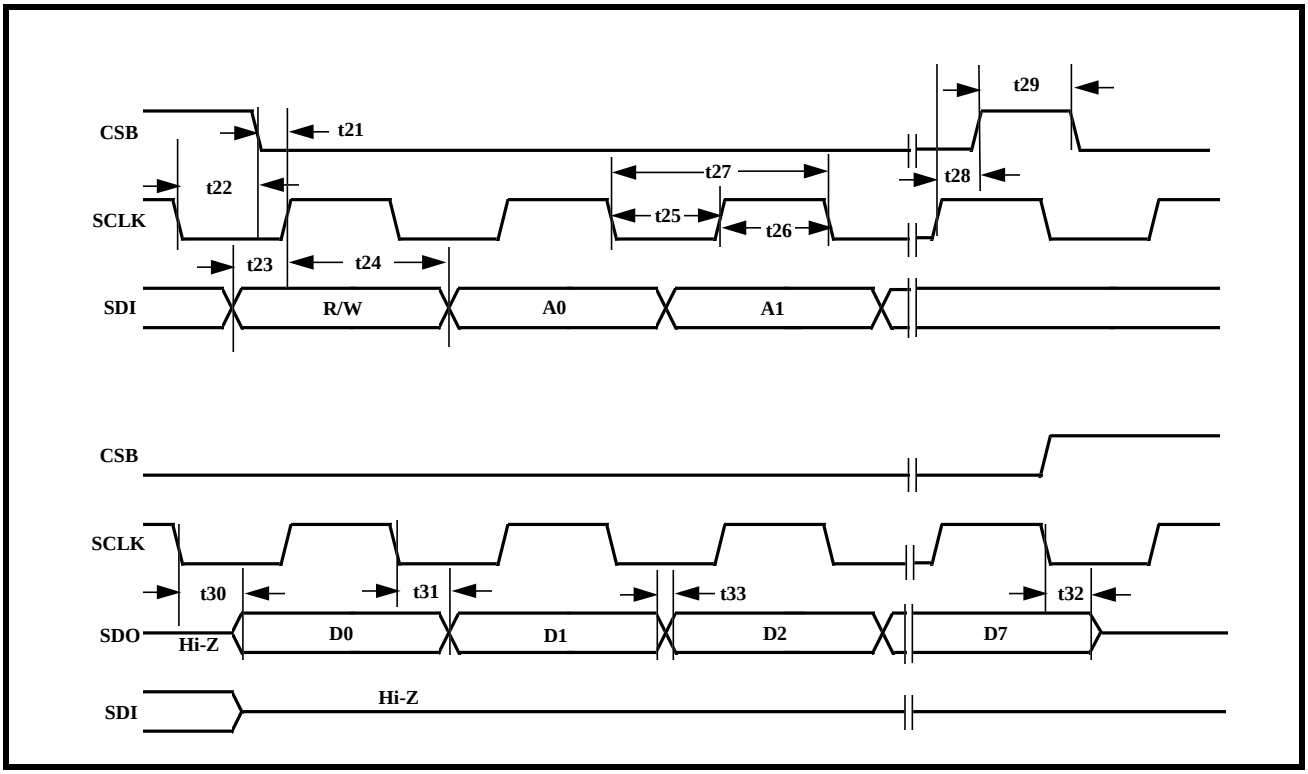
R/W = “0” for “Write” Operations

Denotes a “don’t care” value (shaded areas)

Simplified Interface Option

The user can simplify the design of the circuitry connecting to the Microprocessor Serial Interface by tying both the SDO and SDI pins together, and reading data from and/or writing data to this “combined” signal. This simplification is possible because only one of these signals are active at any given time. The inactive signal will be tri-stated.

FIGURE 4. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE



ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT71D00ID	24 Lead JEDEC SOIC (300 mil)	-40°C to +85°C
XRT71D00IQ32	32 Lead TQFP	-40°C to +85°C