Signetics

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Status	Product Specification
FAST Products	

FAST 74F189A

64-Bit TTL Bipolar RAM, Inverting (3-State)

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F189A	5ns	55mA

FEATURES

- High speed performance
- Replaces 74F189
- Address access time: 8 ns max vs 28ns for 74F189
- Power dissipation: 4.3 mW/bit typ
- Schottky clamped TTL
- One chip enable
- Inverting outputs (For non-inverting outputs see 74F219A)
- Buffered PNP inputs
- 3-state outputs
- 74F189A in 150 mil wide S.O. is preferred option for new designs
- C3F189A in 300 mil wide S.O.L. replaces 74F189 in existing designs

APPLICATIONS

- Scratch pad memory
- Buffer memory
- Push down stacks
- Control store

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F189AN
16-Pin Plastic SO (150 mil)	N74F189AD
16-Pin Plastic SOL (300 mil)	C3F189AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

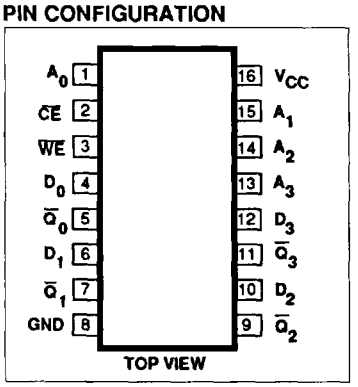
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_3	Data inputs	1.0/1.0	20µA/0.6mA
A_0- A_3	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Chip Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{WE}$	Write Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{Q}_0$- $\overline{Q}_3$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

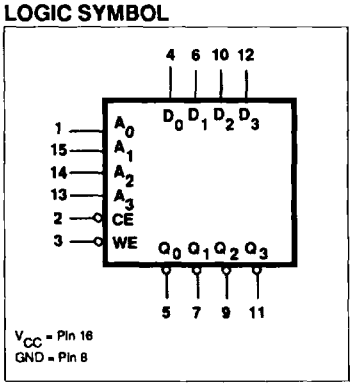
DESCRIPTION

The 74F189A is a high speed, 64-Bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are in High impedance state whenever the Chip Enable ($\overline{CE}$) is High. The outputs are active only in the READ mode ($\overline{WE}$ = High) and the output data is the complement of the stored data.

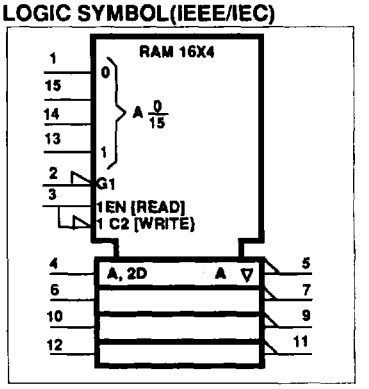
PIN CONFIGURATION



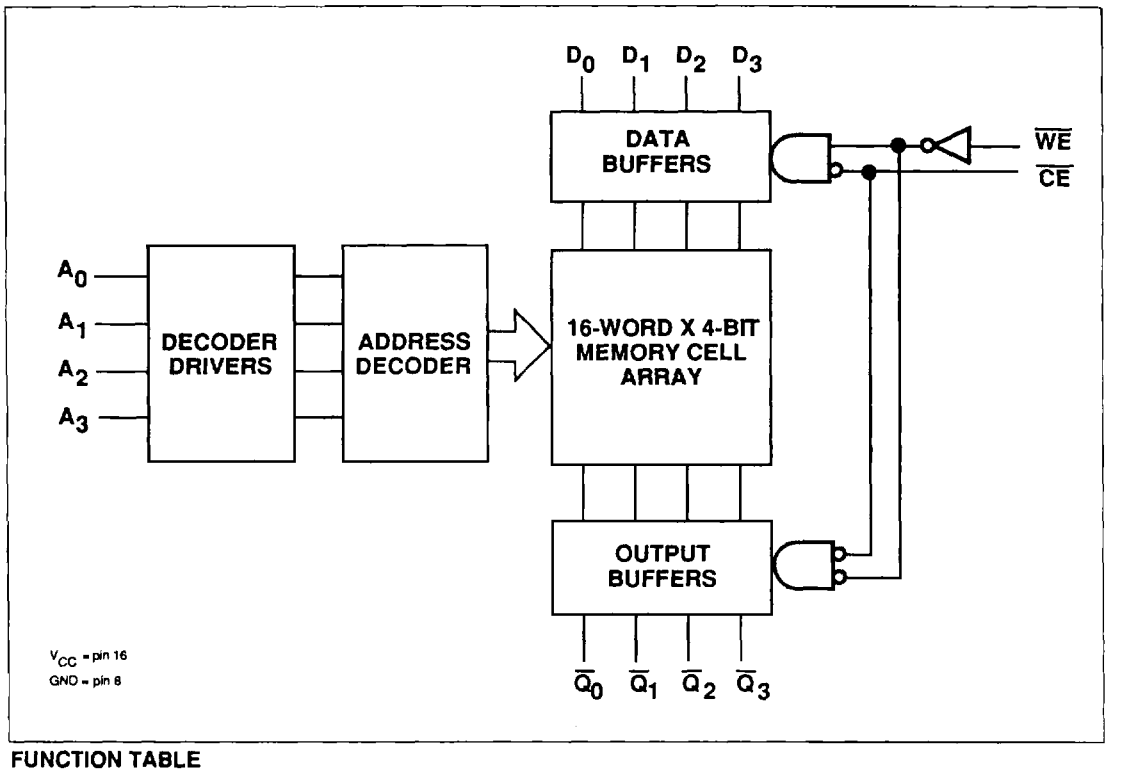
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
$\overline{CE}$	$\overline{WE}$	D_n	$\overline{Q}_n$	
L	H	X	Complement of stored data	Read
L	L	L	High impedance	Write "0"
L	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable Input

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CE}$, $\overline{WE}$					-1.2	mA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	mA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V				-50	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{CE}$ = $\overline{WE}$ = GND			55	80	mA
C_{IN}	Input capacitance		V_{CC} = 5V, V_{IN} = 2.0V			4		pF
C_{OUT}	Output capacitance		V_{CC} = 5V, V_{OUT} = 2.0V			7		pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

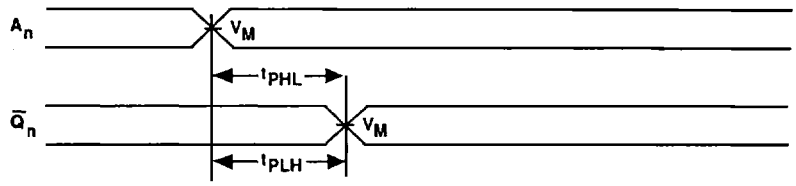
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Access time	Propagation delay A_n to $\overline{Q}_n$	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	8.0 8.0	ns
t_{PZH} t_{PZL}		Enable time $\overline{CE}$ to $\overline{Q}_n$	Waveform 2	2.0 2.0	3.5 4.0	6.0 7.0	1.5 2.0	7.0 7.5	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{CE}$ to $\overline{Q}_n$		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.5	8.0 6.0	ns
t_{PZH} t_{PZL}	Write Recovery time	Enable time $\overline{WE}$ to $\overline{Q}_n$	Waveform 4	2.0 2.5	4.0 4.5	6.5 7.5	2.0 2.5	7.0 8.0	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{WE}$ to $\overline{Q}_n$		Waveform 4	3.5 1.5	5.5 3.5	8.5 6.5	3.0 1.5	9.0 7.0	ns

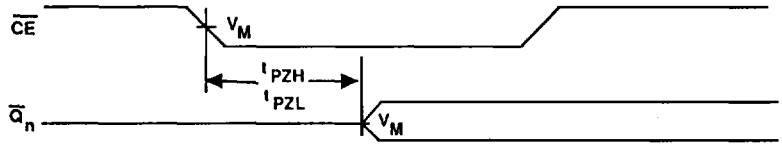
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time A_n to $\overline{WE}$	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A_n to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time D_n to $\overline{WE}$	Waveform 4	7.5 6.5			9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to $\overline{WE}$	Waveform 4	0 0			0 0		ns
$t_s(L)$	Setup time $\overline{CE}$ (falling edge) to $\overline{WE}$ (falling edge)	Waveform 4	0			0		ns
$t_h(L)$	Hold time $\overline{WE}$ (falling edge) to $\overline{CE}$ (rising edge)	Waveform 4	6.5			7.5		ns
$t_w(L)$	Pulse width, Low $\overline{WE}$	Waveform 4	7.0			8.0		ns

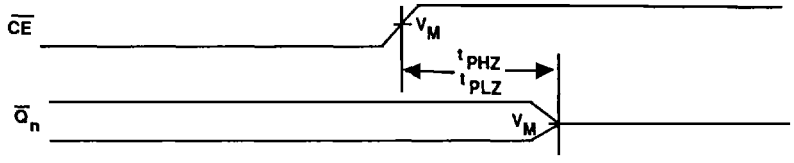
AC WAVEFORMS



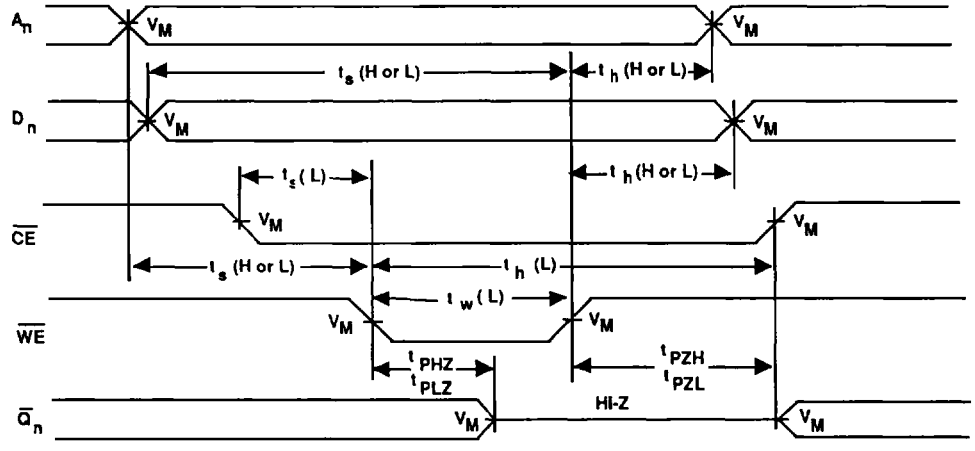
Waveform1. Read Cycle, Address Access Time



Waveform 2. Read Cycle, Chip Enable Access Time



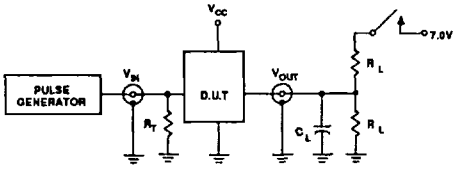
Waveform 3. Read Cycle, Chip Disable Time



Waveform 4. Write Cycle

NOTES: 1. For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

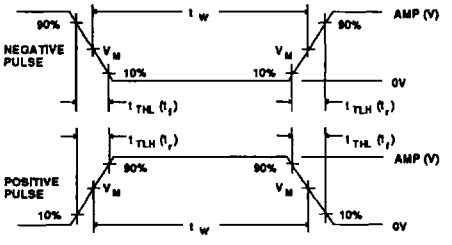
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns