VANTIS
AN AMD COMPANY

MACH4-64/MACH4LV-64

High-Performance EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- **44 pins in PLCC, 44 and 48 pins in TQFP**
- **64 macrocells**
- **7.5 ns t_{PD} Commercial, 10 ns t_{PD} Industrial**
- **133 MHz f_{CNT}**
- **32 I/Os; 2 dedicated inputs/clocks**
- **96 flip-flops**
  - 64 Macrocell flip-flops
  - 32 Input flip-flops
- **Up to 20 product terms per macrocell, with XOR**
- **Flexible clocking**
  - Two global clock pins with selectable edges
  - Asynchronous mode available for each macrocell
- **SpeedLocking for guaranteed fixed timing**
- **5-V and 3.3-V supply voltage options**
  - JEDEC compatible for both 5-V and 3.3-V versions
- **5-V or 3.3-V in-system programmable through JTAG (IEEE Std. 1149.1) interface**
- **JTAG boundary scan testing capability**
- **Input and output switch matrices for high routability and pinout retention**
- **Zero-hold-time input register option**
- **Peripheral Component Interconnect (PCI) compliant (-7/-10/-12 speed grades)**
- **Enhanced features**
  - Bus-Friendly inputs and I/Os
  - PAL Block programmable power-down mode for further power savings
  - Individual output slew rate control
  - Both 5-V and 3.3-V supply voltage options are safe for mixed supply voltage system designs
- **Fully pin-out and function compatible with the MACH211SP**

GENERAL DESCRIPTION

The MACH4-64 (M4-64) and MACH4LV-64 (M4LV-64) are members of Vantis' high-performance EE CMOS MACH 4 family. This device has the same macrocell capability of the popular MACH211SP, with significant additional functional features.

The M4-64 (M4LV-64) consists of 4 PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output

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switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The M4-64 (M4LV-64) has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per macrocell can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The M4-64 (M4LV-64) macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer using software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

The M4-64 (M4LV-64) is fully pin-out and function compatible with the MACH211SP. Each PAL block has a programmable power-down mode for further power saving of up to 50%; each I/O has an individually programmable output slew-rate control bit; and all inputs and I/Os feature the Bus-Friendly circuitry which weakly holds the voltage at the input to a logic low or high level depending on the last driven logic level. Both 5-V and 3.3-V supply operation versions are safe for mixed supply voltage system designs. The 3.3-V supply operation device has its power consumption significantly reduced due to the lower supply voltage, while providing the same high performance as the 5-V version.

Vantis offers software design support for MACH devices through its own development system and device fitters integrated into third-party CAE tools. Platform support extends across PCs, Sun and HP workstations under advanced operating systems such as Windows 3.1, Windows 95 and NT, SunOS and Solaris, and HPUX.

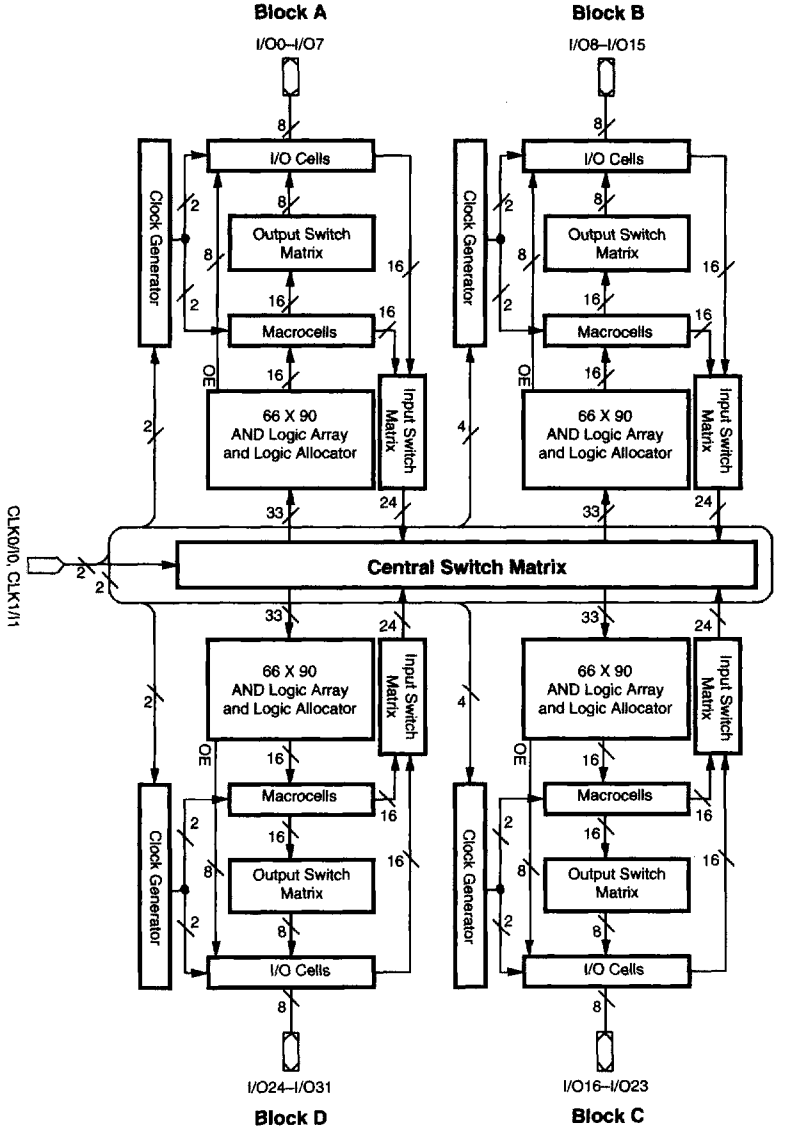
MACHXL software is a complete development system for the PC, supporting Vantis' MACH devices. It supports design entry with Boolean and behavioral syntax, state machine syntax and truth tables. Functional simulation and static timing analysis are also included in this easy-to-use system. This development system includes high-performance device fitters for all MACH devices.

The same fitter technology included in MACHXL software is seamlessly incorporated into third-party tools from leading CAE vendors such as Synario, Viewlogic, Mentor Graphics, Cadence and MINC. Interface kits and MACHXL configurations are also available to support design entry and verification with other leading vendors such as Synopsys, Exemplar, OrCAD, Synplicity and Model Technology. These MACHXL configurations and interfaces accept EDIF 2.0.0 netlists, generate JEDEC files for MACH devices, and create industry-standard SDF, VITAL-compliant VHDL and Verilog output files for design simulation.

Vantis offers in-system programming support for MACH devices through its MACHPRO software enabling MACH device programmability through JTAG compliant ports and easy-to-use PC interface. Additionally, MACHPRO generated vectors work seamlessly with HP3070, GenRad and Teradyne testers to program MACH devices or test them for connectivity.

All MACH devices are supported by industry standard programmers available from a number of vendors. These programmer vendors include Advin Systems, BP Microsystems, Data I/O Corporation, Hi-Lo Systems, SMS GmbH, Stag House, and System General.

BLOCK DIAGRAM



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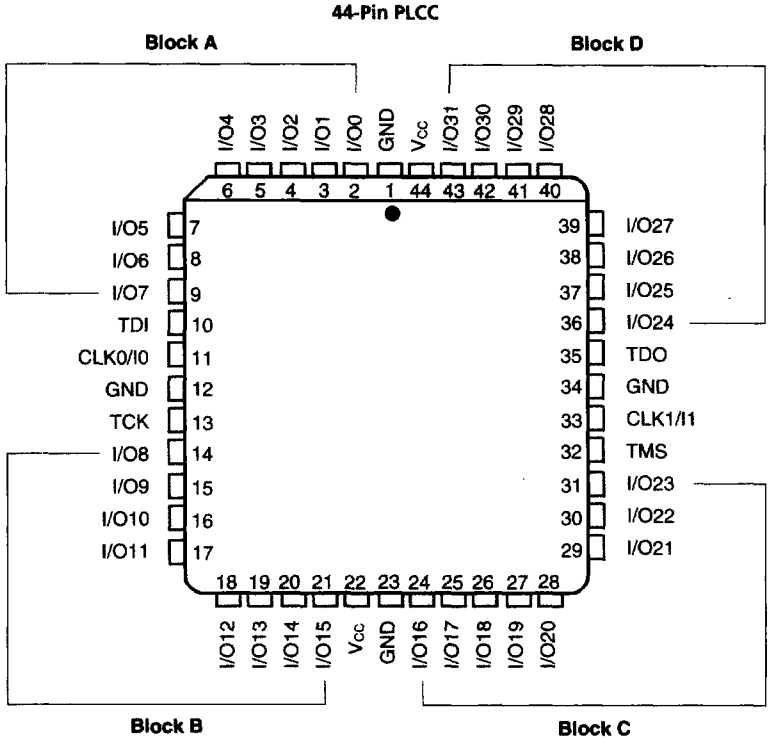
CONNECTION DIAGRAM

Top View



Note:

Pin-compatible with the M4(LV)-32, MACH211SP and MACH111SP.

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

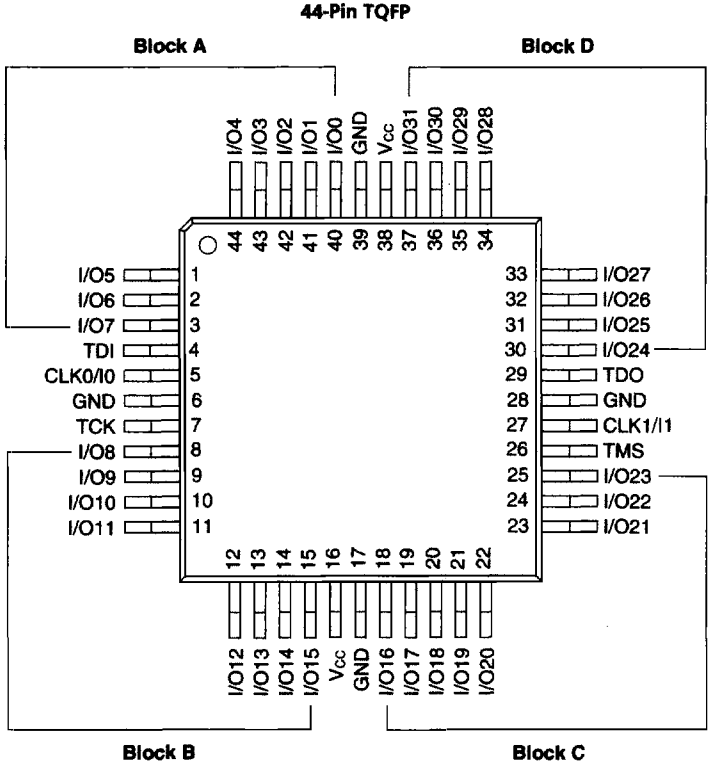
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

CONNECTION DIAGRAM

Top View



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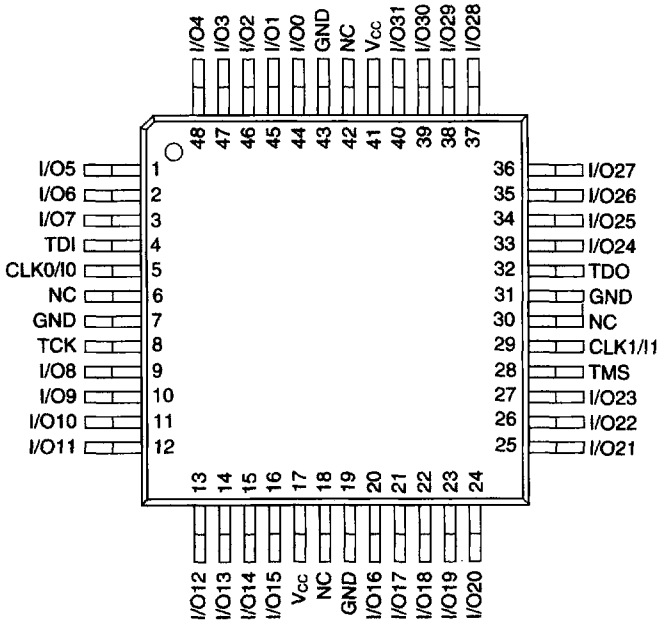
CONNECTION DIAGRAM

Top View

48-Pin TQFP



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Note:
Pin-compatible with the M4(LV)-32.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
NC = No Connect
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out