CYPRESS SEMICONDUCTOR

CMOS Microprogram Controller

Features

- **Fast**
  - **— CY7C910–40 has a 40-ns (min.) clock cycle; commercial**
  - **— CY7C910–46 has a 46-ns (min.) clock cycle; military**
- **Low power**
  - **— I_{CC} (max.) = 70 mA**
- **V_{CC} margin of 5V ±10% commercial and military**
- **Sixteen powerful microinstructions**
- **Three output enable controls for three-way branch**
- **Twelve-bit address word**
- **Four sources for addresses: microprogram counter (MPC), stack, branch address bus, internal holding register**
- **12-bit internal loop counter**
- **Internal 17-word by 12-bit stack can be used for subroutine return address or data storage**
- **Capable of withstanding greater than 2001V static discharge voltage**
- **Pin compatible and functional equivalent to Am2910A**

Functional Description

The CY7C910 is a standalone microprogram controller that selects, stores, retrieves, manipulates, and tests addresses that control the sequence of execution of instructions stored in an external memory. All addresses are 12-bit binary values that designate an absolute memory location.

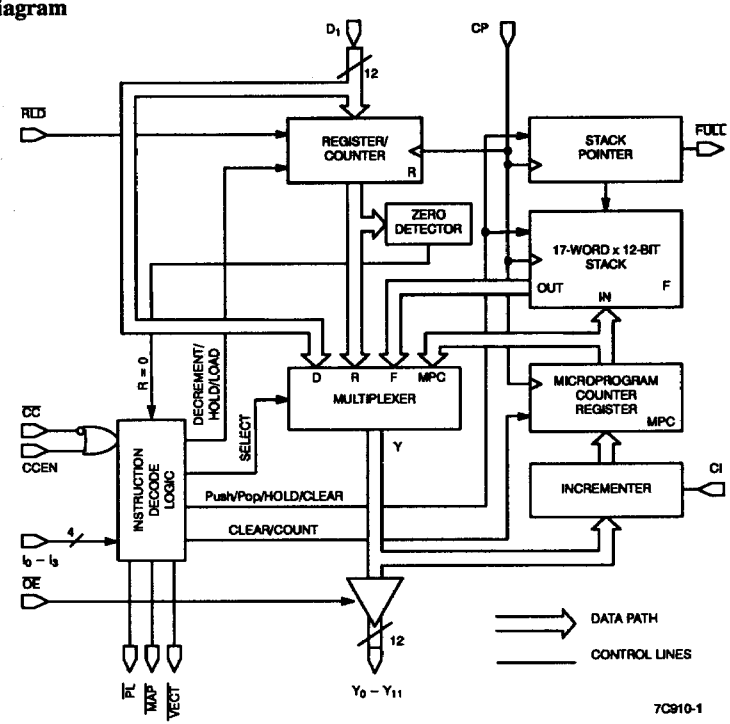
The CY7C910, as illustrated in the block diagram, consists of a 17-word by 12-bit LIFO (Last-In-First-Out) stack and SP (Stack Pointer), a 12-bit RC (Register/Counter), a 12-bit MPC (Micro Program Counter) and incrementer, a 12-bit-wide by 4-input multiplexer, and the required data manipulation and control logic.

The operation performed is determined by four input instruction lines (I_0 – I_3) that in turn select the (internal) source of the next micro-instruction to be fetched. This address is output on the Y_0 – Y_{11} pins. Two additional inputs ($\overline{CC}$ and $\overline{CCEN}$) are provided that are examined during certain instructions and enable the user to make the execution of the instruction either unconditional or dependent upon an external test.

The CY7C910 is a pin-compatible, functional-equivalent, improved-performance replacement for the Am2910A.

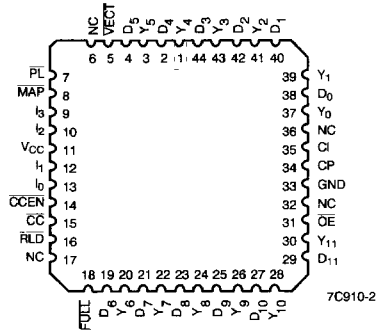
The CY7C910 is fabricated using an advanced 1.2-micron CMOS process that eliminates latch-up, results in ESD protection over 2000 volts, and achieves superior performance and low power dissipation.

Logic Block Diagram

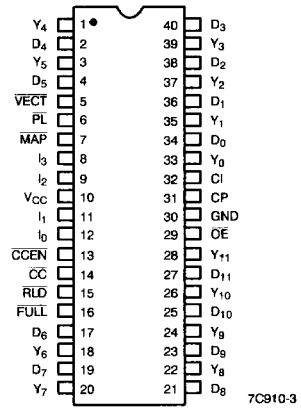


Pin Configurations

PLCC
Top View



DIP
Top View



Selection Guide

Minimum Clock Cycle (ns)	Stack Depth (words)	Operating Range	Part Number
40	17	Commercial	CY7C910–40
46	17	Military	CY7C910–46
50	17	Commercial	CY7C910–50
51	17	Military	CY7C910–51
93	17	Commercial	CY7C910–93
99	17	Military	CY7C910–99

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 30 mA

Static Discharge Voltage ..... >2001V (Per MIL-STD-883 Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%

Note:

1. T_A is the "instant on" case temperature.

6 LOGIC

Pin Definitions

Signal Name	I/O	Description
$D_0 - D_{11}$	I	Direct inputs to the RC (Register/Counter) and multiplexer. D_0 is LSB and D_{11} is MSB
$\overline{RLD}$	I	Register load. Control input to RC that, when LOW, loads data on the $D_0 - D_{11}$ pins into RC on the LOW-to-HIGH clock (CP) transition.
$I_0 - I_3$	I	Instruction inputs that select one of sixteen instructions to be performed by the CY7C910.
$\overline{CC}$	I	Control input that, when LOW, signifies that a test has passed.
$\overline{CCEN}$	I	Enable for $\overline{CC}$ input. When HIGH $\overline{CC}$ is ignored and a pass is forced. When LOW the state of $\overline{CC}$ is examined.
CP	I	Clock input. All internal states are changed on the LOW-to-HIGH clock transitions.
CI	I	Carry input to the LSB of the incrementer for the MPC.
$\overline{OE}$	I	Control for $Y_0 - Y_{11}$ outputs. LOW to enable; HIGH to disable.
$Y_0 - Y_{11}$	O	Address output to microprogram memory. Y_0 is LSB and Y_{11} is MSB.
$\overline{FULL}$	O	When LOW indicates the stack is full.
$\overline{PL}$	O	When LOW, this indicates the pipeline register has been selected as the direct input ($D_0 - D_{11}$) source.
$\overline{MAP}$	O	When LOW, this indicates the mapping PROM (or PLA) has been selected as the direct input ($D_0 - D_{11}$) source.
$\overline{VECT}$	O	When LOW, this indicates the Interrupt Vector has been selected as the direct input ($D_0 - D_{11}$) source.

Architecture of the CY7C910

Introduction

The CY7C910 is a high-performance CMOS microprogram controller that produces a sequence of 12-bit addresses that control the execution of a microprogram. The addresses are selected from one of four sources, depending upon the (internal) instruction being executed ($I_0 - I_3$), and other external inputs. The sources are (1) the external ($D_0 - D_{11}$) inputs, (2) the RC, (3) the stack, and (4) the MPC. Twelve bit lines from each of these four sources are the inputs to a multiplexer as shown in the Logic Block Diagram. The outputs of the multiplexer are applied to the inputs of the three-state output drivers ($Y_0 - Y_{11}$).

External Inputs: $D_0 - D_{11}$

The external inputs are used as the source for destination addresses for the jump or branch type of instructions. These are shown as Ds in the two columns in the Table of Instructions. A second use of these inputs is to load the RC.

Register Counter: RC

The RC is implemented as twelve D-type, edge-triggered flip-flops that are synchronously clocked on the LOW-to-HIGH transition of the clock, CP. The data on the D inputs is synchronously loaded into the RC when the load control input, $\overline{RLD}$, is LOW. The output of the RC is available to the multiplexer as its R input and is output on the Y outputs during certain instructions, indicated with an R in the Table of Instructions.

The RC is operated as a 12-bit down counter. Its contents are decremented and tested to see if they are zero during instructions 8, 9, and 15. This enables micro-instructions to be repeated up to 4096 times. The RC is arranged such that if it is loaded with a number, n, the sequence will be executed exactly n + 1 times.

The Stack and Stack Pointer: SP

The 17-word by 12-bit stack is used to provide return addresses from micro-subroutines or from loops. The SP, which points to the last word written, is integral to the operation of the stack. This permits reference to the data on the top of the stack without having to perform a Pop operation.

The SP operates as an up/down counter that is incremented when a Push operation (instructions 1, 4, or 5) is performed or decremented when a Pop operation (instructions 8, 10, 11, 13, or 15) is performed. The Push operation writes the return address on the stack and the Pop operation effectively removes it. The actual operation occurs on the LOW-to-HIGH clock transition following the instruction.

The stack is initialized by executing instruction zero (JUMP TO LOCATION 0 or RESET). Every time a "jump to subroutine" instruction (1, 5) or a loop instruction (4) is executed, the return address is Pushed onto the stack; and every time a "return from subroutine (or loop)" instruction is executed, the return address is Popped off the stack.

When one subroutine calls another or a loop occurs within a loop (or a combination), which is called nesting, the logical depth of the stack increases. The physical stack depth is 17 words. When this depth occurs, the $\overline{FULL}$ signal goes LOW on the next LOW-to-HIGH clock transition. Any further Push operations on a full stack will cause the data at that location to be overwritten, but will not increment the SP. Similarly, performing a Pop operation on a empty stack will not decrement the SP and may result in non-meaningful data being available at the Y outputs.

The Microprocessor Counter: MPC

The MPC consists of a 12-bit incrementer followed by a 12-bit register. The register usually holds the address of the instruction being fetched. When sequential instructions are fetched, the carry input (CI) to the incrementer is HIGH and one is added to the Y outputs of the multiplexer, which is loaded into the MPC on the next LOW-to-HIGH clock transition. When the CI input is LOW, the Y outputs of the multiplexer are loaded directly into the MPC so that the same instruction is fetched and executed.

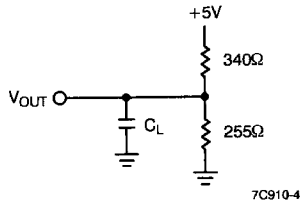
Electrical Characteristics Over Commercial and Military Operating Range, V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V[2]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 1.6 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			− 3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}			10	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = V_{SS}			− 10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{IH} = 2.4V		− 1.6		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.4V		12		mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = V_{SS}/V_{CC}		−40	+40	μA
I_{SC}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0V			− 85	mA
I_{CC}	Supply Current	V_{CC} = Max.	Commercial		70	mA
			Military		90	
I_{CC1}	Supply Current	$V_{IH} \geq$ 3.85V, $V_{IL} \leq$ 0.4V	Commercial		35	mA
			Military		50	

Capacitance[4]

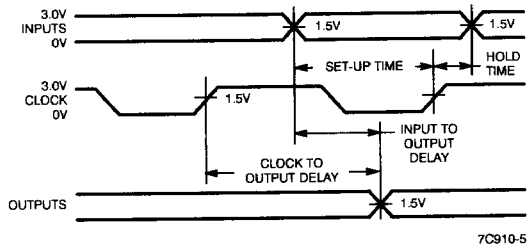
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Output Loads for AC Performance Characteristics[5,6]



All Outputs

Switching Waveforms



Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. Tested initially and after any design or process changes that may affect these parameters.
5. C_L = 50 pF includes scope probe, wiring, and stray capacitance.
6. C_L = 5 pF for output disable tests.

Guaranteed AC Performance Characteristics

The tables below specify the guaranteed AC performance of the CY7C910 over the commercial (0°C to +70°C) and the military (−55°C to +125°C) temperature ranges with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels.

The inputs switch between 0V and 3V with signal transition rates of 1 volt per nanosecond. All outputs have maximum DC current loads.

Clock Requirements[2]

	Commercial			Military		
Speed (ns)	40	50	93	46	51	99
Minimum Clock LOW	20	20	50	23	25	58
Minimum Clock HIGH	20	20	35	23	25	42
Minimum Clock Period I = 14	40	50	93	46	51	100
Minimum Clock Period I = 8, 9, 15	40	50	113	46	51	114

Combinatorial Propagation Delays (C_L = 50 pF)[2, 7]

	Commercial									Military								
From Input	Y			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$			$\overline{FULL}$			Y			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$			$\overline{FULL}$		
Speed (ns)	40	50	93	40	50	93	40	50	93	46	51	99	46	51	99	46	51	99
$D_0 - D_{11}$	17	20	20	—	—	—	—	—	—	21	25	25	—	—	—	—	—	—
$I_0 - I_3$	25	35	50	20	30	51	—	—	—	30	40	54	25	35	58	—	—	—
$\overline{CC}$	22	30	30	—	—	—	—	—	—	27	36	35	—	—	—	—	—	—
$\overline{CCEN}$	22	30	30	—	—	—	—	—	—	27	36	37	—	—	—	—	—	—
CP I = 8, 9, 15[8]	30	40	75	—	—	—	25	31	60	35	46	77	—	—	—	30	35	67
CP All Other I	30	40	55	—	—	—	25	31	60	35	46	61	—	—	—	30	35	67
$\overline{OE}$[8]	21 21	25 27	35 30	—	—	—	—	—	—	22 22	25 30	40 30	—	—	—	—	—	—

Minimum Set-Up and Hold Times Relative to clock LOW-to-HIGH Transition (C_L = 50 pF)[2]

	Commercial						Military					
	Set-Up			Hold			Set-Up			Hold		
Speed (ns)	40	50	93	40	50	93	46	51	99	46	51	99
DI ⇂ RC	13	16	24	0	0	0	13	16	28	0	0	0
DI ⇂ MPC	20	30	58	0	0	0	20	30	62	0	0	0
$I_0 - I_3$	25	35	75	0	0	0	27	38	81	0	0	0
$\overline{CC}$	20	24	63	0	0	0	25	35	65	0	0	0
$\overline{CCEN}$	20	24	63	0	0	0	25	35	63	0	0	0
CI	15	18	46	0	0	0	15	18	58	0	0	0
$\overline{RLD}$	15	19	36	0	0	0	15	20	42	0	0	0

Notes:

7. A dash indicates that a propagation delay path or set-up time does not exist.
8. The enable/disable times are measured to a 0.5 Volt change on the output voltage level with C_L = 5 pF.

Table of Instructions

$I_3 - I_0$	Mnemonic	Name	Reg/Cntr Contents	Result					
				Fail $\overline{CCEN}$ = L and $\overline{CC}$ = H		Pass $\overline{CCEN}$ = H or $\overline{CC}$ = L		Reg/Cntr	Enable
				Y	Stack	Y	Stack		
0	JZ	Jump Zero	X	0	Clear	0	Clear	Hold	PL
1	CJS	Cond JSB PL	X	PC	Hold	D	Push	Hold	PL
2	JMAP	Jump Map	X	D	Hold	D	Hold	Hold	Map
3	CJP	Cond Jump PL	X	PC	Hold	D	Hold	Hold	PL
4	Push	Push/Cond LD CNTR	X	PC	Push	PC	Push	(Note 9)	PL
5	JSPR	Cond JSB R/PL	X	R	Push	D	Push	Hold	PL
6	CJV	Cond Jump Vector	X	PC	Hold	D	Hold	Hold	Vect
7	JRP	Cond Jump R/PL	X	R	Hold	D	Hold	Hold	PL
8	RFCT	Repeat Loop, CNTR $\neq 0$	$\neq 0$	F	Hold	F	Hold	Dec	PL
			=0	PC	Pop	PC	Pop	Hold	PL
9	RPCT	Repeat PL, CNTR $\neq 0$	$\neq 0$	D	Hold	D	Hold	Dec	PL
			=0	PC	Hold	PC	Hold	Hold	PL
10	CRTN	Cond RTN	X	PC	Hold	F	Pop	Hold	PL
11	CJPP	Cond Jump PL & Pop	X	PC	Hold	D	Pop	Hold	PL
12	LDCT	LD Cntr & Continue	X	PC	Hold	PC	Hold	Load	PL
13	LOOP	Test End Loop	X	F	Hold	PC	Pop	Hold	PL
14	CONT	Continue	X	PC	Hold	PC	Hold	Hold	PL
15	TWB	Three-Way Branch	$\neq 0$	F	Hold	PC	Pop	Dec	PL
			=0	D	Pop	PC	Pop	Hold	PL

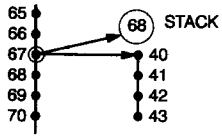
H = HIGH
L = LOW
X = Don't Care

Notes:
9. If $\overline{CCEN}$ = L and $\overline{CC}$ = H, then hold; else load.

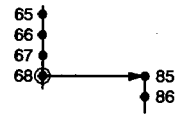
CY7C910 Flow Diagrams

0 Jump Zero (JZ)

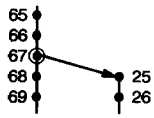
1 Cond JSB PL (CJS)



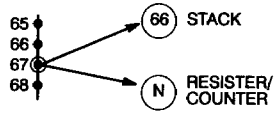
2 Jump Map (JMAP)



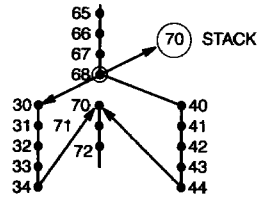
3 Cond Jump PL (CJP)



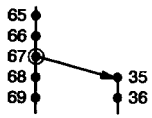
4 Push/Cond LD CNTR (PUSH)



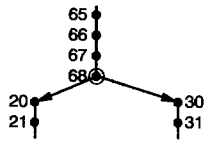
5 Cond JSB R/PL (JSRP)



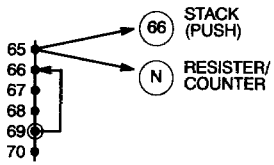
6 Cond Jump Vector (CJV)



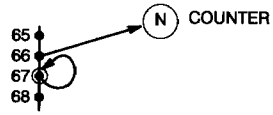
7 Cond Jump R/PL (JRP)



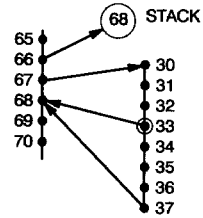
8 Repeat Loop, CNTR ≠ 0 (RFCT)



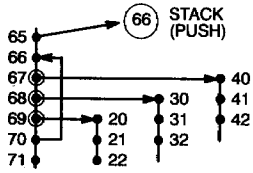
9 Repeat PL, CNTR ≠ 0 (RPCT)



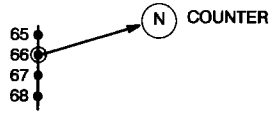
10 Cond Return (CRTN)



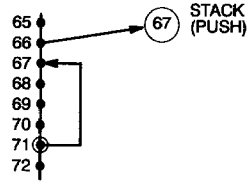
11 Cond Jump PL & POP (CJPP)



12 LD CNTR & Continue (LDCT)

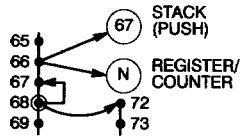


13 Test End Loop (LOOP)



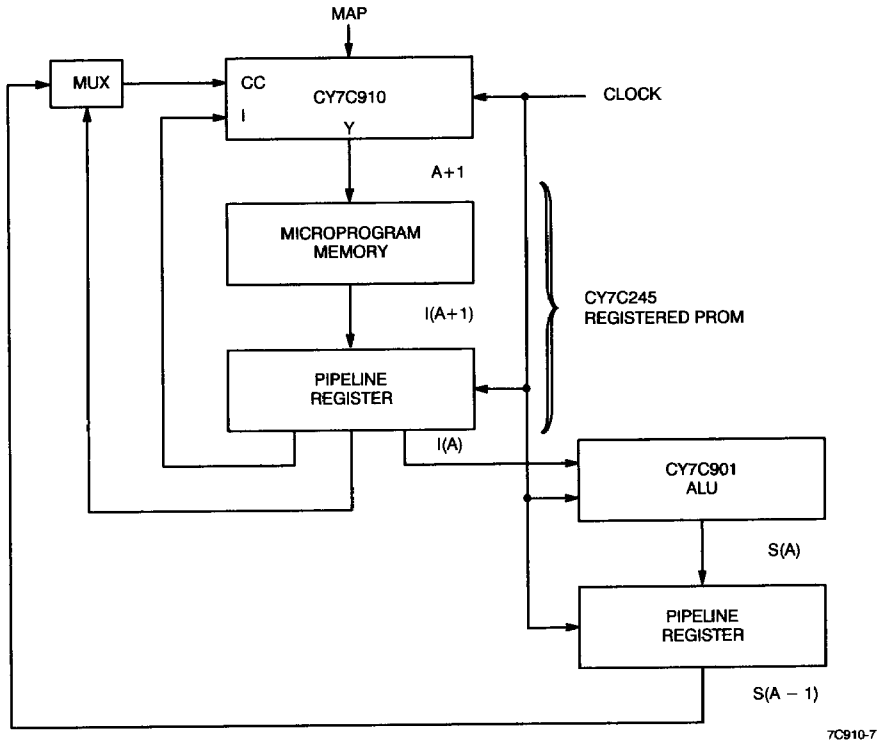
14 Continue (CONT)

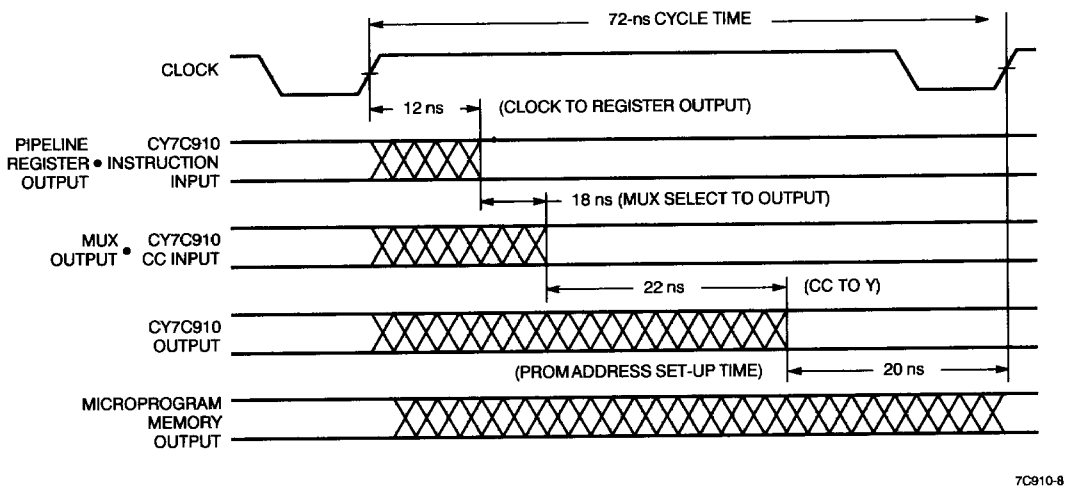
15 Three-Way Branch (TWB)



7C910-6

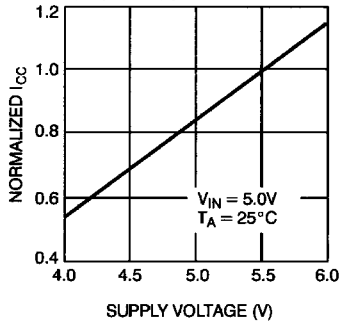
One-Level Pipeline-Based Architecture (recommended)



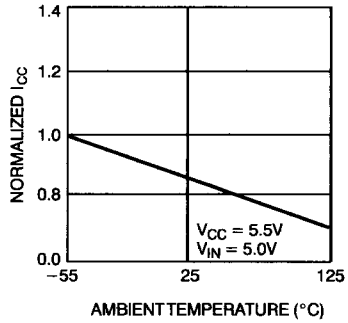


Typical DC and AC Characteristics

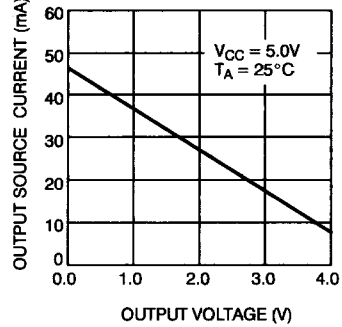
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



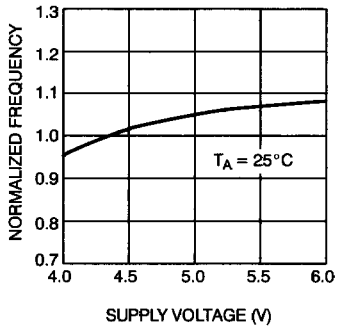
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



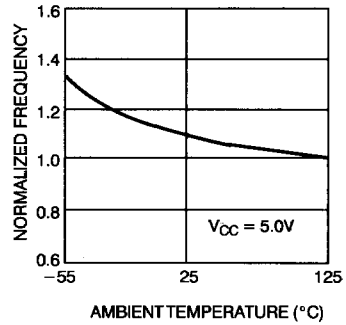
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



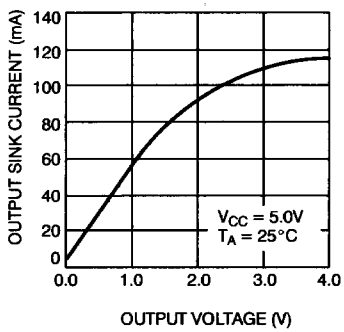
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



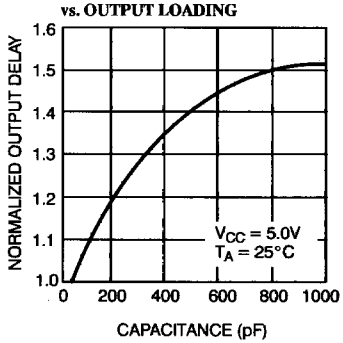
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



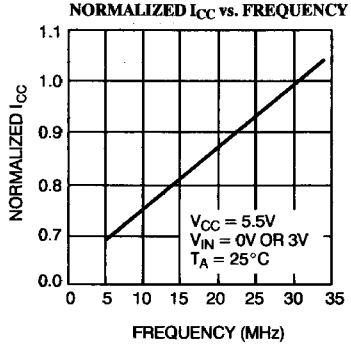
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED OUTPUT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



7C910-9

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
40	CY7C910–40DC	D18	Commercial
	CY7C910–40JC	J67	
	CY7C910–40LC	L67	
	CY7C910–40PC	P17	
46	CY7C910–46DMB	D18	Military
	CY7C910–46LMB	L67	
50	CY7C910–50DC	D18	Commercial
	CY7C910–50JC	J67	
	CY7C910–50LC	L67	
	CY7C910–50PC	P17	
51	CY7C910–51DMB	D18	Military
	CY7C910–51LMB	L67	
93	CY7C910–93DC	D18	Commercial
	CY7C910–93JC	J67	
	CY7C910–93LC	L67	
	CY7C910–93PC	P17	
99	CY7C910–99DMB	D18	Military
	CY7C910–99LMB	L67	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IH}	1, 2, 3
I_{IL}	1, 2, 3
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CC1}	1, 2, 3

Clock Requirements

Parameters	Subgroups
Minimum Clock LOW	7, 8, 9, 10, 11

Combinational Propagation Delays

Parameters	Subgroups
From $D_0 - D_{11}$ to Y	7, 8, 9, 10, 11
From $I_0 - I_3$ to Y	7, 8, 9, 10, 11
From $I_0 - I_3$ to $\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	7, 8, 9, 10, 11
From $\overline{CC}$ to Y	7, 8, 9, 10, 11
From $\overline{CCEN}$ to Y	7, 8, 9, 10, 11
From CP (I = 8, 9, 15) to $\overline{FULL}$	7, 8, 9, 10, 11
From CP (All Other I) to Y	7, 8, 9, 10, 11
From CP (All Other I) to $\overline{FULL}$	7, 8, 9, 10, 11

Minimum Set-Up and Hold Times

Parameters	Subgroups
DI ↓ RC Set-Up Time	7, 8, 9, 10, 11
DI ↓ RC Hold Time	7, 8, 9, 10, 11
DI ↓ MPC Set-Up Time	7, 8, 9, 10, 11
DI ↓ MPC Hold Time	7, 8, 9, 10, 11
$I_0 - I_3$ Set-Up Time	7, 8, 9, 10, 11
$I_0 - I_3$ Hold Time	7, 8, 9, 10, 11
$\overline{CC}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{CC}$ Hold Time	7, 8, 9, 10, 11
$\overline{CCEN}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{CCEN}$ Hold Time	7, 8, 9, 10, 11
CI Set-Up Time	7, 8, 9, 10, 11
CI Hold Time	7, 8, 9, 10, 11
$\overline{RLD}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{RLD}$ Hold Time	7, 8, 9, 10, 11

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