



# DM2M36SJ/DM2M32SJ 2Mbx36/2Mbx32 Enhanced DRAM SIMM

Product Specification

## Features

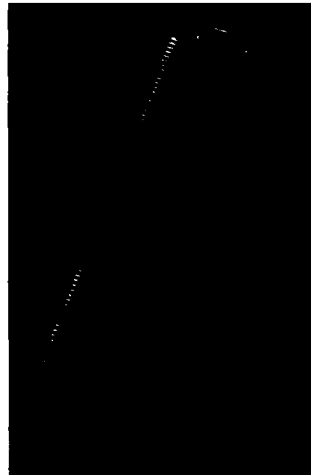
- 4Kbyte SRAM Cache Memory for 15ns Random Reads Within a Page
- Fast DRAM Array for 35ns Access to Any New Page
- Write Posting Register for 15ns Random Writes and Burst Writes Within a Page (Hit or Miss)
- Simple On-chip Page Caching Control Allows DRAM-like System Architecture and Compatibility
- 4Kbyte Wide DRAM to SRAM Bus for 117 Gigabytes/Sec Cache Fill
- On-chip Cache Hit/Miss Comparators Maintain Cache Coherency on Writes
- Hidden Precharge Cycles
- Hidden Refresh or /CAS Before /RAS Type Refresh Cycles
- Extended 64ms Refresh Period for Low Standby Power
- Standard CMOS/TTL Compatible I/O Levels and +5 Volt Supply
- Compatibility with JEDEC 2M x 36 DRAM SIMM Configuration Allows Performance Upgrade in System

## Description

The Ramtron 8Mb enhanced DRAM SIMM module provides a single memory module solution for the main memory or local memory of fast PCs, workstations, servers, and other high performance systems. Due to its fast 15ns cache row register, the EDRAM memory module supports zero-wait-state burst read operations at up to 40MHz bus rates in a non-interleave configuration and >66MHz bus rates with a two-way interleave configuration.

On-chip write posting and fast page mode operation supports 15ns write and burst write operations. On a cache miss, the fast DRAM array reloads the entire 2Kbyte cache over a 2Kbyte-wide bus in 35ns for an effective bandwidth of 58 Gbytes/sec. This means very low latency and fewer wait states on a cache miss than a non-integrated cache/DRAM solution. The JEDEC compatible 72-bit SIMM

configuration allows a single memory controller to be designed to support either JEDEC slow DRAMs or high speed EDRAMs to provide a simple upgrade path to higher system performance.



## Architecture

The DM2M36SJ achieves 2Mb x 36 density by mounting 18 1M x 4 EDRAMs, packaged in 28-pin plastic SOJ packages, on both sides of the multi-layer substrate. Sixteen DM2202 and two DM2212 devices provide data and parity storage. The DM2M32SJ contains 16 DM2202 devices for data only and parity memory is not included.

The EDRAM memory module architecture is very similar to a standard 8Mb DRAM module with the addition of an integrated

cache and on-chip control which allows it to operate much like a page mode or static column DRAM.

The EDRAM's SRAM cache is integrated into the DRAM array as tightly coupled row registers. Memory reads always occur from the cache row register. When the on-chip comparator detects a page hit, only the SRAM is accessed and data is available in 15ns from column address. When a page read miss is detected, the entire new DRAM row is loaded into the cache and data is available at the output all within 35ns from row enable. Subsequent reads within the page

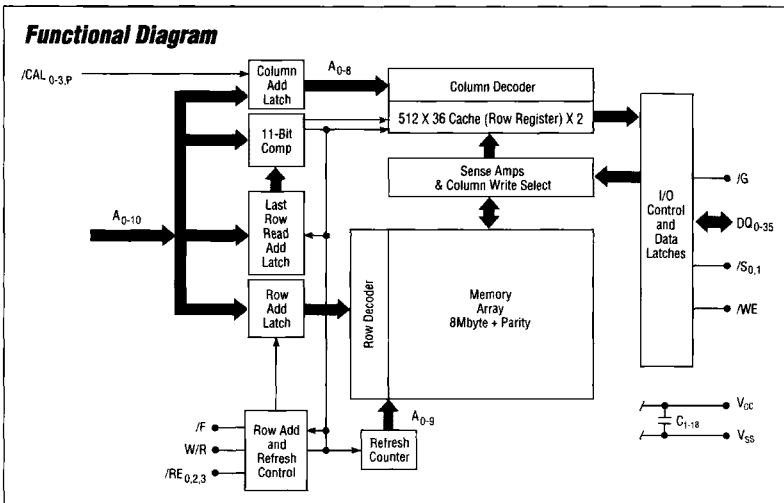
(burst reads or random reads) will continue at 15ns cycle time. Since reads occur from the SRAM cache, the DRAM precharge can occur simultaneously without degrading performance. The on-chip refresh counter with independent refresh bus allows the EDRAM to be refreshed during cache reads.

Memory writes are internally posted in 15ns and directed to the DRAM array. During a write hit, the on-chip address comparator activates a parallel write path to the SRAM cache to maintain coherency. The EDRAM delivers 15ns cycle page mode memory writes. Memory writes do not affect the contents of the cache row register except during a cache hit.

By integrating the SRAM cache as row registers in the DRAM array and keeping the on-chip control simple, the EDRAM is able to provide superior performance

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## Functional Diagram



without any significant increase in die size over standard slow DRAMs. By eliminating the need for SRAMs and cache controllers, system cost, board space, and power can all be reduced.

## Functional Description

The EDRAM is designed to provide optimum memory performance with high speed microprocessors. As a result, it is possible to perform simultaneous operations to the DRAM and SRAM cache sections of the EDRAM. This feature allows the EDRAM to hide precharge and refresh operation during SRAM cache reads and maximize SRAM cache hit rate by maintaining valid cache contents during write operations even if data is written to another memory page. These new functions, in conjunction with the faster basic DRAM and cache speeds of the EDRAM, minimize processor wait states.

## EDRAM Basic Operating Modes

The EDRAM operating modes are specified in the table below.

### Hit and Miss Terminology

In this datasheet, "hit" and "miss" always refer to a hit or miss to the page of data contained in the SRAM cache row register. This is always equal to the contents of the last row that was read from (as modified by any write hit data). Writing to a new page does not cause the cache to be modified.

### DRAM Read Hit

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the last row read address latch (LRR; an 11-bit latch loaded on each /RE active read cycle). If the row address matches the LRR, the requested data is already in the SRAM cache and no DRAM memory reference is initiated. The data specified by the column address is available at the output pins at the greater of times  $t_{CC}$  or  $t_{CQV}$ . Since no DRAM activity is initiated, /RE can be brought high after time  $t_{RE1}$ , and a shorter precharge time,  $t_{RP1}$ , is required. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time  $t_{CC}$  after each column address changes. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

### DRAM Read Miss

If a DRAM read request is initiated by clocking /RE with W/R low and /F and /CAL high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match the LRR, the requested data is not in SRAM cache and a new row must be fetched from the DRAM. The EDRAM will load the new row data into the SRAM cache and update the LRR latch. The data at the specified column address is available at the output pins at the greater of times  $t_{RC}$ ,  $t_{CC}$ , and  $t_{CQV}$ . It is possible to bring /RE high after time  $t_{RE}$  since the new row data is safely latched into SRAM cache. This allows the EDRAM to precharge the DRAM array while data is accessed from SRAM cache. It is possible to access additional SRAM cache locations by providing new column addresses to the multiplex address inputs. New data is available at the output at time  $t_{CC}$  after each column address change. During read cycles, it is possible to operate in either static column mode with /CAL=high or page mode with /CAL clocked to latch the column address.

### DRAM Write Hit

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit address latch loaded on each /RE active read). If the row address matches, the EDRAM will write data to both the DRAM array and selected SRAM cache simultaneously to maintain coherency. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE ( $t_{RA1} + t_{ASC}$  for the column address and  $t_{DS}$  for the data). During a write burst sequence, the second write data can be posted at time  $t_{RSW}$  after /RE. Subsequent writes within a page can occur with write cycle time  $t_{WC}$ . With /G enabled and /WE disabled, it is possible to perform cache read operations while the /RE is activated in write hit mode. This allows read-modify-write, write-verify, or random read-write sequences within the page with 15ns cycle times (the first read cannot complete until after time  $t_{RAC2}$ ). At the end of a write sequence (after /CAL and /WE are brought high and  $t_{RE}$  is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, the /CAL input can be used as a byte write select in multi-chip systems. If /CAL

## EDRAM Basic Operating Modes

Function	/S	/RE	W/R	/F	$A_{0-10}$	Comment
Read Hit	L	↓	L	H	Row = LRR	No DRAM Reference, Data in Cache
Read Miss	L	↓	L	H	Row ≠ LRR	DRAM Row to Cache
Write Hit	L	↓	H	H	Row = LRR	Write to DRAM and Cache, Reads Enabled
Write Miss	L	↓	H	H	Row ≠ LRR	Write to DRAM, Cache Not Updated, Reads Disabled
Internal Refresh	X	↓	X	L	X	
Low Power Standby	H	H	X	X	X	1mA Standby Current
Unallowed Mode	H	↓	X	H	X	

H = High; L = Low; X = Don't Care; ↓ = High-to-Low Transition; LRR = Last Row Read

is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

### DRAM Write Miss

If a DRAM write request is initiated by clocking /RE while W/R and /F are high, the EDRAM will compare the new row address to the LRR address latch (an 11-bit latch loaded on each /RE active read cycle). If the row address does not match, the EDRAM will write data to the DRAM array only and contents of the current cache is not modified. The write address and data are posted to the DRAM as soon as the column address is latched by bringing /CAL low and the write data is latched by bringing /WE low (both /CAL and /WE must be high when initiating the write cycle with the falling edge of /RE). The write address and data can be latched very quickly after the fall of /RE ( $t_{RAM} + t_{ASC}$  for the column address and  $t_{DS}$  for the data). During a write burst sequence, the second write data can be posted at time  $t_{RSW}$  after /RE. Subsequent writes within a page can occur with write cycle time  $t_{PC}$ . During a write miss sequence, cache reads are inhibited and the output buffers are disabled (independently of /G) until time  $t_{WRR}$  after /RE goes high. At the end of a write sequence (after /CAL and /WE are brought high and  $t_{RE}$  is satisfied), /RE can be brought high to precharge the memory. It is possible to perform cache reads concurrently with the precharge. During write sequences, a write operation is not performed unless both /CAL and /WE are low. As a result, /CAL can be used as a byte write select in multi-chip systems. If /CAL is not clocked on a write sequence, the memory will perform a /RE only refresh to the selected row and data will remain unmodified.

### /RE Inactive Operation

It is possible to read data from the SRAM cache without clocking /RE. This option is desirable when the external control logic is capable of fast hit/miss comparison. In this case, the controller can avoid the time required to perform row/column multiplexing on hit cycles. This capability also allows the EDRAM to perform cache read operations during precharge and refresh cycles to minimize wait states. It is only necessary to select /S and /G and provide the appropriate column address to read data as shown in the table below. The row address of the SRAM cache accessed without clocking /RE will be specified by the LRR address latch loaded during the last /RE active read cycle. To perform a cache read in static column mode, /CAL is held high, and the cache contents at the specified column address will be valid at time  $t_{VC}$  after address is stable. To perform a cache read in page mode, /CAL is clocked to latch the column address. The cache data is valid at time  $t_{VC}$  after the column address is setup to /CAL.

Function	/S	/G	/CAL	$A_{0-8}$
Cache Read (Static Column)	L	L	H	Column Address
Cache Read (Page Mode)	L	L	↕	Column Address

H = High; L = Low; X = Don't Care; ↕ = Transitioning

### Write-Per-Bit Operation

The DM2M36SJ EDRAM SIMM provides a write-per-bit capability to selectively modify individual parity bits ( $DQ_{8,17,26,35}$ ) for byte write operations. The parity device (DM2212) is selected via /CAL<sub>p</sub>. Data bits do not require or support write-per-bit capability. Byte write selection to non-parity bits is accomplished via /CAL<sub>0-3</sub>. The bits to be written are determined by a bit mask data word which is placed on the parity I/O data pins prior to clocking /RE. The logic one bits in the mask data select the bits to be written. As soon as the mask is latched by /RE, the mask data is removed and write data can be placed on the

databus. The mask is only specified on the /RE transition. During page mode burst write operations, the same mask is used for all write operations.

### Internal Refresh

If /F is active (low) on the assertion of /RE, an internal refresh cycle is executed. This cycle refreshes the row address supplied by an internal refresh counter. This counter is incremented at the end of the cycle in preparation for the next /F type refresh cycle. When /F type refreshing is used, at least 1,024 /F cycles must be executed every 64ms. /F refresh cycles can be hidden because cache memory can be read under column address control throughout the entire /F cycle. /F cycles are the only active cycles during which /S can be disabled. In this case, the output remains disabled.

### /CAL Before /RE Refresh ("CAS Before /RAS")

/CAL before /RE refresh, a special case of internal refresh, is discussed in the "Reduced Pin Count Operation" section below.

### /RE Only Refresh Operation

Although /F refresh using the internal refresh counter is the recommended method of EDRAM refresh, it is possible to perform an /RE only refresh using an externally supplied row address. /RE refresh is performed by executing a *write cycle* (W/R and /F are high) where /CAL is not clocked. This is necessary so that the current cache contents and LRR are not modified by the refresh operation. All combinations of addresses  $A_{3,5}$  must be sequenced every 64ms refresh period.  $A_{10}$  does not need to be cycled. Read refresh cycles are not allowed because a DRAM refresh cycle does not occur when a read refresh address matches the LRR address latch.

### Low Power Mode

The EDRAM enters its low power mode when /S is high. In this mode, the internal DRAM circuitry is powered down to reduce standby current to 1mA.

### Initialization Cycles

A minimum of 10 initialization (start-up) cycles are required before normal operation is guaranteed. A combination of eight /F refresh cycles and two read cycles to different row addresses are necessary to complete initialization.

### Unallowed Mode

Read, write, or /RE only operations must not be initiated to unselected memory banks by clocking /RE when /S is high.

### Reduced Pin Count Operation

Although it is desirable to use all EDRAM control pins to optimize system performance, it is possible to simplify the interface to the EDRAM by either tying pins to ground or by tying one or more control inputs together. The /S input can be tied to ground if the low power standby mode is not required. The /CAL and /F pins can be tied together if hidden refresh operation is not required. In this case, a CBR refresh (/CAL before /RE) can be performed by holding the combined input low prior to /RE. The /WE input can be tied to /CAL if independent posting of column addresses and data are not required during write operations. In this case, both column address and write data will be latched by the combined input during writes. If these techniques are used, the EDRAM will require only four control lines for operation (/RE, /CAS [combined /CAL, /F, and /WE], W/R, and /G). The simplified control interface still allows the fast page read/write cycle times, fast random read/write times, and hidden precharge functions available with the EDRAM.

## Pinout

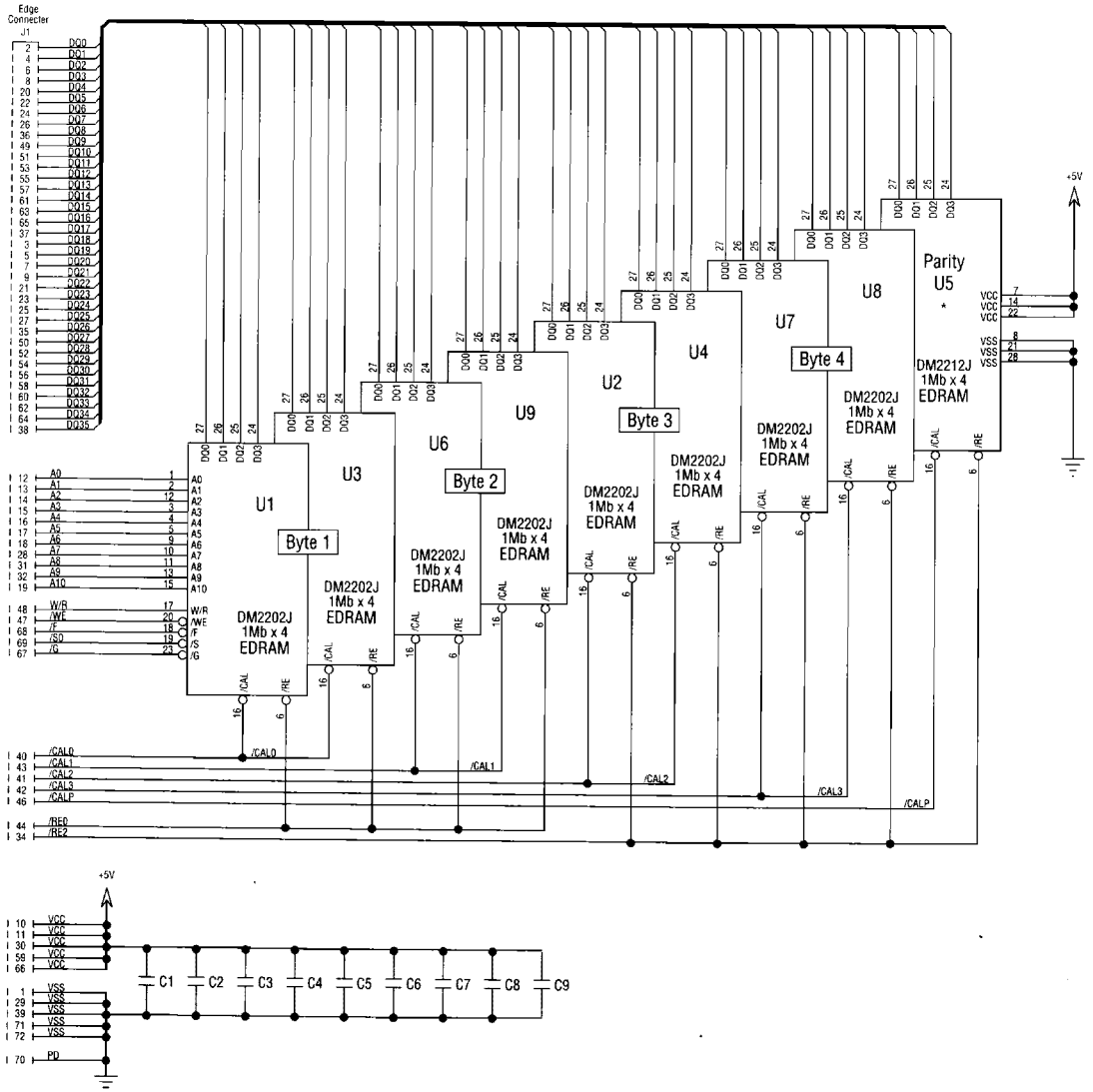
Pin No.	Function	Interconnect (Component Pin)	Organization
1	GND	C (8,21,28)	Ground
2	DQ <sub>0</sub>	U1,10 (27)	Byte 1 I/O 1
3	DQ <sub>18</sub>	U2,11 (24)	Byte 3 I/O 1
4	DQ <sub>1</sub>	U1,10 (26)	Byte 1 I/O 2
5	DQ <sub>19</sub>	U2,11 (25)	Byte 3 I/O 2
6	DQ <sub>2</sub>	U1,10 (25)	Byte 1 I/O 3
7	DQ <sub>20</sub>	U2,11 (26)	Byte 3 I/O 3
8	DQ <sub>3</sub>	U1,10 (24)	Byte 1 I/O 4
9	DQ <sub>21</sub>	U2,11 (27)	Byte 3 I/O 4
10	+5 Volts	C (7,14,22)	V <sub>CC</sub>
11	+5 Volts	C (7,14,22)	V <sub>CC</sub>
12	A <sub>0</sub>	C (1)	Address
13	A <sub>1</sub>	C (2)	Address
14	A <sub>2</sub>	C (12)	Address
15	A <sub>3</sub>	C (3)	Address
16	A <sub>4</sub>	C (4)	Address
17	A <sub>5</sub>	C (5)	Address
18	A <sub>6</sub>	C (9)	Address
19	A <sub>10</sub>	C (15)	Address
20	DQ <sub>4</sub>	U3,12 (27)	Byte 1 I/O 5
21	DQ <sub>22</sub>	U4,13 (24)	Byte 3 I/O 5
22	DQ <sub>5</sub>	U3,12 (26)	Byte 1 I/O 6
23	DQ <sub>23</sub>	U4,13 (25)	Byte 3 I/O 6
24	DQ <sub>6</sub>	U3,12 (25)	Byte 1 I/O 7
25	DQ <sub>24</sub>	U4,13 (26)	Byte 3 I/O 7
26	DQ <sub>7</sub>	U3,12 (24)	Byte 1 I/O 8
27	DQ <sub>25</sub>	U4,13 (27)	Byte 3 I/O 8
28	A <sub>7</sub>	C (10)	Address
29	GND	C (8,21,28)	Ground
30	+5 Volts	C (7,14,22)	V <sub>CC</sub>
31	A <sub>8</sub>	C (11)	Address
32	A <sub>9</sub>	C (13)	Address
33	/RE <sub>3</sub>	U10-18 (6)	Bank 1 Row Enable
34	/RE <sub>2</sub>	U2,4,5,7,8 (6)	Bank 0 Row Enable (Bytes 3,4, Parity)
35	DQ <sub>26</sub> *	U5,14 (27)	Parity I/O for Byte 3
36	DQ <sub>8</sub> *	U5,14 (26)	Parity I/O for Byte 1

Pin No.	Function	Interconnect (Component Pin)	Organization
37	DQ <sub>17</sub> *	U5,14 (25)	Parity I/O for Byte 2
38	DQ <sub>35</sub> *	U5,14 (24)	Parity I/O for Byte 4
39	GND	C (8,21,28)	Ground
40	/CAL <sub>0</sub>	U1,3,10,12 (16)	Byte 1 Column Address Latch
41	/CAL <sub>2</sub>	U2,4,11,13 (16)	Byte 3 Column Address Latch
42	/CAL <sub>3</sub>	U7,8,16,17 (16)	Byte 4 Column Address Latch
43	/CAL <sub>1</sub>	U6,9,15,18 (16)	Byte 2 Column Address Latch
44	/RE <sub>0</sub>	U1,3,6,9 (6)	Bank 0 Row Enable (Bytes 1,2)
45	/S <sub>1</sub>	U10-18 (19)	Chip Select Bank 1
46	/CAL <sub>P</sub> *	U5,14 (16)	Parity Column Address Latch
47	/WE	C (20)	Write Enable
48	W/R	C (17)	W/R Mode Control
49	DQ <sub>9</sub>	U6,15 (27)	Byte 2 I/O 1
50	DQ <sub>27</sub>	U7,16 (27)	Byte 4 I/O 1
51	DQ <sub>10</sub>	U6,15 (26)	Byte 2 I/O 2
52	DQ <sub>28</sub>	U7,16 (26)	Byte 4 I/O 2
53	DQ <sub>11</sub>	U6,15 (25)	Byte 2 I/O 3
54	DQ <sub>29</sub>	U7,16 (25)	Byte 4 I/O 3
55	DQ <sub>12</sub>	U6,15 (24)	Byte 2 I/O 4
56	DQ <sub>30</sub>	U7,16 (24)	Byte 4 I/O 4
57	DQ <sub>13</sub>	U9,18 (24)	Byte 2 I/O 5
58	DQ <sub>31</sub>	U8,17 (24)	Byte 4 I/O 5
59	+5 Volts	C (7,14,22)	V <sub>CC</sub>
60	DQ <sub>32</sub>	U8,17 (26)	Byte 4 I/O 6
61	DQ <sub>14</sub>	U9,18 (25)	Byte 2 I/O 6
62	DQ <sub>33</sub>	U8,17 (25)	Byte 4 I/O 7
63	DQ <sub>15</sub>	U9,18 (26)	Byte 2 I/O 7
64	DQ <sub>34</sub>	U8,17 (24)	Byte 4 I/O 8
65	DQ <sub>16</sub>	U9,18 (27)	Byte 2 I/O 8
66	+5 Volts	C (7,14,22)	V <sub>CC</sub>
67	/G	C (23)	Output Enable
68	/F	C (18)	Refresh Mode Control
69	/S <sub>0</sub>	U1-9 (19)	Chip Select Bank 0
70	PD	Signal GND	Presence Detect
71	GND	C (8,21,28)	Ground
72	GND	C (8,21,28)	Ground

C = Common to All Memory Chips, U1 = Chip 1, etc.

\*No Connect for DM2M32SJ

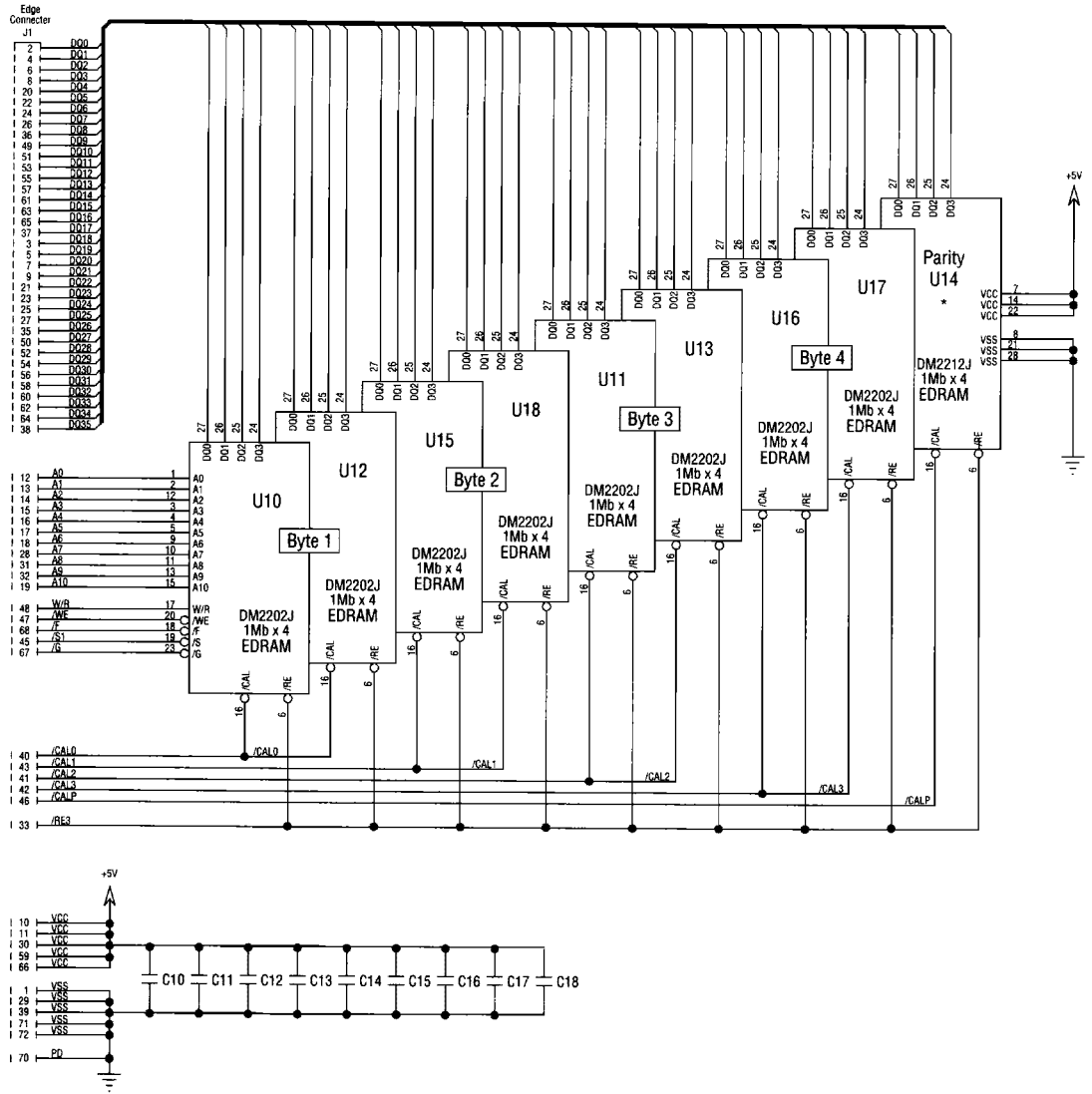
# Interconnect Diagram — Bank 0 (Components Mounted on Front Side)



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\*DM2212 is not present on the DM2M32SJ.

# Interconnect Diagram — Bank 1 (Components Mounted on Back Side)



\*DM2212 is not present on the DM2M32SJ.

## Pin Descriptions

### ***/RE<sub>0,2,3</sub>* — Row Enable**

This input is used to initiate DRAM read and write operations and latch a row address as well as the states of W/R and /E. It is not necessary to clock /RE to read data from the EDRAM SRAM row registers. On read operations, /RE can be brought high as soon as data is loaded into cache to allow early precharge.

### ***/CAL<sub>0-3,P</sub>* — Column Address Latch**

This input is used to latch the column address and in combination with /WE to trigger write operations. When /CAL is high, the column address latch is transparent. When /CAL is low, the column address is closed and the output of the latch contains the address present while /CAL was high. /CAL can be toggled when /RE is low or high. However, /CAL must be high during the high-to-low transition of /RE except for /F refresh cycles.

### ***W/R* — Write/Read**

This input along with /F specifies the type of DRAM operation initiated on the low going edge of /RE. When /F is high, W/R specifies either a write (logic high) or read operation (logic low).

### ***/F* — Refresh**

This input will initiate a DRAM refresh operation using the internal refresh counter as an address source when it is low on the low going edge of /RE.

### ***/WE* — Write Enable**

This input controls the latching of write data on the input data pins. A write operation is initiated when both /CAL and /WE are low.

## Absolute Maximum Ratings

(Beyond Which Permanent Damage Could Result)

Description	Ratings
Input Voltage ( $V_{IN}$ )	- 1 ~ 7v
Output Voltage ( $V_{OUT}$ )	- 1 ~ 7v
Power Supply Voltage ( $V_{CC}$ )	- 1 ~ 7v
Ambient Operating Temperature ( $T_A$ )	0 ~ 70°C
Storage Temperature ( $T_S$ )	-55 ~ 150°C
Static Discharge Voltage (Per MIL-STD-883 Method 3015)	>2000V
Short Circuit O/P Current ( $I_{OUT}$ )	50mA*

\* One output at a time per device; short duration

### ***/G* — Output Enable**

This input controls the gating of read data to the output data pin during read operations.

### ***/S<sub>0,1</sub>* — Chip Select**

This input is used to power up the I/O and clock circuitry. When /S is high, the EDRAM remains in a powered-down condition; read and write cycles cannot be executed while /S is high. /S must remain active throughout any read or write operation. Only the /F refresh operation can be executed when /S is high.

### ***DQ<sub>0-35</sub>* — Data Input/Output**

These bidirectional data pins are used to read and write data to the EDRAM. On the DM2212 write-per-bit memory, these pins are also used to specify the bit mask used during write operations.

### ***A<sub>0-10</sub>* — Multiplex Address**

These inputs are used to specify the row and column addresses of the EDRAM data. The 11-bit row address is latched on the falling edge of /RE. The 9-bit column address can be specified at any other time to select read data from the SRAM cache or to specify the write column address during write cycles.

### ***V<sub>CC</sub>* Power Supply**

These inputs are connected to the +5 volt power supply.

### ***V<sub>SS</sub>* Ground**

These inputs are connected to the power supply ground connection.

## Capacitance

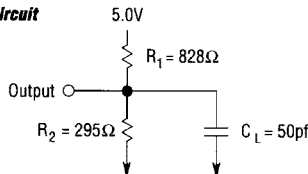
Description	Max*	Pins
Input Capacitance	130/136pf	A <sub>0-9</sub>
Input Capacitance	165/180pf	A <sub>10</sub> , W/R, /WE, /F
Input Capacitance	97/100pf	/S <sub>0</sub> , /S <sub>1</sub>
Input Capacitance	52/55pf	/RE <sub>0</sub>
Input Capacitance	55/65pf	/RE <sub>2</sub>
Input Capacitance	92/92pf	/RE <sub>3</sub>
Input Capacitance	62/62pf	/G
Input Capacitance	52/55pf	/CAL <sub>0-3</sub>
Input Capacitance	32pf	/CAL <sub>P</sub>
I/O Capacitance	16pf	DQ <sub>0-35</sub>

\* DM2M32SJ/DM2M36SJ, respectively

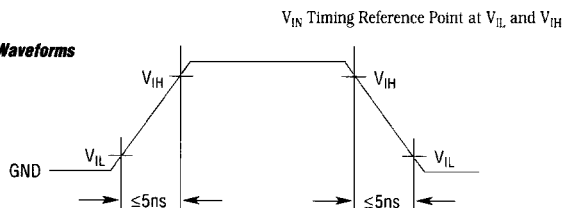
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## AC Test Load and Waveforms

### Load Circuit



### Input Waveforms



## Electrical Characteristics

( $T_A = 0 - 70^\circ\text{C}$ )

Symbol	Parameters	Min	Max	Test Conditions
$V_{CC}$	Supply Voltage	4.75V	5.25V	All Voltages Referenced to $V_{SS}$
$V_{IH}$	Input High Voltage	2.4V	6.5V	
$V_{IL}$	Input Low Voltage	-1.0V	0.8V	
$V_{OH}$	Output High Level	2.4V	—	$I_{OUT} = -5\text{mA}$
$V_{OL}$	Output Low Level	—	0.4V	$I_{OUT} = 4.2\text{mA}$
$I_{i(L)}$	Input Leakage Current	-10 $\mu\text{A}$	10 $\mu\text{A}$	$0\text{V} \leq V_{IN} \leq 6.5\text{V}$ , All Other Pins Not Under Test = 0V
$I_{O(L)}$	Output Leakage Current	-10 $\mu\text{A}$	10 $\mu\text{A}$	$0\text{V} \leq V_{IN}$ , $0\text{V} \leq V_{OUT} \leq 5.5\text{V}$

### Operating Current — DM2M32SJ

Symbol	Operating Current	33MHz Typ <sup>(1)</sup>	-15 Max	-20 Max	Test Condition	Notes
$I_{CC1}$	Random Read	880mA	1800mA	1440mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
$I_{CC2}$	Fast Page Mode Read	520mA	1160mA	920mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
$I_{CC3}$	Static Column Read	440mA	880mA	720mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
$I_{CC4}$	Random Write	1080mA	1520mA	1200mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
$I_{CC5}$	Fast Page Mode Write	400mA	1080mA	840mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
$I_{CC6}$	Standby	16mA	16mA	16mA	All Control Inputs Stable $\geq V_{CC} - 0.2\text{V}$	
$I_{CCT}$	Average Typical Operating Current	240mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

### Operating Current — DM2M36SJ

Symbol	Operating Current	33MHz Typ <sup>(1)</sup>	-15 Max	-20 Max	Test Condition	Notes
$I_{CC1}$	Random Read	990mA	2025mA	1620mA	/RE, /CAL, /G and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
$I_{CC2}$	Fast Page Mode Read	585mA	1305mA	1035mA	/CAL, /G and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
$I_{CC3}$	Static Column Read	495mA	990mA	810mA	/G and Addresses Cycling: $t_{SC} = t_{SC}$ Minimum	2, 4
$I_{CC4}$	Random Write	1215mA	1710mA	1350mA	/RE, /CAL, /WE and Addresses Cycling: $t_C = t_C$ Minimum	2, 3
$I_{CC5}$	Fast Page Mode Write	450mA	1215mA	945mA	/CAL, /WE and Addresses Cycling: $t_{PC} = t_{PC}$ Minimum	2, 4
$I_{CC6}$	Standby	18mA	18mA	18mA	All Control Inputs Stable $\geq V_{CC} - 0.2\text{V}$	
$I_{CCT}$	Average Typical Operating Current	270mA	—	—	See "Estimating EDRAM Operating Power" Application Note	1

(1) "33MHz Typ" refers to worst case  $I_{CC}$  expected in a system operating with a 33MHz memory bus. In this typical example, page mode and random reads refer to page burst hits and misses. Writes are two clock cycle random and page mode writes. See power applications note for further details. This parameter is not 100% tested or guaranteed.

(2)  $I_{CC}$  is dependent on cycle rates and is measured with CMOS levels and the outputs open.

(3)  $I_{CC}$  is measured with a maximum of one address change while /RE =  $V_{IL}$ .

(4)  $I_{CC}$  is measured with a maximum of one address change while /CAL =  $V_{IH}$ .

## Switching Characteristics

Discrete devices have been tested from 4.7V to 5.3V  $V_{CC}$  and to 75°C to guarantee SIMM specifications. ( $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0$  to 70°C,  $C_L = 50\text{pf}$ )

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
$t_{AC}^{(1)}$	Column Address Access Time		15		20	ns
$t_{ACH}$	Column Address Valid to /CAL Inactive (Write Cycle)	15		20		ns
$t_{AQX}$	Column Address Change to Output Data Invalid	5		5		ns
$t_{ASC}$	Column Address Setup Time	5		5		ns
$t_{ASR}$	Row Address Setup Time	5		6		ns
$t_C$	Row Enable Cycle Time	65		85		ns
$t_{C1}$	Row Enable Cycle Time, Cache Hit (Row=LRR), Read Cycle Only	25		32		ns
$t_{CA}$	Address Cycle Time (Cache Hits)	15		20		ns
$t_{CAE}$	Column Address Latch Active Time	6		7		ns
$t_{CAH}$	Column Address Hold Time	0		1		ns
$t_{CDR}^{(2)}$	Column Address Delay from /RE Low, After /CAL Assertion in a Write Hit Cycle	35		45		ns
$t_{CH}$	Column Address Latch High Time (Latch Transparent)	5		7		ns
$t_{CHR}$	/CAL Inactive Lead Time to /RE Inactive (Write Cycles Only)	-1		-1		ns
$t_{CHW}$	Column Address Latch High to Write Enable Low (Multiple Writes)	0		0		ns
$t_{CQV}$	Column Address Latch High to Data Valid		17		20	ns
$t_{CQX}$	Column Address Latch Inactive to Data Invalid	5		5		ns
$t_{CRP}$	Column Address Latch Setup Time to Row Enable	5		6		ns
$t_{CWL}$	/WE Low to /CAL Inactive	5		7		ns
$t_{DH}$	Data Input Hold Time	0		1		ns
$t_{DMH}$	Mask Hold Time From Row Enable (Write-Per-Bit)	1.5		2		ns
$t_{DMS}$	Mask Setup Time to Row Enable (Write-Per-Bit)	5		6		ns
$t_{DS}$	Data Input Setup Time	5		6		ns
$t_{GQV}^{(1)}$	Output Enable Access Time		5		6	ns
$t_{GOX}^{(3,4)}$	Output Enable to Output Drive Time	0	5	0	6	ns
$t_{GQZ}^{(5,6)}$	Output Turn-Off Delay From Output Disabled (/G $\uparrow$ )	0	5	0	6	ns
$t_{MH}$	/F and W/R Mode Select Hold Time	0		1		ns
$t_{MSU}$	/F and W/R Mode Select Setup Time	5		6		ns
$t_{NRH}$	/CAL, /G, and /WE Hold Time For /RE-Only Refresh	0		0		ns
$t_{NRS}$	/CAL, /G, and /WE Setup Time For /RE-Only Refresh	5		6		ns
$t_{PC}$	Column Address Latch Cycle Time	15		20		ns
$t_{RAC}^{(1)}$	Row Enable Access Time, On a Cache Miss		35		45	ns
$t_{RAC1}^{(1)}$	Row Enable Access Time, On a Cache Hit (Limit Becomes $t_{AC}$ )		17		22	ns
$t_{RAC2}^{(1,7)}$	Row Enable Access Time for a Cache Write Hit		35		45	ns
$t_{RAH}$	Row Address Hold Time	1.5		2		ns
$t_{RE}$	Row Enable Active Time	35	100000	45	100000	ns

## Switching Characteristics (continued)

Discrete devices have been tested from 4.7V to 5.3V  $V_{CC}$  and to 75°C to guarantee SIMM specifications. ( $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0$  to 70°C,  $C_L = 50pF$ )

Symbol	Description	-15		-20		Units
		Min	Max	Min	Max	
$t_{RE1}$	Row Enable Active Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
$t_{REF}$	Refresh Period		64		64	ms
$t_{RGX}$	Output Enable Don't Care From Row Enable (Write, Cache Miss), O/P Hi Z	10		13		ns
$t_{RP}^{(8)}$	Row Precharge Time	25		32		ns
$t_{RP1}$	Row Precharge Time, Cache Hit (Row=LRR) Read Cycle	10		13		ns
$t_{RRH}$	Read Hold Time From Row Enable (Write Only)	0		1		ns
$t_{RSH}$	Last Write Address Latch to End of Write	15		20		ns
$t_{RSW}$	Row Enable to Column Address Latch Low For Second Write	40		51		ns
$t_{RWL}$	Last Write Enable to End of Write	15		20		ns
$t_{SC}$	Column Address Cycle Time	15		20		ns
$t_{SHR}$	Select Hold From Row Enable	0		1		ns
$t_{SQV}^{(1)}$	Chip Select Access Time		15		20	ns
$t_{SQX}^{(3,4)}$	Output Turn-On From Select Low	0	15	0	20	ns
$t_{SQZ}^{(5,6)}$	Output Turn-Off From Chip Select	0	10	0	13	ns
$t_{SSR}$	Select Setup Time to Row Enable	5		6		ns
$t_T$	Transition Time (Rise and Fall)	1	10	1	10	ns
$t_{WC}$	Write Enable Cycle Time	15		20		ns
$t_{WCH}$	Column Address Latch Low to Write Enable Inactive Time	5		7		ns
$t_{WHR}^{(9)}$	Write Enable Hold After /RE	0		1		ns
$t_{WI}$	Write Enable Inactive Time	5		7		ns
$t_{WP}$	Write Enable Active Time	5		7		ns
$t_{WQV}^{(1)}$	Data Valid From Write Enable High		15		20	ns
$t_{WQX}^{(3,6)}$	Data Output Turn-On From Write Enable High	0	15	0	20	ns
$t_{WQZ}^{(4,5)}$	Data Turn-Off From Write Enable Low	0	15	0	20	ns
$t_{WRP}$	Write Enable Setup Time to Row Enable	5		5		ns
$t_{WRR}$	Write to Read Recovery (Cache Miss)		15		20	ns

(1)  $V_{OUT}$  Timing Reference Point at 1.5V

(2) Column Address is Ignored Prior to  $t_{CDR}$  for This Specific Cycle

(3) Parameter Defines Time When Output is Enabled (Sourcing or Sinking Current) and is Not Referenced to  $V_{OH}$  or  $V_{OL}$

(4) Minimum Specification is Referenced from  $V_{IH}$  and Maximum Specification is Referenced from  $V_{IL}$  on Input Control Signal

(5) Parameter Defines Time When Output Achieves Open-Circuit Condition and is Not Referenced to  $V_{OH}$  or  $V_{OL}$

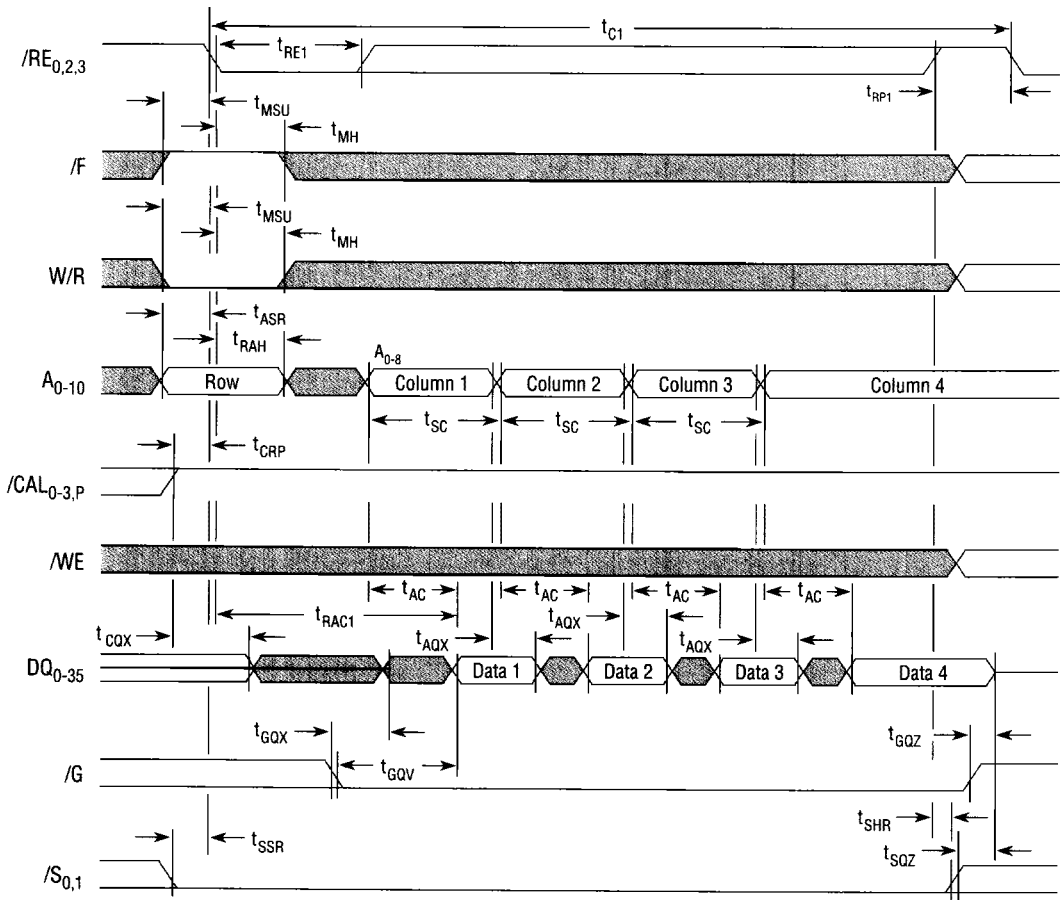
(6) Minimum Specification is Referenced from  $V_{IL}$  and Maximum Specification is Referenced from  $V_{IH}$  on Input Control Signal

(7) Access Parameter Applies When /CAL Has Not Been Asserted Prior to  $t_{RAC2}$

(8) For Back-to-Back /F Refreshes,  $t_{RP} = 40ns$ . For Non-consecutive /F Refreshes,  $t_{RP} = 25ns$  and  $32ns$  Respectively

(9) For Write-Per-Bit Devices,  $t_{WHR}$  is Limited By Data Input Setup Time,  $t_{DS}$

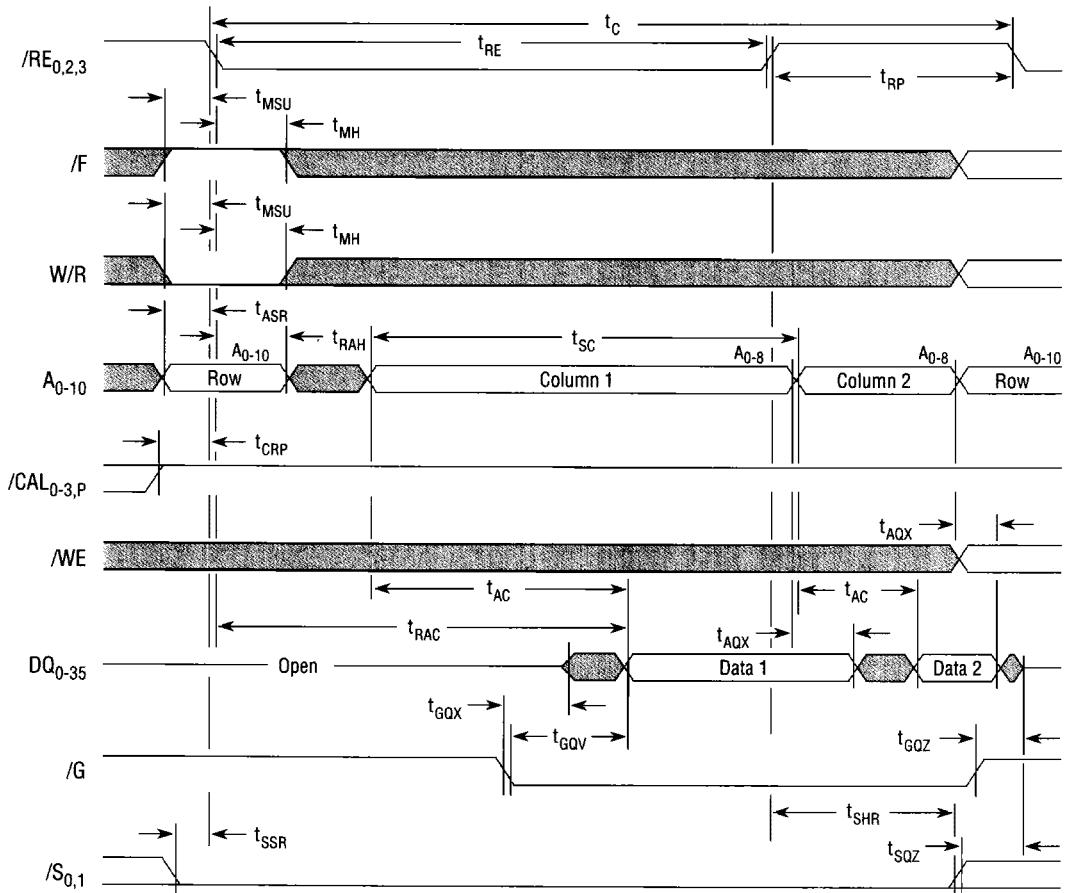
***/RE Active Cache Read Hit (Static Column Mode)***



Don't Care or Indeterminate

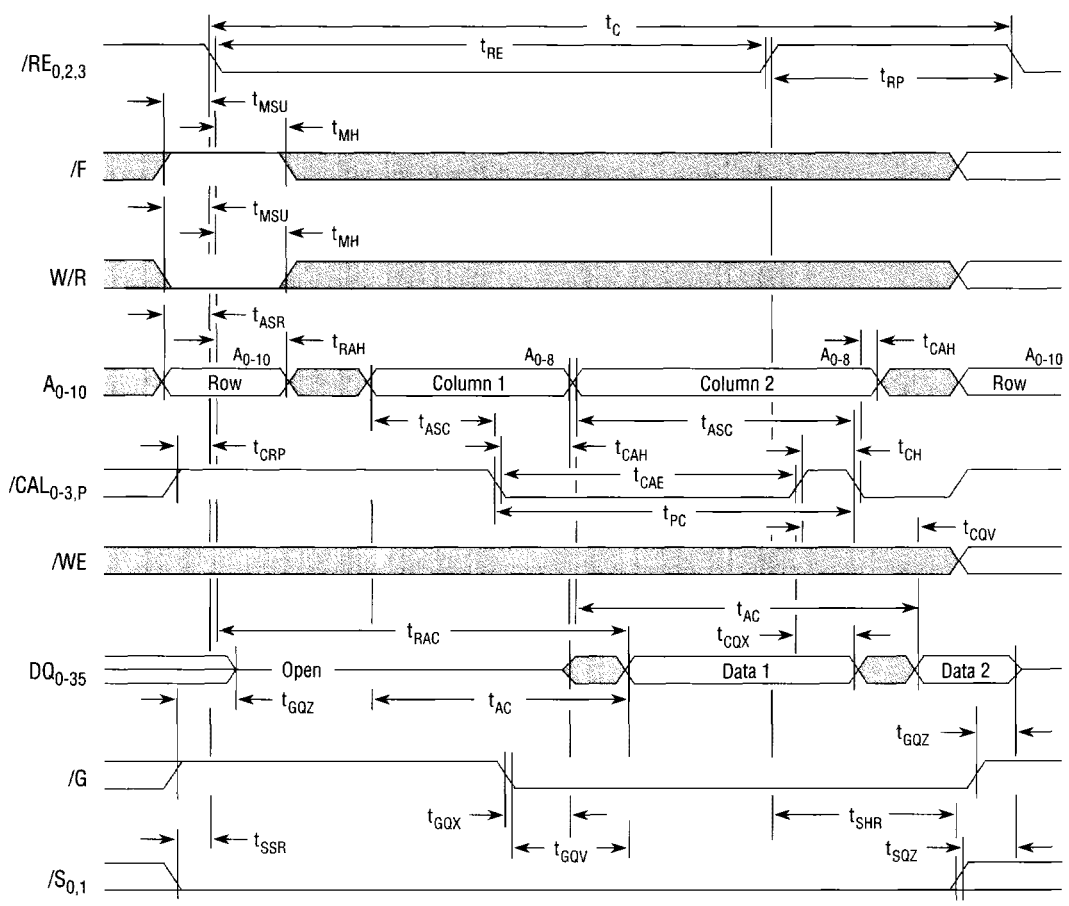


***/RE Active Cache Read Miss (Static Column Mode)***



Don't Care or Indeterminate 

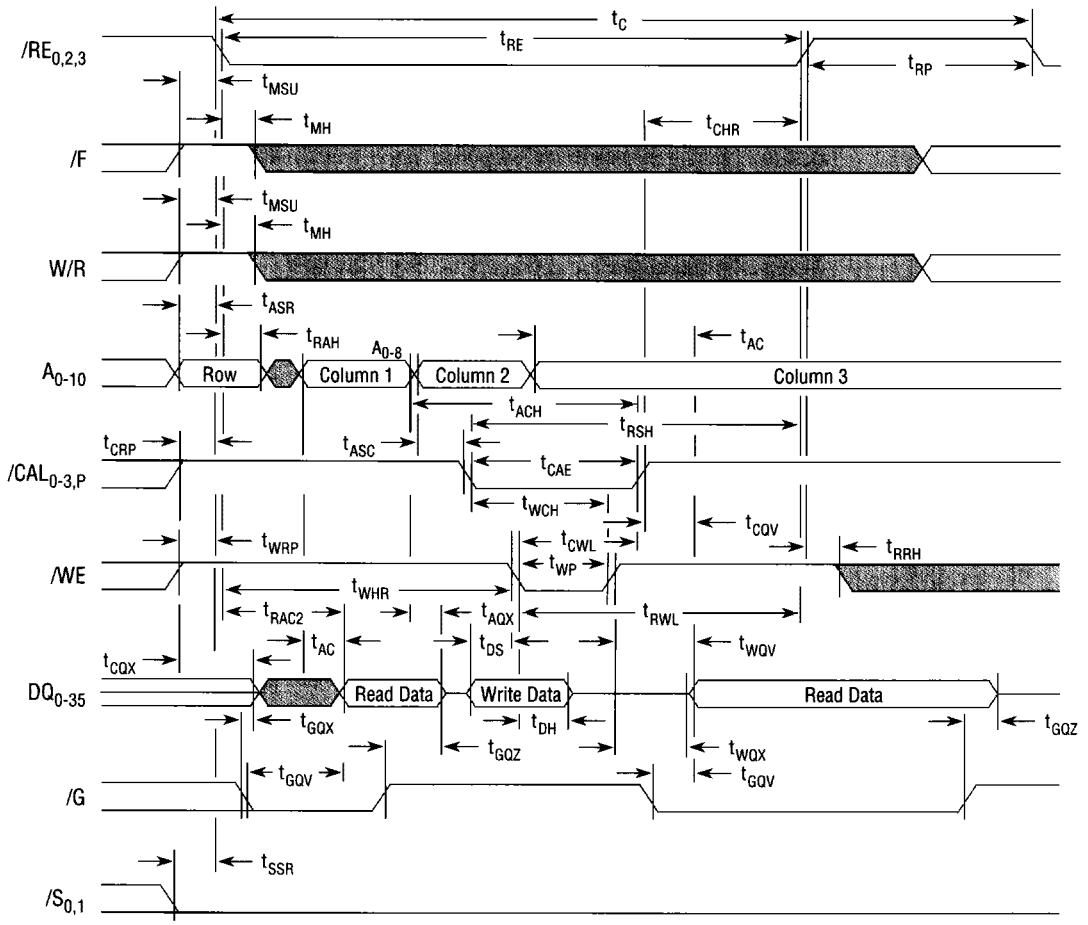
**/RE Active Cache Read Miss (Page Mode)**



Don't Care or Indeterminate



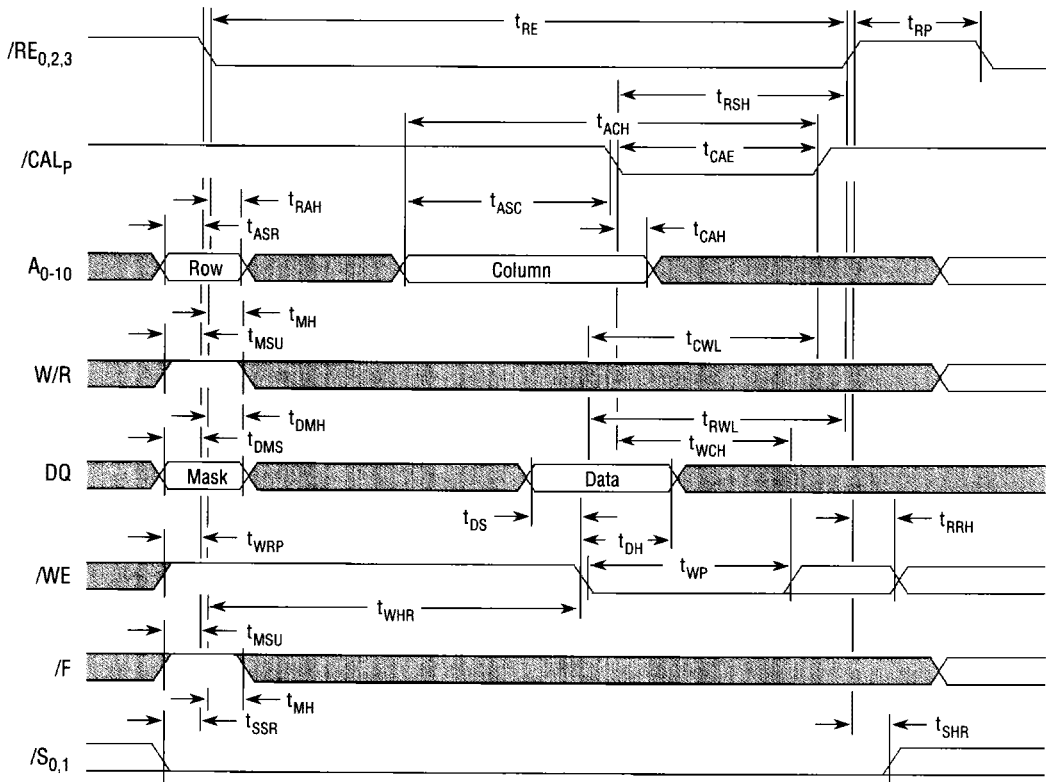
**Page Read/Write During Write Hit Cycle (Can Include Read-Modify-Write)**




Don't Care or Indeterminate

- NOTES: 1. If column address 1 equals column address 2, then a read-modify-write cycle is performed.  
 2. Parity bits  $DQ_{8,17,26,35}$  must have mask provided at falling edge of  $\overline{RE}$ .

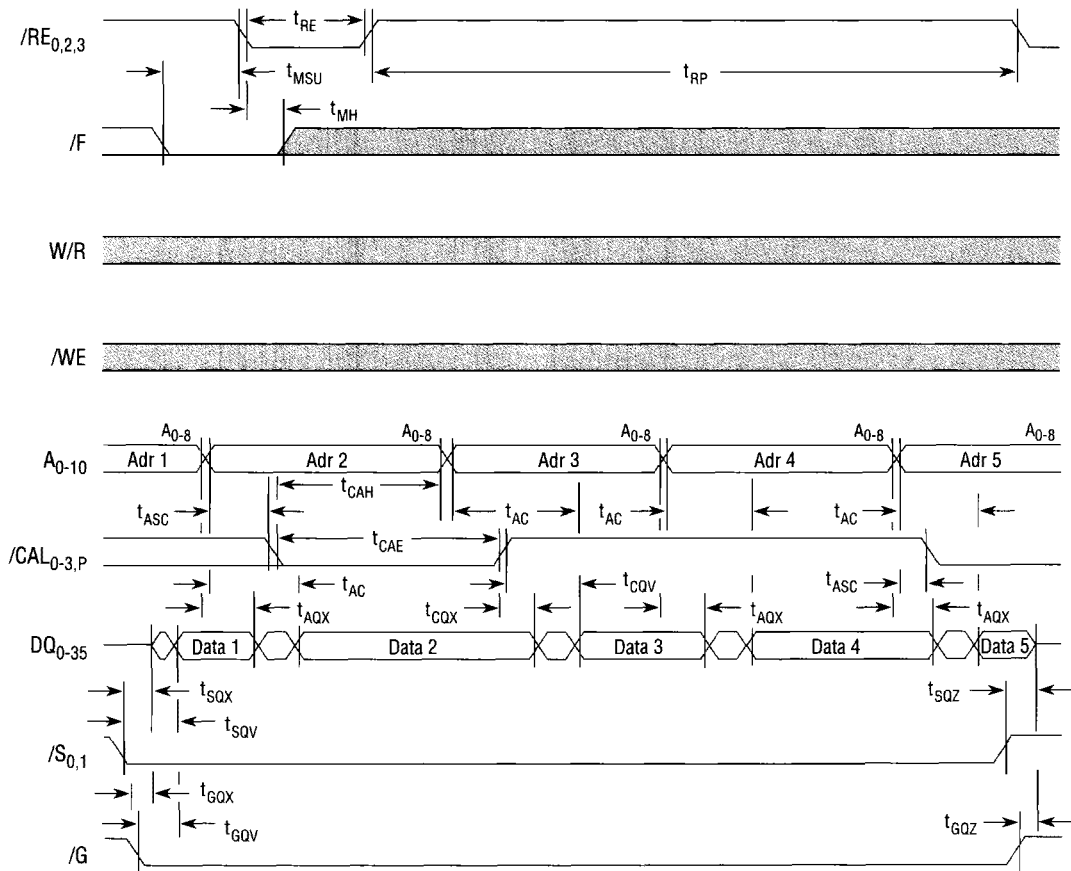
### Write-Per-Bit Cycle ( $\bar{G} = \text{High}$ )



Don't Care or Indeterminate 

- NOTES:
1. Data mask bit high (1) enables bit write; data mask bit low (0) inhibits bit write.
  2. Two X4 EDRAM options are available, one with write-per-bit (DM2212) and one without write-per-bit (DM2202).
  3. Write-per-bit waveform applies to parity bits only ( $DQ_{8,17,26,35}$ ).

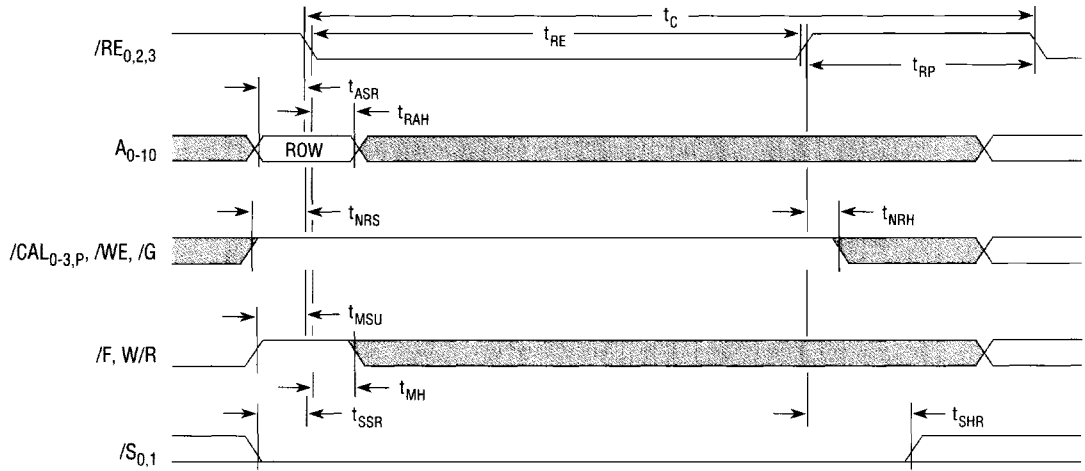
***/F Refresh (Including "CAS Before RAS") with Page Mode and Static Column Cache Reads***



Don't Care or Indeterminate 

- NOTES: 1. During  $/F$  refresh cycles,  $/S$  is a don't care unless cache reads are performed. For cache reads,  $/S$  must be low.  
 2. If  $/CAL$  is low when  $/RE$  falls, a "CAS before RAS" type refresh occurs.

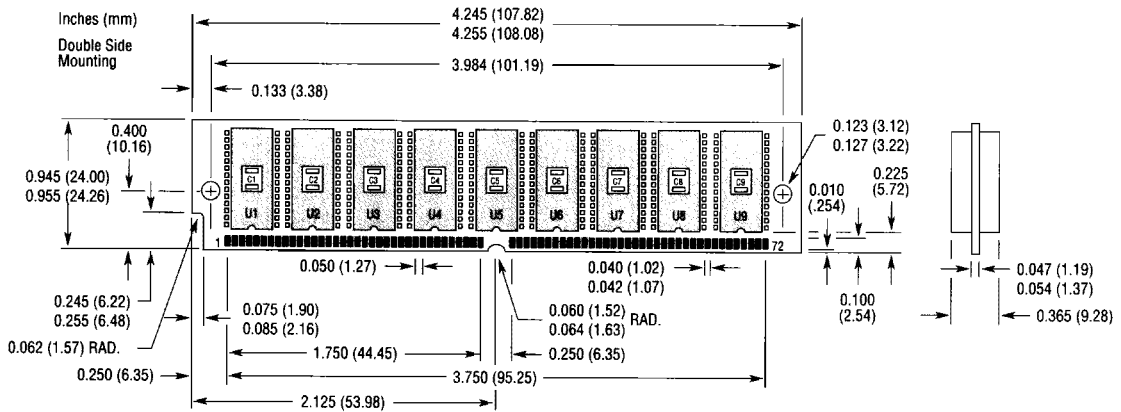
**/RE-Only Refresh**



Don't Care or Indeterminate

NOTES: 1. All binary combinations of A<sub>0-9</sub> must be refreshed every 64ms interval. A<sub>10</sub> does not have to be cycled, but must remain valid during row address setup and hold times.

## Mechanical Data 72 Pin SIMM Module



U1-U4, U6-U9, U10-U13, U15-U17 — Ramtron DM2202J-XX, 1M x 4 EDRAMs, 300 Mil SOJ  
 U5, U14 — Ramtron DM2212J-XX, 1M x 4 EDRAM with Write-Per-Bit (Not present on DM2M32SJ)  
 C1-C18 — 0.22µF Chip Capacitors  
 Socket — Molex 78441-7202 or Equivalent

## Part Numbering System

**DM2M36SJ - 15**

**Access Time from Cache in Nanoseconds**

15ns  
20ns

**Packaging System**

J = 300 Mil, Plastic SOJ

**Memory Module Configuration**

S = SIMM

**I/O Width (Including Parity)**

32 = 32 Bits  
36 = 36 Bits  
40 = 40 Bits

**Memory Depth (Megabits)**

1M  
2M  
4M

**Dynamic Memory**