Am4055/5055 • Am4056/5056 • Am4057/5057

Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers

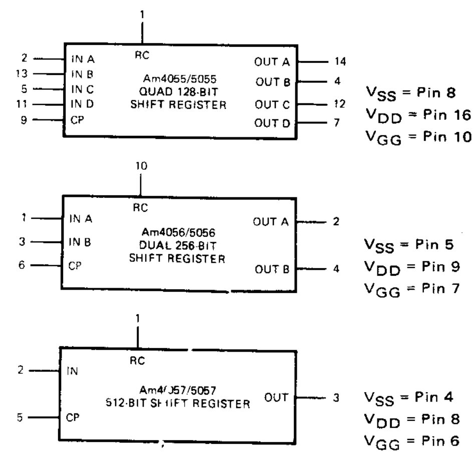
Distinctive Characteristics

- Internal recirculate
- Single TTL compatible clock
- Operation guaranteed from DC to 1.5MHz
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

These devices are a family of static P-channel MOS shift registers in three configurations. The Am4055/5055 is a quad 128-bit register; the Am4056/5056 is a dual 256-bit register; and the Am4057/5057 is a single 512-bit register. All three devices include on chip recirculate. The registers are all clocked by a single low-level clock input. Because the registers are static, the clock may be stopped indefinitely in the LOW state without loss of data. Each of the registers has a single data input; data on the input is written into the register on the HIGH-to-LOW clock edge. A single recirculate control (RC) on each chip determines whether the registers on that chip are to write data in from the data inputs or recirculate the data appearing on the output. If RC is LOW, new data is written in; if RC is HIGH then the data on the output will be written back into the register input on the next clock pulse.

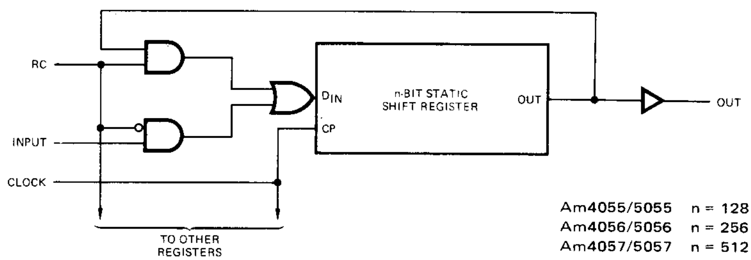
LOGIC SYMBOLS



MOS-450

5

LOGIC BLOCK DIAGRAM
(One Register Shown)



Am4055/5055 n = 128
Am4056/5056 n = 256
Am4057/5057 n = 512

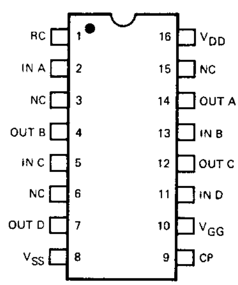
MOS-451

ORDERING INFORMATION

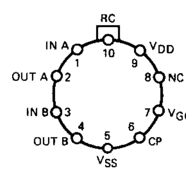
Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +70°C	MM5055N
16-Pin Hermetic DIP	0°C to +70°C	MM5055D
16-Pin Hermetic DIP	−55°C to +125°C	MM4055D
TO-100 Can	0°C to +70°C	MM5056H
TO-100 Can	−55°C to +125°C	MM4056H
8-Pin Molded DIP	0°C to +70°C	MM5057N
8-Pin Hermetic DIP	0°C to +70°C	MM5057D
8-Pin Hermetic DIP	−55°C to +125°C	MM4057D

CONNECTION DIAGRAMS

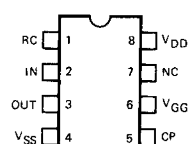
Am4055/5055



Am4056/5056



Am4057/5057



MOS-452

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −10V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −20V to V_{SS} +0.3V

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Am4055 Am4056 Am4057	−55°C to +125°C	5.0V ±5%	0V	−12V ±5%
Am5055 Am5056 Am5057	0°C to +70°C	5.0V ±5%	0V	−12V ±5%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −0.5mA		2.4			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA				0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	4055/6/7	V_{SS}−1.0		V_{SS}+0.3	Volts
			5055/6/7	V_{SS}−1.5		V_{SS}+0.3	
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		V_{SS}−18.5		V_{SS}−4.2	Volts
I_{IL}	Input Leakage Current	V_{IN} = −10.0V, all other pins GND, T_A = 25°C			0.01	0.5	μA
I_{DD}	V_{DD} Power Supply Current	T_A = 25°C, $t_{\phi pw}H$ = 160 ns Data = 1010. . . output open	f ≤ 2.2MHz		15.0	20.0	mA
			f ≤ 10KHz		13.0	18.0	
I_{GG}	V_{GG} Power Supply Current		f ≤ 1.6MHz		10.5	15.5	
			f ≤ 2.2MHz		13.0	19.0	
			f ≤ 10KHz		6.5	9.0	

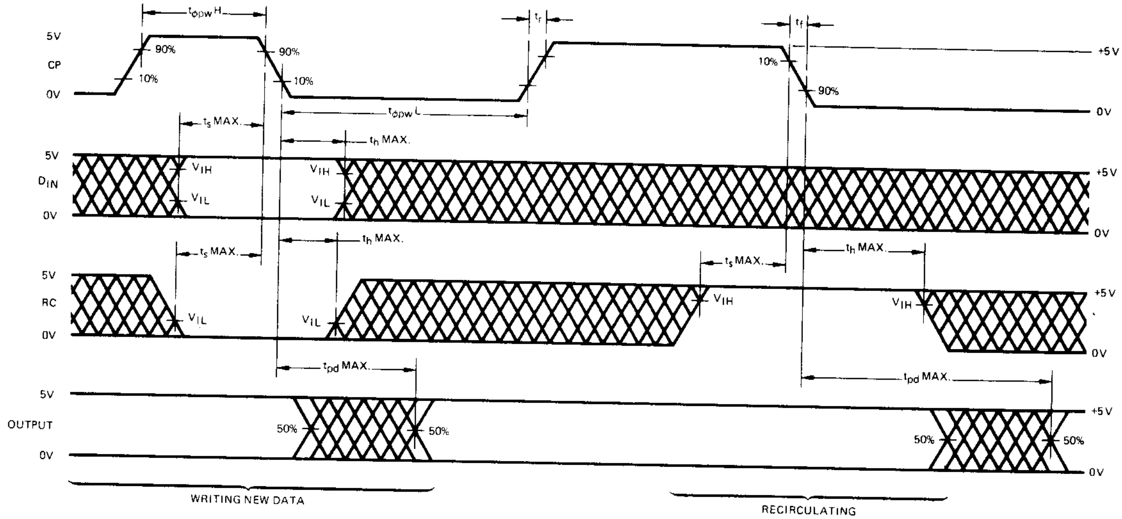
Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12V, 25°C ambient.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Am4055/6/7 Min.	Am4055/6/7 Typ.	Am4055/6/7 Max.	Am5055/6/7 Min.	Am5055/6/7 Typ.	Am5055/6/7 Max.	Units
f	Clock Frequency		0		1.0	0		1.5	MHz
$t_{\phi pw}H$	Clock HIGH Time		0.4		1.0	0.23		100	μs
$t_{\phi pw}L$	Clock LOW Time		0.4		∞	0.3		∞	μs
t_r, t_f	Clock Rise and Fall Times				200			200	ns
t_s	Set-up Time, D or RC Inputs (see definitions)	$t_r = t_f \leq$ 10ns	260			110			ns
t_h	Hold Time, D or RC Inputs (see definitions)	$t_r = t_f \leq$ 10ns	120			40			ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 4k, C_L = 10pF		350	700		250	345	ns
C_{in}	Capacitance, Data and RC Inputs (Note 2)	f = 1MHz, $V_{IN} = V_{SS}$		4	7		4	7	pF
C_ϕ	Capacitance, Clock Input (Note 2)	f = 1MHz, $V_{IN} = V_{SS}$			14			14	pF

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, t_{pd} min. is always much greater than t_h(D) max.

TIMING DIAGRAM



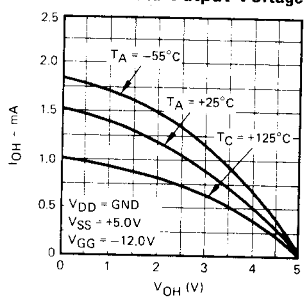
MOS-453

KEY TO TIMING DIAGRAM

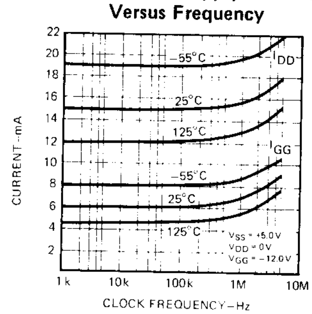
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE. ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

PERFORMANCE CURVES

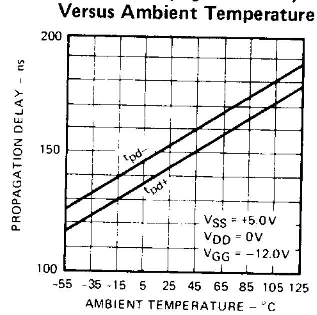
Typical Data Output HIGH Current Versus Data Output Voltage



Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature



MOS-454

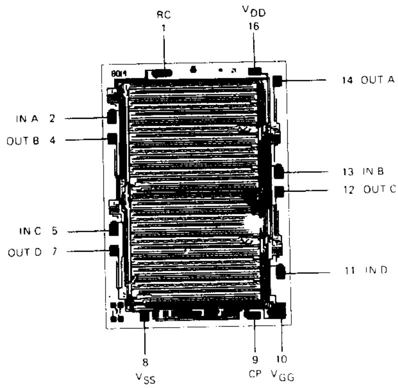
DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

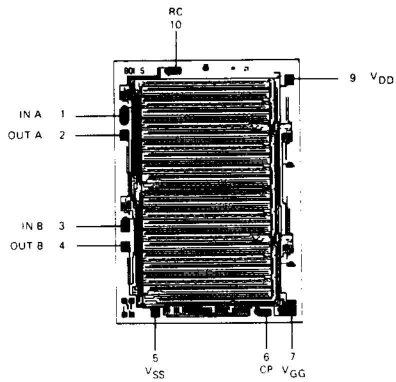
SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

Metallization and Pad Layouts

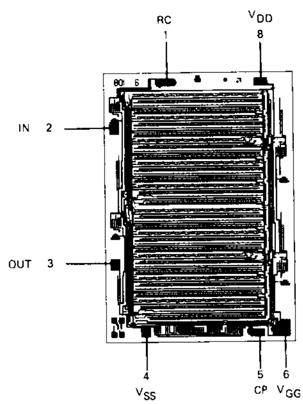
Am4055/5055



Am4056/5056



Am4047/5057



DIE SIZES 0.101" X 0.140"