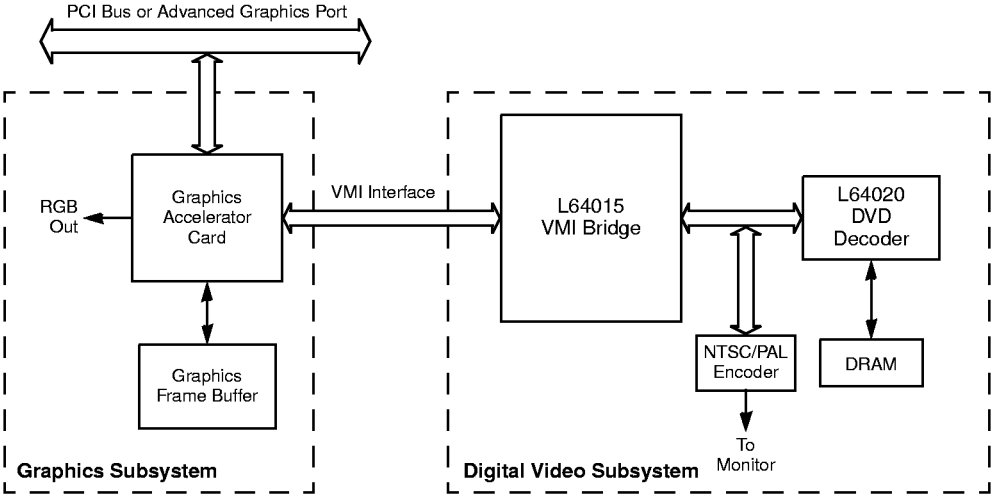
L64015 VMI Bridge

Advance Datasheet

The L64015 VMI Bridge chip is a companion chip of LSI Logic's L64020 Digital Video Decoder (DVD). The L64015 serves as an interface between a notebook computer with a VMI (Video Module Interface) ready graphics device and the decompressed video and audio bitstream output from a DVD Decoder. The video output can be viewed on either an RGB PC monitor or an NTSC/PAL TV. Decompressed audio is fed through the optional VMI audio port as I^2S formatted stereo. The host interface utilizes the VMI interface. The L64015 acts as an interface for VMI host control of the DVD Decoder.

Figure 1 shows the L64015 in a typical system.

Figure 1 Typical System Block Diagram



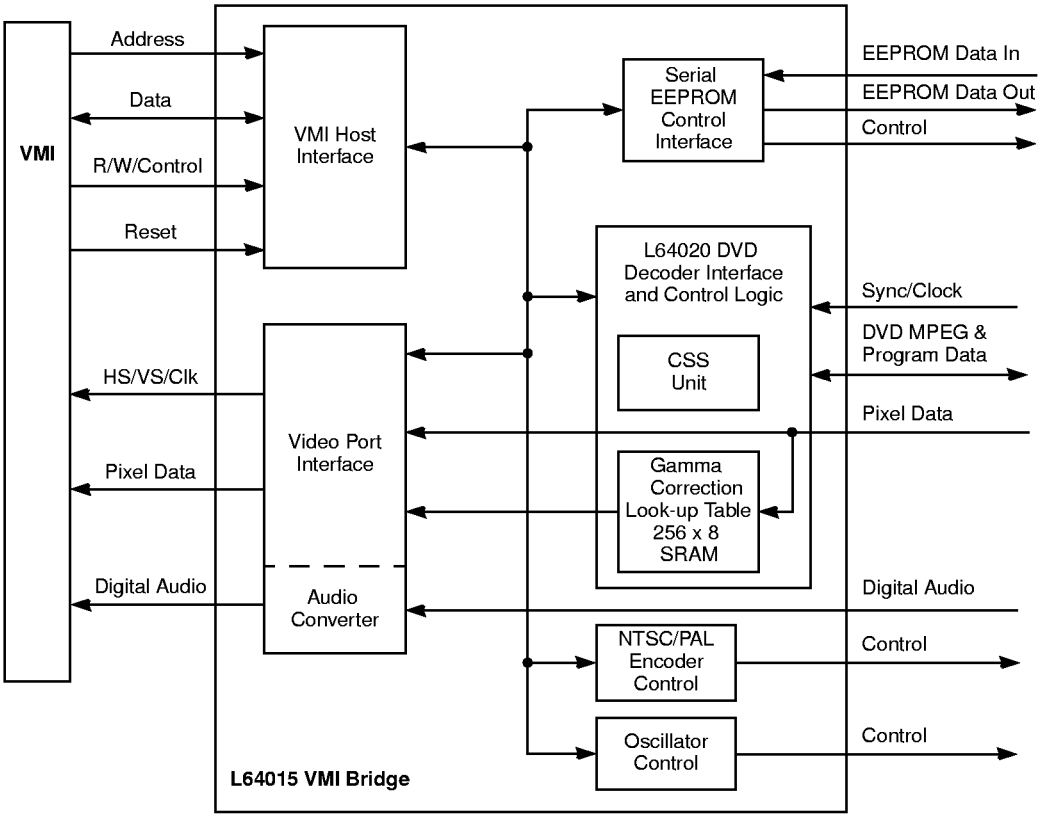
Features and Benefits

- Built-in Content Scrambling System (CSS) circuitry
- Programmable Built-in Video Color Control
- Compliance with VMI bus interface standard
- Analog stereo I^2S support for optional VMI interface features
- 0.5-µm LCA500K technology with 3.3 V operation
- Provides seamless video data transfer between graphics subsystem and digital video solution
- Supports DVD playback of CSS and non-CSS datastreams
- Supports various displays with gamma correction of CRTs
- 144-pin Plastic Quad Flat Pack (PQFP) package
- Supports Industry standard audio interface
- Provides high-performance and low-power consumption
- Available in cost-effective package

Functional Description

The L64015 provides complete control of the L64020 DVD decoder from a VMI port. Figure 2 shows a block diagram of the L64015. Short descriptions of the functional blocks follow the figure. Refer to the *L64015 VMI Bridge Technical Manual* for detailed information.

Figure 2 L64015 Functional Block Diagram



VMI Host Interface

Through this interface, the VMI host can access the L64015 direct and indexed registers, the L64020 DVD Decoder registers, and the Serial EEPROM. The L64015 registers control system capabilities such as DMA, interrupts, reset, wait, and port enabling.

L64020 DVD Decoder Interface and Control Logic

The DVD Decoder Interface and Control Logic provides access to the DVD Decoder's indexed registers and data ports. The interface and control functions handle register addressing, port enabling, reset, wait, and interrupt control. The control logic generates the required HREF and VREF signals for the DVD Decoder. The interrupt control logic receives interrupt requests from the DVD Decoder and relays them to the Host.

Gamma Correction Look-up Table

The 256 x 8 SRAM contains gamma correction information, which is arranged as a look-up table. When gamma correction look-up is enabled, the incoming 8-bit pixel data from the DVD Decoder is used as the address for the correct SRAM location. Each 8-bit SRAM location contains gamma corrected video luminance information. The L64015 accesses the information in the look-up table, and sends this information to the Host in place of the luminance video data that originated from the L64020.

Serial EEPROM Control Interface

The L64015 uses the I^2C two-wire interface to read four bytes of data from a Serial EEPROM. The EEPROM contains CIS data. The host can read or write the data serially and read data in parallel bytes through the L64015.

Video Port Interface

The L64015 video logic outputs a horizontal sync, vertical sync, and a pixel clock. The pixel data output is in eight-bit format and is compliant with the YUV byte ordering specification.

The audio logic also converts digital audio from the DVD Decoder into I^2S data in stereo format. The L64020 DVD Decoder supplies audio data that is delta-sigma modulated with a wide selection of oversampling rates.

NTSC/PAL Encoder Control

An optional, external NTSC/PAL encoder converts CCIR-601 pixel data to composite video and SVideo for viewing on television. The pixel data originates from the DVD Decoder.

Content Scrambling System (CSS) Unit

The CSS Unit provides authentication and descrambling functions. The CSS Unit can be bypassed for nonscrambled streams.

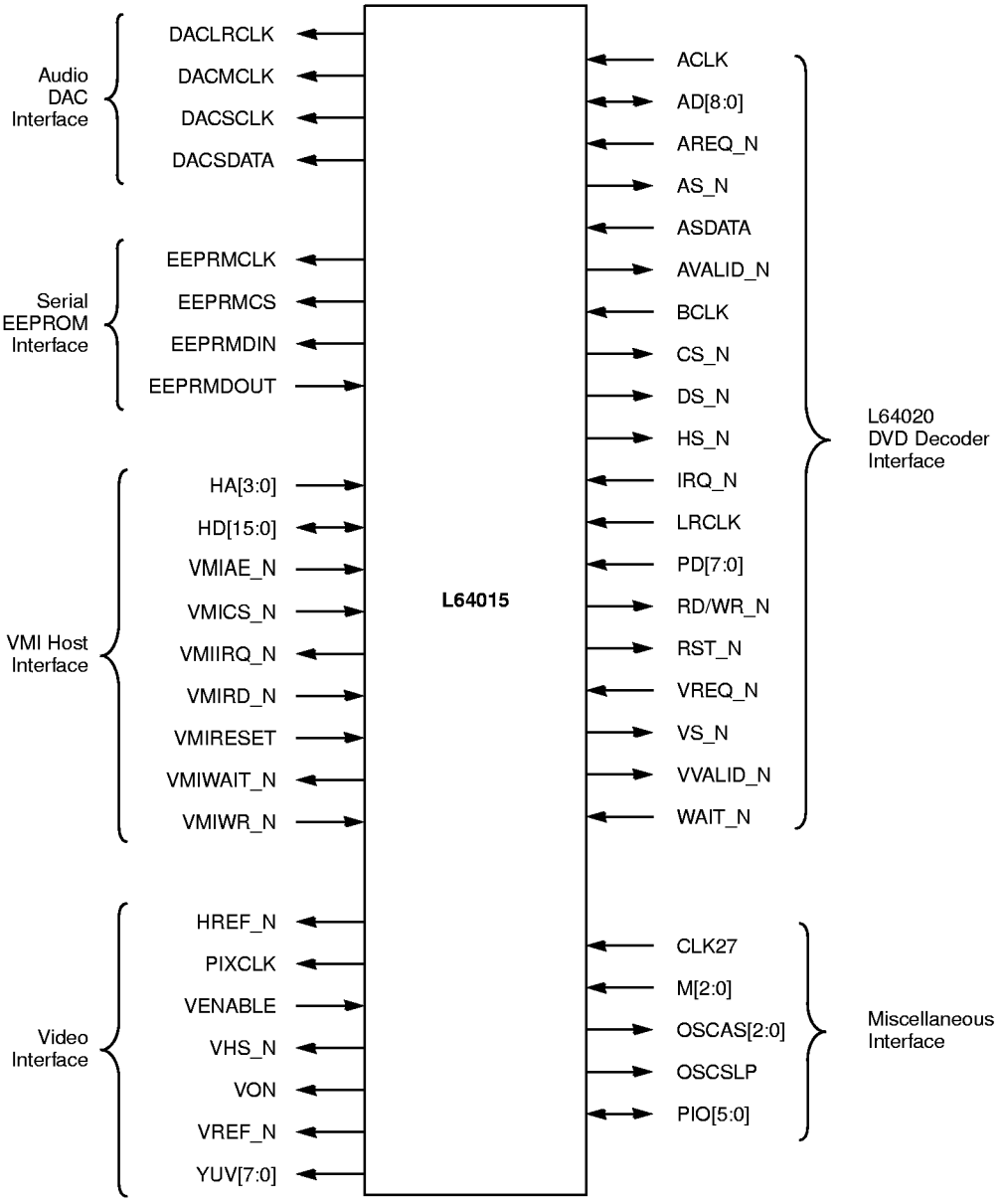
Local Registers and Decoder

The local registers reside in the L64015 and provide control over a variety of hardware functions.

Signal Descriptions

This chapter describes the external signals of the L64015. The descriptions are categorized according to the interface. Active-LOW signals have "_N" appended to the end of their names.

Figure 3 L64015 Logic Symbol



Audio DAC Interface

DACLRCLK **Audio DAC Left/Right Clock** **Output**
This output enables the left or right serial data output.

DACLRCLK	Description
0	Left Channel Enabled
1	Right Channel Enabled

DACMCLK **Audio DAC Master Clock** **Output**
DACMCLK is the digital audio master clock. Its frequency is programmable.

DACSCLK **Audio DAC Serial Clock** **Output**
DACSCLK is the serial audio digital PCM clock. Its frequency is programmable.

DACSDATA **Audio DAC Serial Data** **Output**
This signal is the digital PCM signal that carries audio information. DACSDATA uses the I^2S format.

Serial EEPROM Interface

EEPRMCLK **EEPROM Clock** **Output**
EEPRMCLK is the clock signal to the external EEPROM.

EEPRMCS **EEPROM Chip Select** **Output**
EEPRMCS enables the external EEPROM for read or write operations.

EEPRMDIN **Data to EEPROM** **Output**
EEPRMDIN is the serial data output to the external EEPROM.

EEPRMDOUT **Data from EEPROM** **Input**
EEPRMDOUT is the serial data input from the external EEPROM.

VMI Host Interface

HA[3:0] **Host Address [3:0]** **Input**
This four-bit address provides the host with access to the L64015's internal registers.

HD[15:0] **Host Data [15:0]** **Input/Output**
HD[15:0] is the 16-bit bidirectional data bus. HD15 is the most-significant bit.

VMIAE_N **VMI Address Enable** **Input**
The host asserts this input LOW to inform the L64015 that the address on HA[3:0] is valid for a host read or write of the L64015.

VMICS_N **VMI Device Chip Select** **Input**
The host asserts this input LOW when accessing the L64015.

VMIIRQ_N **VMI Interrupt Request** **Output**
The L64015 asserts this signal LOW to inform the VMI host that the VMI card needs service.

VMIRD_N **VMI I/O Read** **Input**
The VMI host asserts this signal LOW to read data from the VMI card's I/O registers. VMICS_N or VMIAE_N must be asserted at the same time.

VMIRESET **VMI Reset** **Input**
Asserting this signal HIGH clears all L64015 registers and returns the L64015 to its original unconfigured state that existed prior to initialization.

VMIWAIT_N **VMI Wait** **Output**
The L64015 asserts this signal LOW to delay completion of a memory or I/O access cycle currently in progress.

VMIWR_N **VMI I/O Write** **Input**
The VMI host asserts this signal LOW to write data to the VMI card's I/O registers. VMICS_N or VMIAE_N must be asserted at the same time.

L64020 DVD Decoder Interface

ACLK **Decoder Audio Master Clock** **Input**
ACLK is an audio output clock from the DVD Decoder.

AD[8:0] **Decoder Address/Data [8:0]** **Input/Output**
AD[8:0] functions as a nine-bit address bus, an eight-bit host data bus, or an eight-bit channel data bus.

AREQ_N **Decoder Audio Request** **Input**
The L64020 asserts AREQ_N when it is ready to receive a new byte of coded audio data in A/V PES stream mode (from a transport stream demultiplexer) or a new byte of any data in a program stream mode. The decoder is ready when the channel input FIFO is not full.

AS_N **Decoder Address Strobe** **Output**
When L64015 asserts this signal, the DVD Decoder latches the address.

ASDATA **Decoder Audio Serial Data** **Input**
ASDATA receives serial, digital audio data from the L64020's audio decoder.

AVALID_N **Decoder Audio Valid** **Output**
When the L64015 puts a valid data byte on the CH_DATA bus, it asserts this signal in response to assertion of the AREQ_N signal from the DVD Decoder. The DVD Decoder reads the byte when the L64015 deasserts AVALID_N.

BCLK **Decoder Audio Bit Serial Clock** **Input**
The L64015 uses this input to clock in the serial audio data from the DVD Decoder.

CS_N **Decoder Chip Select** **Output**
The L64015 asserts this signal LOW to access the L64020 DVD Decoder for either a read or a write operation. CS_N must be asserted LOW the entire read/write cycle.

DS_N **Decoder Data Strobe** **Output**
The L64015 asserts this signal LOW to strobe data in or out of the L64020 DVD Decoder.

HS_N **Decoder Horizontal Sync** **Output**
HS_N is the horizontal sync signal to the DVD Decoder and NTSC/PAL Encoder. HS_N is synchronous to CLK27.

IRQ_N **Decoder Interrupt Request** **Input**
The L64020 asserts this signal LOW to tell the L64015 that an unmasked interrupt condition has occurred in the DVD Decoder.

LRCLK **Decoder Audio Left/Right Clock** **Input**
Using the default setting, LRCLK is driven HIGH when the ASDATA pin has a right channel sample, and LRCLK is driven LOW when the ASDATA pin has a left channel sample.

PD[7:0] **Decoder Pixel Data [7:0]** **Input**
The PD[7:0] bus carries the pixel data for the reconstructed pictures. The pixel data is formatted in ITU_R BT.601 YCbCr chromaticity.

RD/WR_N **Decoder Read/Write** **Output**
The L64015 drives this signal HIGH for a read cycle or drives it LOW for a write cycle. The L64015 also asserts the chip select signal (CS_N) during a write or read cycle.

RST_N **Decoder Reset** **Output**
When the L64015 asserts RST_N, the L64020 resets its internal microcontroller, FIFO controllers, state machines, and registers. The minimum reset pulse width is 8 CLK27 cycles (SYSCLK). Both CLK27 and ACLK must be running during reset.

VREQ_N **Decoder Video Request** **Input**
The DVD Decoder asserts VREQ_N when it is ready to receive a new byte of coded audio data in A/V PES stream mode. The decoder is ready when the channel FIFO is not near full. VREQ_N is not used in program stream modes.

VS_N **Decoder Vertical Sync** **Output**
VS_N is the vertical sync signal to both the DVD Decoder and the NTSC/PAL Encoder.

VVALID_N **Decoder Valid Video** **Output**
The L64015 asserts this signal in response to VREQ_N if there is a valid data byte on the AD[8:0] bus. The L64020 inputs the byte when it deasserts VREQ_N.

WAIT_N **Decoder Wait** **Input**
The L64020 asserts WAIT_N to indicate that its Host Interface is busy with a read or write bus cycle and deasserts it when the current cycle is completed. WAIT_N is 3-stated when CS_N is not active.

Video Interface

HREF_N **Video Horizontal Reference** **Output**
This signal provides the horizontal sync signal to the Video Port.

PIXCLK **Video Pixel Clock** **Output**
The operating frequency for this clock is selectable at either 13.5 MHz or 27 MHz.

VENABLE **Video Enable** **Input**
When HIGH, this signal enables outputs to the Video Port.

VHS_N **Video Horizontal Sync** **Output**
VHS_N is the Video horizontal sync.

VON **Video On** **Output**
The L64015 drives this signal HIGH when the video outputs are active. VON is LOW when the Video Port outputs are high impedance.

VREF_N **Video Vertical Reference** **Output**
VREF_N provides the vertical sync signal to the Video Port.

YUV[7:0] **Video Luma/Chroma [7:0]** **Output**
This eight-bit output bus contains color luminance and chrominance data.

Miscellaneous Interface

CLK27 **27-MHz Clock** **Input**
This clock is the 27-MHz system clock from an external oscillator.

M[2:0] **Mode Select [2:0]** **Input**
The mode select signals enable either normal operation or one of the test modes as shown below:

M2	M1	M0	Function
0	0	1	Normal VMI operation
1	1	0	3-state output test
1	1	1	Scan flip-flop test

OSCAS[2:0] **Audio Oscillator Frequency Set [2:0]** **Output**
These signals are output to the oscillator and indicate the audio master clock frequency.

OSCAS2	OSCAS1	OSCAS0	Selected Audio Clock (MHz)
0	0	0	12.288
0	0	1	11.2896
0	1	0	8.192
0	1	1	24.576
1	0	0	8.192
1	0	1	16.9344
1	1	0	18.432
1	1	1	11.2896

OSCSLP **Oscillator Sleep** **Output**
When the L64015 asserts this signal, it forces the external oscillator into sleep mode.

PIO[5:0] **Programmable I/O** **Input/Output**
These user-defined signals are available for control or status functions.

Electrical Requirements

This section specifies the electrical requirements for the L64015. Four tables list electrical data in the following categories:

- Absolute Maximum Ratings (Table 1)
- Recommended Operating Conditions (Table 2)
- Capacitance (Table 3)
- DC Characteristics (Table 4)

Table 1 Absolute Maximum Ratings

Symbol	Parameter	Limits[1]	Unit
V_{DD}	DC Supply	−0.3 to +3.9	V
V_{IN}	5 V Compatible Input Voltage	−1.0 to 6.5	V
I_{IN}	DC Input Current	±10	µA
T_{STG}	Storage Temperature Range, Plastic	−40 to +125	°C

1. Referenced to V_{SS}.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
V_{DD}	DC Supply, Commercial	+3.14 to +3.45	V
T_A	Operating Ambient Temperature	0 to +70	°C
T_J	Junction Temperature	≤150	°C

Table 3 Capacitance

Symbol	Parameter[1]	Min	Typ	Max	Unit
C_{IN}	Input Capacitance (5 V compatible)	–	3.0	–	pF
C_{OUT}	Output Capacitance	–	3.0	–	pF
C_{IO}	I/O Bus Capacitance	–	3.0	–	pF

1. Measurement conditions are V_{IN} = 3.3 V, T_A = 25 °C, and clock frequency = 1 MHz.

Table 4 DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{DD}	Supply Voltage	–	3.14	3.3	3.45	V
V_{IL}	Voltage Input Low	–	V_{SS} – 0.5	–	0.8	V
V_{IH}	Voltage Input High	5 V compatible	2.0	–	5.5	V
V_T	Switching Threshold	–	–	1.4	2.0	V
V_{OH}	Voltage Output High	I_{OH} = –4.0 mA I_{OH} = –6.0 mA (PIO)	2.4	–	V_{DD}	V
V_{OL}	Voltage Output Low	I_{OL} = 4.0 mA I_{OL} = 6.0 mA (PIO)	–	0.2	0.4	V
I_{IN}	Input Current	V_{IN} = V_{DD} or V_{SS}	–10	±1	10	µA
I_{OZ}	Current 3-State Output Leakage	V_{OUT} = V_{SS} or V_{DD}	–10	±1	10	µA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}	TBD	TBD	TBD	µA
I_{CC}	Dynamic Supply Current	V_{DD} = Max, f = 27 MHz	–	TBD	–	mA

1. Junction temperature range: 0 to 115 °C, ± 5% power supply.

Pinout, Package, and Ordering Information

The L64015 is available in a 144-pin PQFP package. Table 5 provides ordering information for the L64015. Table 6 provides an alphabetical pin list for the 144-pin PQFP package.

Table 5 L64015 Ordering Information

Part Number	Order Number	Clock Frequency	Package Type	Operating Range
L64015	TBD	27 MHz	144-pin PQFP	Commercial

Table 6 Alphabetical Pin List for the 144-pin PQFP Package

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ACLK	126	HD0	59	NC	92	VDD	20
AD0	9	HD1	67	NC	93	VDD	36
AD1	10	HD2	61	NC	94	VDD	37
AD2	11	HD3	62	NC	122	VDD	45
AD3	12	HD4	65	OSCAS0	119	VDD	58
AD4	13	HD5	66	OSCAS1	117	VDD	63
AD5	15	HD6	68	OSCAS2	120	VDD	72
AD6	16	HD7	69	OSCSLP	103	VDD	74
AD7	17	HD8	39	PD0	139	VDD	91
AD8	19	HD9	34	PD1	138	VDD	96
ADATA	123	HD10	33	PD2	135	VDD	108
AREQ_N	21	HD11	32	PD3	134	VDD	109
AS_N	4	HD12	31	PD4	132	VDD	118
AVALID_N	25	HD13	30	PD5	131	VDD	128
BCLK	125	HD14	29	PD6	130	VDD	136
CLK27	121	HD15	28	PD7	129	VDD	144
CS_N	3	HREF_N	83	PIO0	114	VENABLE	27
DACLRCLK	112	HS_N	141	PIO1	115	VHS_N	75
DACMCLK	113	IRQ_N	140	PIO2	116	VMIAE_N	55
DACSCLK	111	LRCLK	124	PIO3	133	VMICS_N	49
DACSDATA	106	M0	76	PIO4	137	VMIIRQ_N	51
DS_N	6	M1	79	PIO5	85	VMIRD_N	52
EEPRMCLK	64	M2	82	PIXCLK	80	VMIRESET_N	57
EEPRMCS	60	NC[2]	44	RD/WR_N	7	VMIWAIT_N	56
EEPRMDIN	77	NC	48	Reserved[1]	46	VMIWR_N	53
EEPRMDOUT	78	NC	84	Reserved	47	VON	26
HA0	43	NC	86	Reserved	50	VREF_N	81
HA1	42	NC	88	RST_N	8	VREQ_N	23
HA2	41	NC	89	VDD	1	VS_N	142
HA3	40	NC	90	VDD	18	VSS	2

(Sheet 1 of 2)

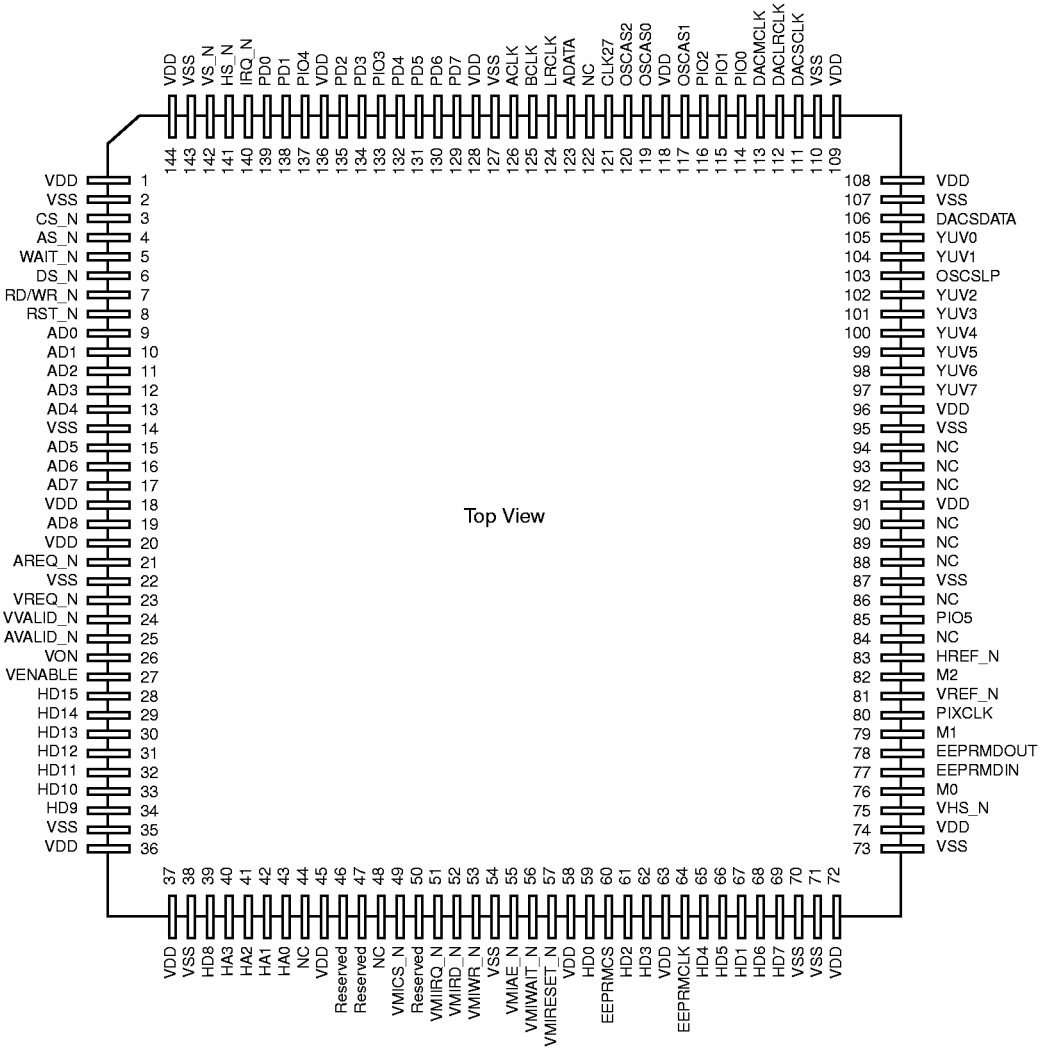
Table 6 Alphabetical Pin List for the 144-pin PQFP Package (Cont.)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
VSS	14	VSS	71	VSS	127	YUV2	102
VSS	22	VSS	73	VSS	143	YUV3	101
VSS	35	VSS	87	VVALID_N	24	YUV4	100
VSS	38	VSS	95	WAIT_N	5	YUV5	99
VSS	54	VSS	107	YUV0	105	YUV6	98
VSS	70	VSS	110	YUV1	104	YUV7	97

(Sheet 2 of 2)

1. Reserved pins should be tied HIGH for normal operation.
2. NC pins are not connected.

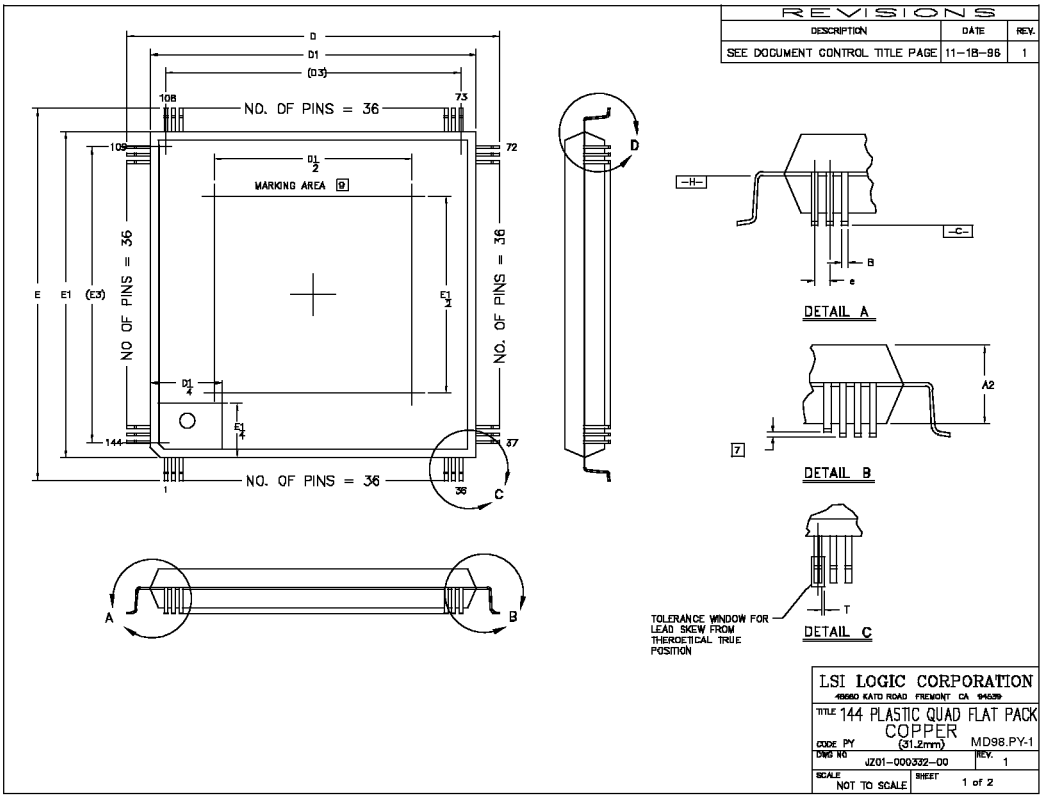
Figure 4 L64015 Pinout



Notes:

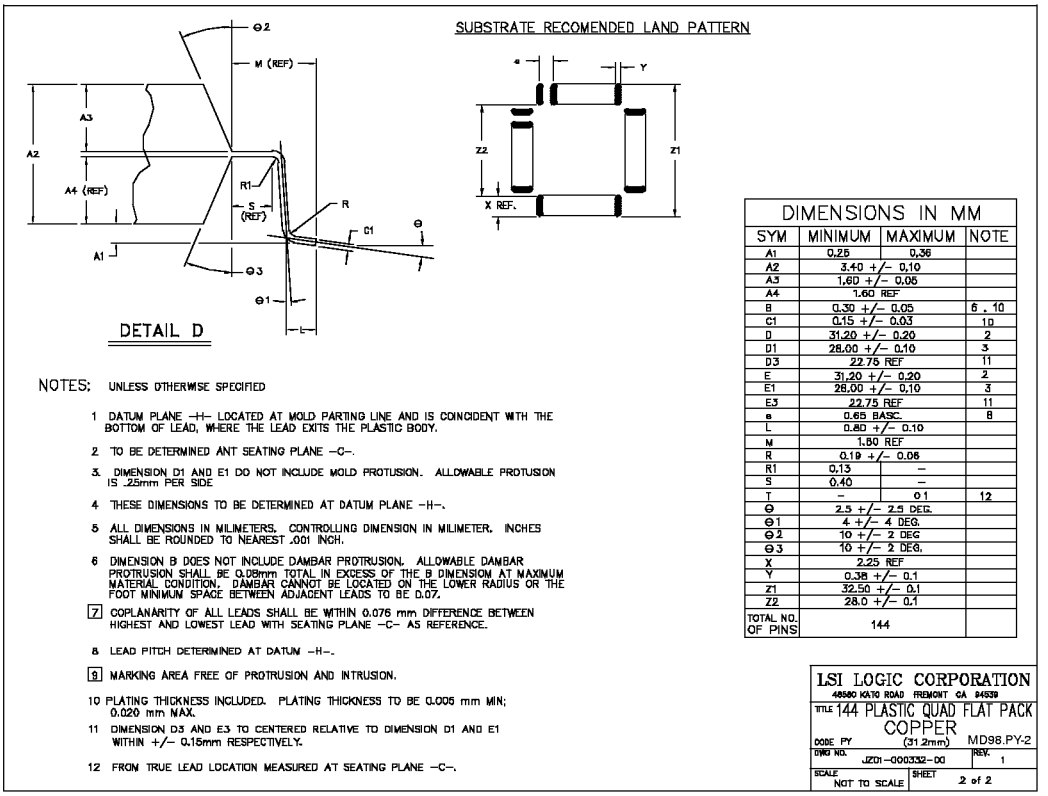
- *NC* pins are not connected.
- *Reserved* pins should be tied HIGH for normal operation.

Figure 5 144-pin PQFP (PY) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code PY.**

Figure 5 144-pin PQFP (PY) Mechanical Drawing (Cont.)



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code PY.**