# 3A DUAL OPEN-DRAIN MOSFET DRIVERS

## FEATURES

- **Independently-Programmable Rise and Fall Times**
- **Low Output Impedance ..... 3.5Ω Typ**
- **High Speed $t_R$, $t_F$ .... <30 ns with 1800 pF Load Typ**
- **Short Delay Times ..... 35 ns Typ**
- **Wide Operating Range ..... 4.5V to 18V**

## APPLICATIONS

- **Motor Controls**
- **Driving Bipolar Transistors**
- **Driver for Nonoverlapping Totem Poles**
- **Reach-Up/Reach-Down Driver**

## RUGGED

- **Tough CMOS™ Construction**
- **Latch-Up Protected: Will Withstand >500 mA Reverse Current (Either Polarity)**
- **Input Withstands Negative Swings Up to –5V**

## ORDERING INFORMATION

| Part No. | Package | Temperature Range |
|---|---|---|
| TC4406CPA | 8-Pin PDIP | 0°C to +70°C |
| TC4406EPA | 8-Pin PDIP | – 40°C to + 85°C |
| TC4406EOE | 16-Pin SO Wide | – 40°C to + 85°C |
| TC4406MJA | 8-Pin CerDIP | – 55°C to +125°C |
| TC4406COE | 16-Pin SO Wide | 0°C to +70°C |
| TC4407CPA | 8-Pin PDIP | 0°C to +70°C |
| TC4407EPA | 8-Pin PDIP | – 40°C to + 85°C |
| TC4407EOE | 16-Pin SO Wide | – 40°C to + 85°C |
| TC4407MJA | 8-Pin CerDIP | – 55°C to +125°C |
| TC4407COE | 16-Pin SO Wide | 0°C to +70°C |

## GENERAL DESCRIPTION

The TC4406 and TC4407 are CMOS buffer-drivers constructed with complementary MOS outputs, where the drains of the totem-pole output have been left separated so that individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of drain current-limiting resistors in the pull-up and/or pull-down sections, allowing the user to define the rates of rise and fall for a capacitive load; or a reduced output swing, if driving a resistive load, or to limit base current, when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 ns for a 1800-pF load. There is no upper limit.

For driving MOSFETs in motor-control applications, where slow-ON/fast-OFF operation is desired, these devices are superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because they allow accurate control of turn-ON, while maintaining fast turn-OFF and maximum noise immunity for the device being driven.

When used to drive bipolar transistors, these drivers maintain the high speeds common to other TelCom drivers. They allow insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-OFF. By proper positioning of the resistor, either npn or pnp transistors can be driven.

For driving many loads in low-power regimes, these drivers, because they have very low quiescent current (<250 µA) and minimize shoot-through currents in the output stage, require significantly less power than similar drivers, and can be helpful in meeting low-power budgets.

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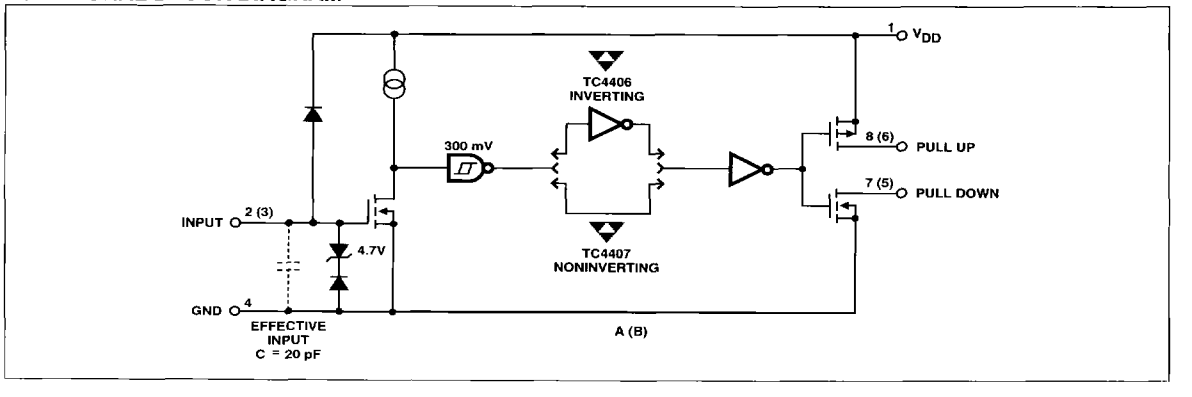
## FUNCTIONAL BLOCK DIAGRAM



Because neither drain in an output is dependent on the other (though they do switch simultaneously), these devices can also be used as open-drain buffer/drivers where both drains are available in one device, thus minimizing chip count. Unused open drains should be returned to the supply rail that their device sources are connected to (pull-downs to ground, pull-ups to $V_{DD}$), to prevent static damage. Alternatively, in situations where timing resistors or other means of limiting crossover currents are used, like drains may be paralleled for greater current-carrying capacity.

The TC4406 and TC4407 are built using TelCom Semiconductor' new Tough CMOS process and are capable of giving reliable service in the most demanding electrical environments: they will not latch up under any conditions within their power and voltage ratings; they are not subject to damage when up to 5V of noise spiking of either polarity occurs on their ground pin; and they can accept, without damage or logic upset, up to 1/2 amp of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +22V
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 55°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 45°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS:

unless otherwise specified, specifications measured at $T_A$ = +25°C with 4.5V ≤ $V_{DD}$ ≤ 18V.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| $V_{IH}$ | Logic 1 High Input Voltage | | 2.4 | — | — | V |
| $V_{IL}$ | Logic 0 Low Input Voltage | | — | — | 0.8 | V |
| $I_{IN}$ | Input Current | – 5V ≤ $V_{IN}$ ≤ $V_{DD}$ | – 1 | — | 1 | µA |
| **Output** | | | | | | |
| $V_{OH}$ | High Output Voltage | | $V_{DD}$ – 0.025 | — | — | V |
| $V_{OL}$ | Low Output Voltage | | — | — | 0.025 | V |
| $R_O$ | Output Resistance, Pull Up | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V | — | 2.8 | 5 | Ω |
| $R_O$ | Output Resistance, Pull Down | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V | — | 3.5 | 5 | Ω |
| $I_{PK}$ | Peak Output Current (Any Drain) | Duty cycle <2%, t ≤ 300µsec | — | 3 | — | A |
| $I_{DC}$ | Continuous Output Current (Any Drain) | | — | — | 150 | mA |
| $I_R$ | Latch-Up Protection (Any Drain) Withstand Reverse Current | Duty cycle <2%, t ≤ 300µsec | > 500 | — | — | mA |
| **Switching Time (Note 1)** | | | | | | |
| $t_R$ | Rise Time | Figure 1, $C_L$ = 1800 pF | — | 23 | 35 | ns |
| $t_F$ | Fall Time | Figure 1, $C_L$ = 1800 pF | — | 25 | 35 | ns |
| $t_{D1}$ | Delay Time | Figure 1, $C_L$ = 1800 pF | — | 33 | 75 | ns |
| $t_{D2}$ | Delay Time | Figure 1, $C_L$ = 1800 pF | — | 38 | 75 | ns |
| **Power Supply** | | | | | | |
| $I_S$ | Power Supply Current | $V_{IN}$ = 3V (Both Inputs) | — | 1.5 | 2.5 | mA |
| | | $V_{IN}$ = 0V (Both Inputs) | — | 0.15 | 0.25 | mA |

## ELECTRICAL CHARACTERISTICS:

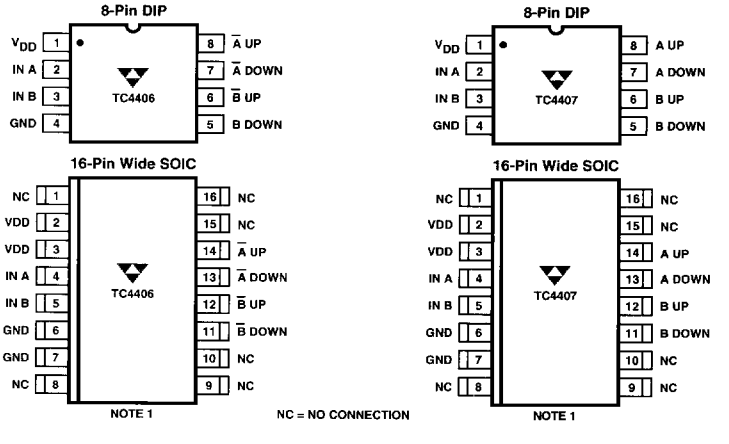
Specifications measured over operating temperature range with $4.5V \le V_{DD} \le 18V$, unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| $V_{IH}$ | Logic 1 High Input Voltage | | 2.4 | — | — | V |
| $V_{IL}$ | Logic 0 Low Input Voltage | | — | — | 0.8 | V |
| $I_{IN}$ | Input Current | $-5V \le V_{IN} \le V_{DD}$ | – 10 | — | 10 | µA |
| **Output** | | | | | | |
| $V_{OH}$ | High Output Voltage | | $V_{DD}$ – 0.025 | — | — | V |
| $V_{OL}$ | Low Output Voltage | | — | — | 0.025 | V |
| $R_O$ | Output Resistance, Pull Up | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V | — | 3.7 | 8 | Ω |
| $R_O$ | Output Resistance, Pull Down | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V | — | 4.3 | 8 | Ω |
| $I_{PK}$ | Peak Output Current (Any Drain) | Duty cycle <2%, t ≤ 300µsec | — | 3 | — | A |
| $I_{DC}$ | Continuous Output Current (Any Drain) | | — | — | 150 | mA |
| $I_R$ | Latch-Up Protection (Any Drain) Withstand Reverse Current | Duty cycle <2%, t ≤ 300µsec | >500 | — | — | mA |
| **Switching Time (Note 1)** | | | | | | |
| $t_R$ | Rise Time | Figure 1, $C_L$ = 1800 pF | — | — | 60 | ns |
| $t_F$ | Fall Time | Figure 1, $C_L$ = 1800 pF | — | — | 60 | ns |
| $t_{D1}$ | Delay Time | Figure 1, $C_L$ = 1800 pF | — | — | 100 | ns |
| $t_{D2}$ | Delay Time | Figure 1, $C_L$ = 1800 pF | — | — | 100 | ns |
| **Power Supply** | | | | | | |
| $I_S$ | Power Supply Current | $V_{IN}$ = 3V (Both Inputs) | — | 2 | 3.5 | mA |
| | | $V_{IN}$ = 0V (Both Inputs) | — | 0.2 | 0.3 | mA |

**NOTE** : 1. Switching times guaranteed by design.



## PIN CONFIGURATIONS



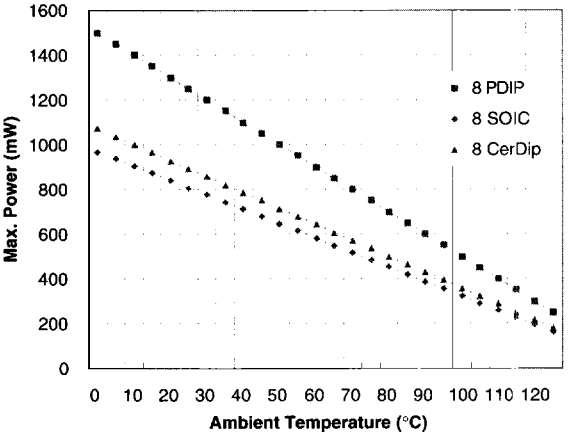

**NOTE:** 1. Duplicate pins must both be connected for proper operation.

## POWER-ON OSCILLATION

**It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.**

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement.

### Thermal Derating Curve



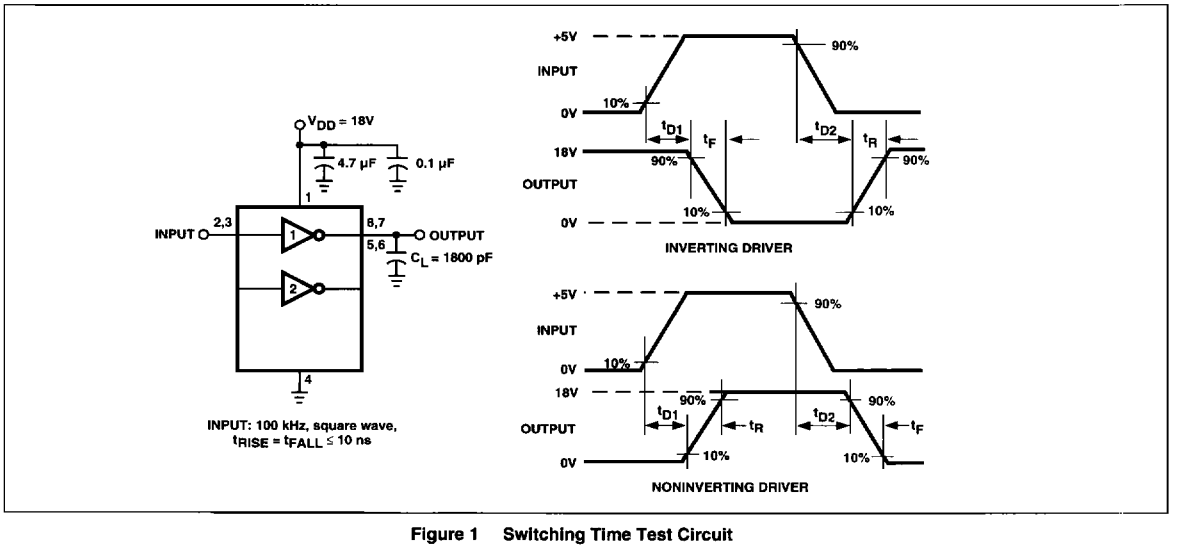
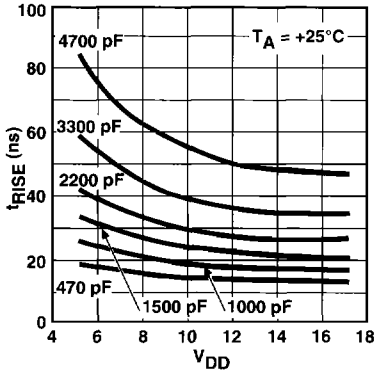



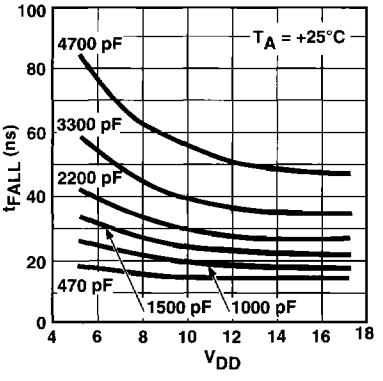

**Figure 1 Switching Time Test Circuit**

## TYPICAL CHARACTERISTICS CURVES

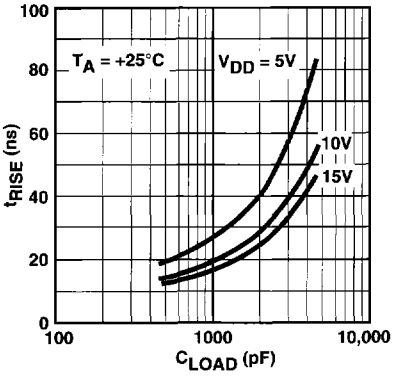
Rise Time vs. Supply Voltage



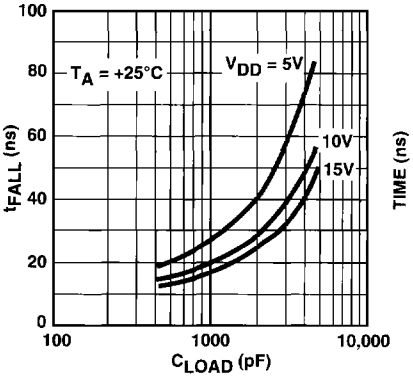

Fall Time vs. Supply Voltage



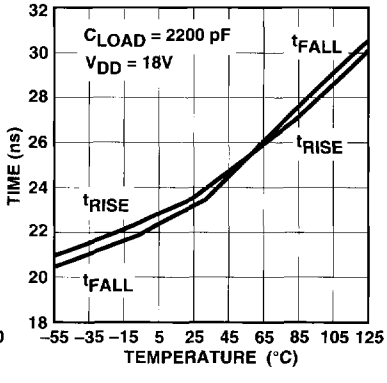

Rise Time vs. Capacitive Load



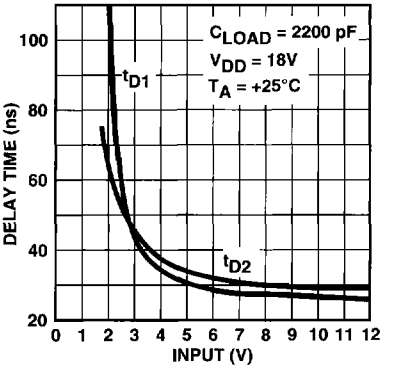

Fall Time vs. Capacitive Load



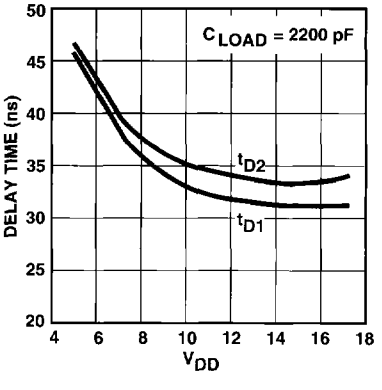

Rise and Fall Times vs. Temperature



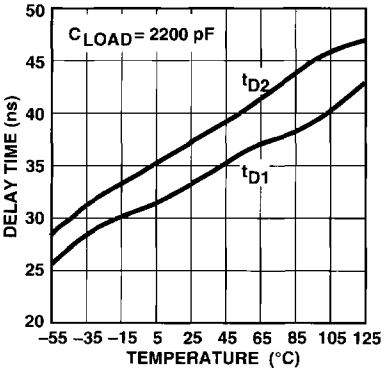

Propagation Delay vs. Input Amplitude



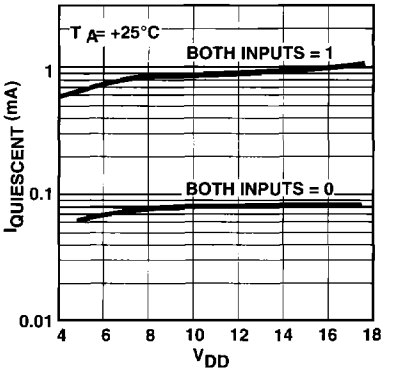

Propagation Delay Time vs. Supply Voltage




Propagation Delay Time vs. Temperature




Quiescent Supply Current vs. Voltage

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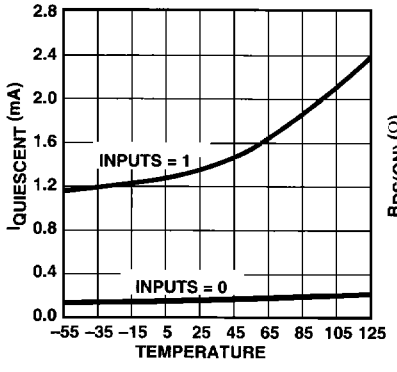
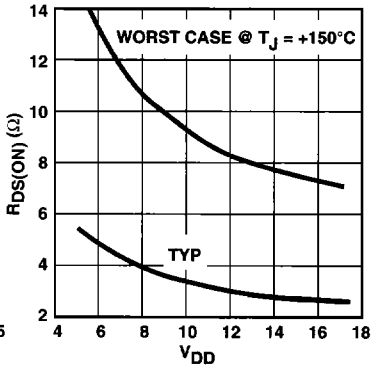
## TYPICAL CHARACTERISTICS CURVES (Cont.)

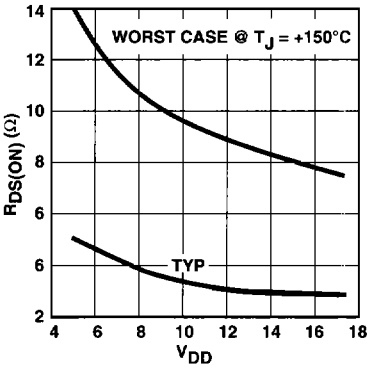
Quiescent Current vs. Temperature




Output Resistance (Pull Up) vs. Supply Voltage

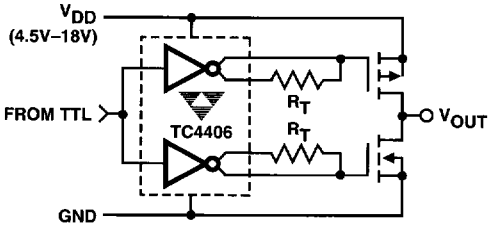



Output Resistance (Pull Down) vs. Supply Voltage

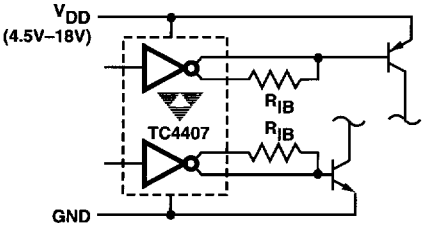



## TYPICAL APPLICATIONS

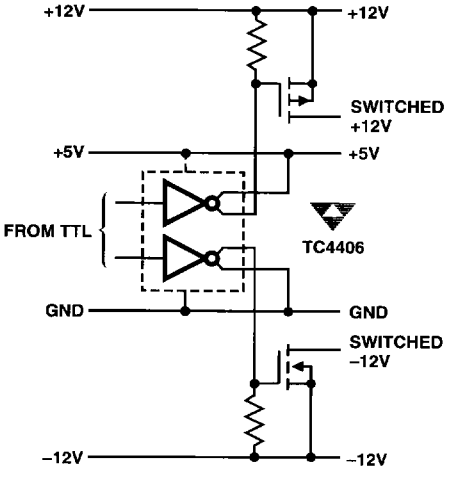
Zero Crossover-Current Totem-Pole Switch



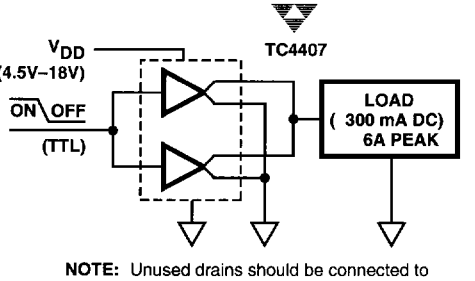

Driving Bipolar Transistors




Reach-Up and Reach-Down Driving




High-Side Switch




NOTE: Unused drains should be connected to their respective supplies.