ABRIDGED VERSION

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SSI 33P3710
PD Read Channel IC

Target Specification

February 1996

DESCRIPTION

The SSI 33P3710 device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for a PD drive system. Functional blocks include an input attenuator, pulse detector, programmable filter, timebase generator, and data synchronizer. PD data rates from 6 to 30 Mbit/s for (2,7) code can be programmed using internal DACs whose reference current are set by two external resistors (RR, RX).

Programmable functions of the SSI33P3710 are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

FEATURES

GENERAL

- Programmable PD data rate of 6 to 30 Mbit/s (2,7RLL) code. Internal DAC controlled
- Supports AGC and equalizer/filter for CD signal down to 1x speed
- Complete zoned recording application support
- Low Power operation (450 mW typical @ 5V)
- Bi-directional serial port register access
- Register programmed power management (Sleep mode < 5 mW)
- Power supply range (4.5 to 5.5V)
- Small footprint 64-lead TQFP package

PULSE DETECTOR

- Internal multiplexer for PD/CD signal inputs
- Programmable attenuator (min: -24 dB, 4-bit resolution)
- Fast attack/decay mode for rapid AGC recovery
- Low drift AGC hold circuitry
- Temperature compensated, exponential control AGC
- Wide bandwidth, precision full-wave rectifier
- Programmable LEVEL pin time constant
- Signal swing qualification circuit
- Bottom clamp and envelope type pulse qualification circuitry for pit mark recording
- Internal test decay timing
- External $\overline{\text{LOW-Z}}$ and AGC HOLD control pin

PROGRAMMABLE FILTER

- Supports two ranges of Programmable cutoff frequency : 4 to 24 MHz, 0.5 to 8 MHz
- Programmable boost/equalization of 0 to 12 dB
- Single-ended normal outputs for $\overline{\text{CD}}$ (inverted)/PD pulse qualification

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FEATURES (continued)

- Differential normal and differentiated signal outputs
- ± 20% Fc accuracy (Fc = 0.5 to 8 MHz)
- ±15% Fc accuracy (Fc = 8 to 24 MHz)
- Less than 2.0% total harmonic distortion
- No external filter components required

TIME BASE GENERATOR

- Better than 2.0% frequency resolution
- Up to 65 MHz frequency output (FOUT: Output buffer limited)
- Independent divide by M and N registers
- VCO center frequency matched to data synchronizer VCO
- FOUT output available except in power down mode

DATA SYNCHRONIZER

- Fast acquisition phase lock loop with zero phase restart technique
- Fully integrated data synchronizer
- No external delay lines, active devices, or active PLL components
- Programmable decode window symmetry control via serial port
- Window shift control ±30% (4-bit)
- Includes delayed data and VCO clock monitor pins
- Separated qualifier output (RDO) and data synchronizer input (RDI)

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