5-band stereo equalizer circuit

TEA6360

FEATURES

- Monolithic integrated 5-band stereo equalizer circuit.
- Five filters for each channel.
- Centre frequency, bandwidth and maximum boost/cut defined by external components.
- Choise for variable or constant Q-factor via I²C software.
- Defeat mode
- All stages are DC-coupled.
- I²C-bus control for all functions.
- Two different addresses programmable.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 14)	7	8.5	13.2	V
I_P	supply current	-	*	-	mA
$V_{1,32}$	input voltage range	-	2.1 to V_{P-1}	-	V
V_o	maximum output signal level (RMS value, pins 13 and 20)	- 1.1		-	V
G_v	total signal gain, all filters linear	–0.5	-	0	dB
B	-1 dB frequency response (linear)	0 to 20	-	-	kHz
T_{amb}	operating ambient temperature	–40	-	+85	°C

* Value to be fixed.

GENERAL DESCRIPTION

The 5-band stereo equalizer is an I²C-bus controlled tone processor for application in car radio sets, TV sets and music centres. It offers the possibility of sound control as well as equalization of sound pressure behaviour of different rooms or loudspeakers, especially in cars.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6360	32	shrink DIL	plastic	SOT232

5-band stereo equalizer circuit

TEA6360

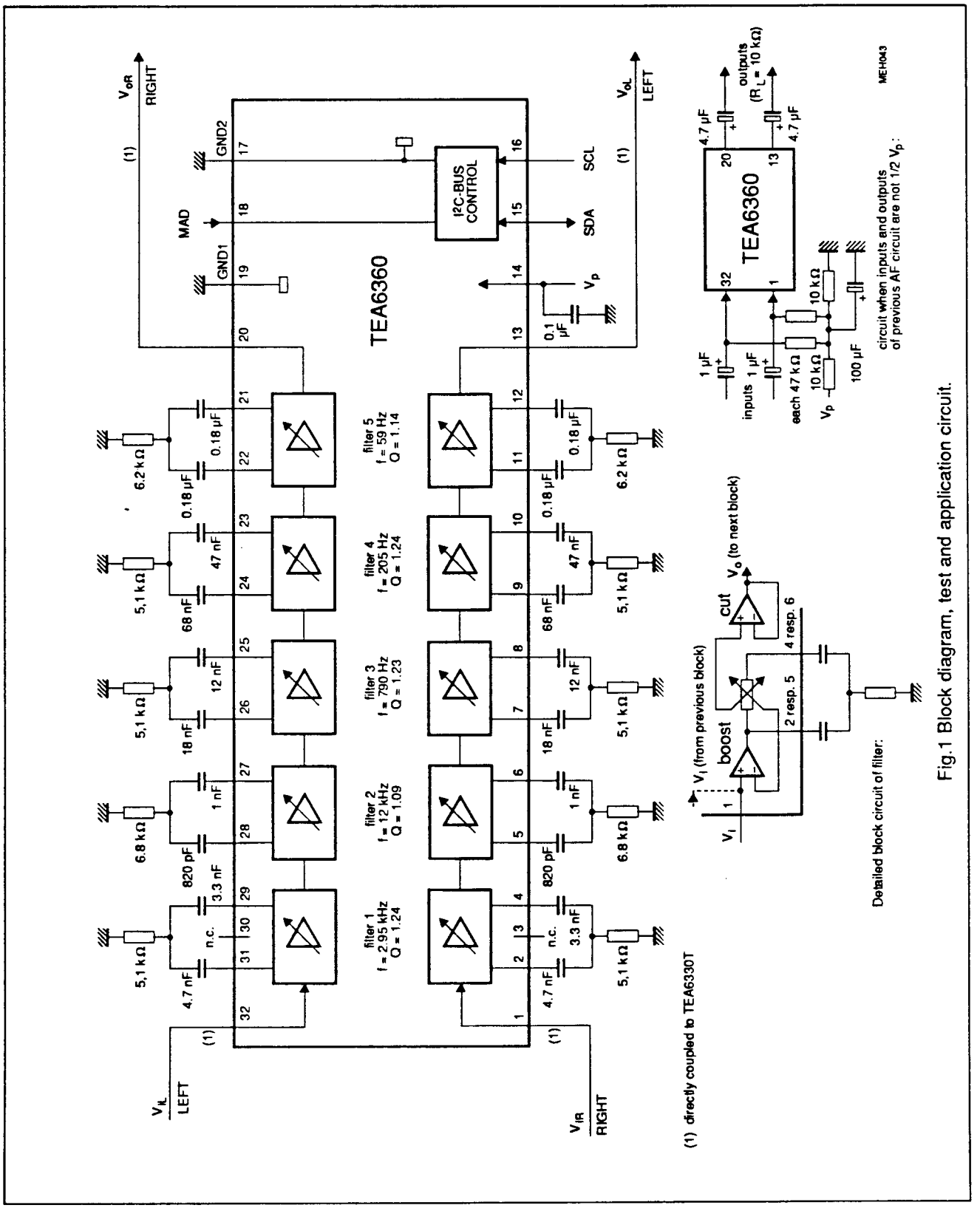


Fig.1 Block diagram, test and application circuit.

5-band stereo equalizer circuit

FUNCTIONAL DESCRIPTION

The TEA6360 is performed with ten equal filter amplifiers with its connections A and B (see Fig.1).

The central frequencies for the different filters as well as the bandwidth and the control ranges for boost and cut depent on the external components. Each filter can have different values but for one filter the centre frequency as well as the control range for boost and cut are the same. That means the curves for boost and cut are symmetrical.

The contol range (maximum value in dB) is divided into five steps and one extra step for the linear position.

For 12 dB maximum gain the typical step set is 2.4 dB. The internal resistor chain of each filter amplifier is optimized for 12 dB maximum gain. Therefore the typical gain factors for 15 dB applification are as follows:

step 1 = 2.7 dB
step 2 = 5.5 dB
step 3 = 8.4 dB
step 4 = 11.6 dB
step 5 = 15.0 dB

Control of the different filters is selected by the subaddress byte (Table 1). The position of the filter in the left channel and that in the right is always the same; the position of the boost part is independent controllable from the position of the cut part (see Tables 2 and 3).

If only boost (cut on step 0) or cut (boost on step 0) is used, the quality factor of the filter has its maximum value in the maximum position (step 5). With decreasing step number the quality factor decreases also (variable quality factor). In this mode the control pattern is according to Table 4.
A different control is necessary for getting a constant quality factor over the whole control range. For boost condition have the boost parts to be set on the position step 5; and control for the different steps is performed by the cut part and vice versa for the cut function. The pattern for this mode is given in Table 5.

The cut part has to follow the boost part in each filter for economic reasons. So the signal is first amplified and then attenuated. This has to be taken into account for the internal level diagram in case of constant quality factor. This may result in a mode between constant Q and non-constant Q mode; for example for the position +2 it is not necessary to amplifie with step +5 and then attenuate with –3 step. The combination of step +4 with step –2 for reaching position +2 is a good result (quasi constant quality factor, (see Table 6).

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Ground pins 19, 28 and 43 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 14)	0	13.2	V
V_n	voltage on all pins, grounds excluded	0	V_P	V
P_{tot}	total power dissipation	0	500	mW
T_{stg}	storage temperature range	–40	+150	°C
T_{amb}	operating ambient temperature range	–40	+85	°C
V_{ESD}	electrostatic handling* for all pins		±500	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

5-band stereo equalizer circuit

TEA6360

PINNING

SYMBOL	PIN	DESCRIPTION
V_{iL}	1	audio frequency input LEFT
F1LA	2	connection A for filter 1 LEFT (f = 2.95 kHz)
n.c.	3	not connected
F1LB	4	connection B for filter 1 LEFT(f = 2.95 kHz)
F2LA	5	connection A for filter 2 LEFT (f = 12 kHz)
F2LB	6	connection B for filter 2 LEFT (f = 12 kHz)
F3LA	7	connection A for filter 3 LEFT (f = 790 Hz)
F3LB	8	connection B for filter 3 LEFT (f = 790 Hz)
F4LA	9	connection A for filter 4 LEFT (f = 205 Hz)
F4LB	10	connection B for filter 4 LEFT (f = 205 Hz)
F5LA	11	connection A for filter 5 LEFT (f = 59 Hz)
F5LB	12	connection B for filter 5 LEFT (f = 59 Hz)
V_{oL}	13	audio frequency output LEFT
V_P	14	supply voltage (+8.5 V)
SDA	15	I^2C-bus data line
SCL	16	I^2C-bus clock line
GND2	17	ground 2 (I^2C-bus ground)
MAD	18	modul address
GND1	19	ground 1 (analog ground)
V_{oR}	20	audio frequency output RIGHT
F5RB	21	connection B for filter 5 RIGHT (f = 59 Hz)
F5RA	22	connection A for filter 5 RIGHT (f = 59 Hz)
F4RB	23	connection B for filter 4 RIGHT (f = 205 Hz)
F4RA	24	connection A for filter 4 RIGHT (f = 205 Hz)
F3RB	25	connection B for filter 3 RIGHT (f = 790 Hz)
F3RA	26	connection A for filter 3 RIGHT (f = 790 Hz)
F2RB	27	connection B for filter 2 RIGHT (f = 12 kHz)
F2RA	28	connection A for filter 2 RIGHT (f = 12 kHz)
F1RB	29	connection B for filter 1 RIGHT (f = 2.95 kHz)
n.c.	30	not connected
F1RA	31	connection A for filter 1 RIGHT (f = 2.95 kHz)
V_{iR}	32	audio frequency input RIGHT

PIN CONFIGURATION

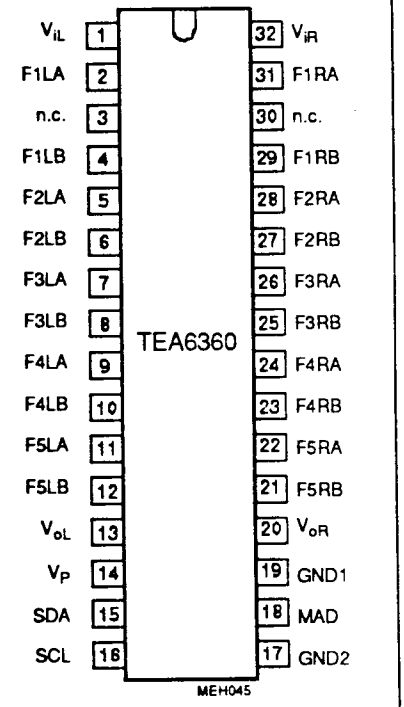


Fig.2 Pin configuration.

CHARACTERISTICS

V_P = 8.5 V; f_i = 1 kHz (R_S = 600 Ω), R_L = 10 kΩ, T_{amb} = 25 °C and measurements taken in Fig.1, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage.range (pin 14)		7	8.5	13.2	V
I_P	supply current (pin 14)	V_P = 8.5 V	-	24	-	mA
		V_P = 12 V	-	26	-	mA
Analog part						
R_i	input resistor (pins 1 and 32)		1	-	-	MΩ
$V_{1,32}$	input voltage range at any stage		2.1 to V_P–1	-	-	V
$V_{13,20}$	output voltage range at any stage		1.0 to V_P–1	-	-	V
V_o	output signal level (RMS value, pins 13 and 20)	control range 0 to +5, variable Q-factor or quasi constant Q-factor	1.1	-	-	V
R_o	output resistor (pins 13 and 20)		-	100	-	Ω
R_L	admissable load resistance at outputs (pins 13 and 20)		2	-	-	kΩ
C_L	admissable load capacitance at outputs (pins 13 and 20)		-	-	2.5	nF
G_v	total signal gain ($G = V_o / V_i$)	all filters linear	–0.5	-	0	dB
B	frequency response	all filters linear, roll off frequency for –1 dB				
	minimum value	(DC-coupled)	0	-	-	Hz
	maximum value		20	-	-	kHz
α_{Cr}	crosstalk attenuation between channels	f = 250 to 10000 Hz				
	all filters linear		60	75	-	dB
	all filters maximum boost		55	-	-	dB
	all filters maximum cut		55	-	-	dB
THD	distortion (pins 13 and 20)	f = 20 to 12500 Hz; V_P = 8.5 to 12 V				
	$V_{o\ (rms)}$ = 1.1 V	all filters linear	-	0.2	0.5	%
	$V_{o\ (rms)}$ = 0.1 V	all filters linear	-	0.05	0.2	%
	$V_{o\ (rms)}$ = 1.1 V	all filters max. boost	-	0.5	1.0	%
	$V_{o\ (rms)}$ = 0.1 V	all filters max. boost	-	0.1	0.3	%
	$V_{o\ (rms)}$ = 0.1 V	all filters maximum cut	-	0.2	0.5	%
	$V_{o\ (rms)}$ = 1 V	all filters max. boost f = 1 kHz	-	-	0.35	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_N	weighted output noise voltage (RMS value)	CCIR 468-3, maximum gain/filter of 12 dB				
	defeat mode		-	8	16	μV
	all filters linear		-	23	46	μV
	all filters maximum boost		-	70	140	μV
	all filters maximum cut		-	23	46	μV
α_{Cr}	crosstalk between bus inputs and signal outputs, 20 log ($V_{bus(p-p)}/V_{o(rms)}$)	all filters linear	-	120	-	dB
RR	ripple rejection at $V_{ripple\ (rms)}$ < 200 mV	all filters linear				
	for f = 100 Hz		-	70	-	dB
	for f = 40 to 12500 Hz		-	60	-	dB
Internal filters of analog part						
Q	Q-factor dependent on maximum gain					
	maximum gain 10 dB		0.1	-	1.2	
	maximum gain 12 dB		0.1	-	1.4	
	maximum gain 15 dB		0.1	-	1.8	
R_{tot}	total resistor of different filter sections		29.6	37.0	44.4	kΩ
ΔR_{tot}	tolerance between any filter section		-	-	±3	%
Internal controls of analog part via I²C-bus						
Step	number of steps for boost and cut		-	5	-	
	for linear		-	1	-	
	step resolution	maximum gain 12 dB	-	2.4	-	dB
	step set error		-	0.5	-	dB
ΔV_o	DC offset between any step or neighbouring step		-	-	±10	mV
I²C-bus control SDA and SCL, pins 15 and 16						
V_{IH}	input level HIGH		3	-	5	V
V_{IL}	input level LOW		0	-	1.5	V
I_I	input current		-	-	±10	μA
V_{ACK}	acknowledge voltage on SDA	I_{15} = 3 mA at LOW	-	-	0.4	V
Module address bit (pin 18)						
V_{IH}	input level HIGH for address 1000 0110		3	-	V_P	V
V_{IL}	input level LOW for address 1000 0100		0	-	1.5	V
I_I	input current		-	-	±10	μA
Power on reset: When reset is active the DEF-bit (defeat) is set and the I²C-bus receiver is in reset position.						
RESET	start of reset	increasing V_P	-	-	2.5	V
		decreasing V_P	4.2	5.0	5.8	V
	end of reset	increasing V_P	5.2	6.0	6.8	V

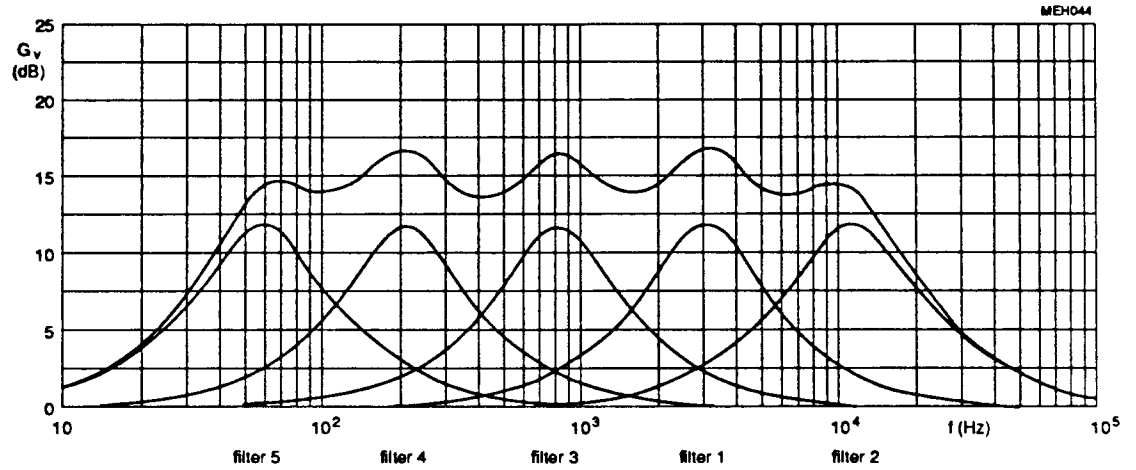


Fig.3 Frequency response for maximum boost of +12 dB according to Fig.1. For maximum cut the curves are symmetrical to negative gain values.

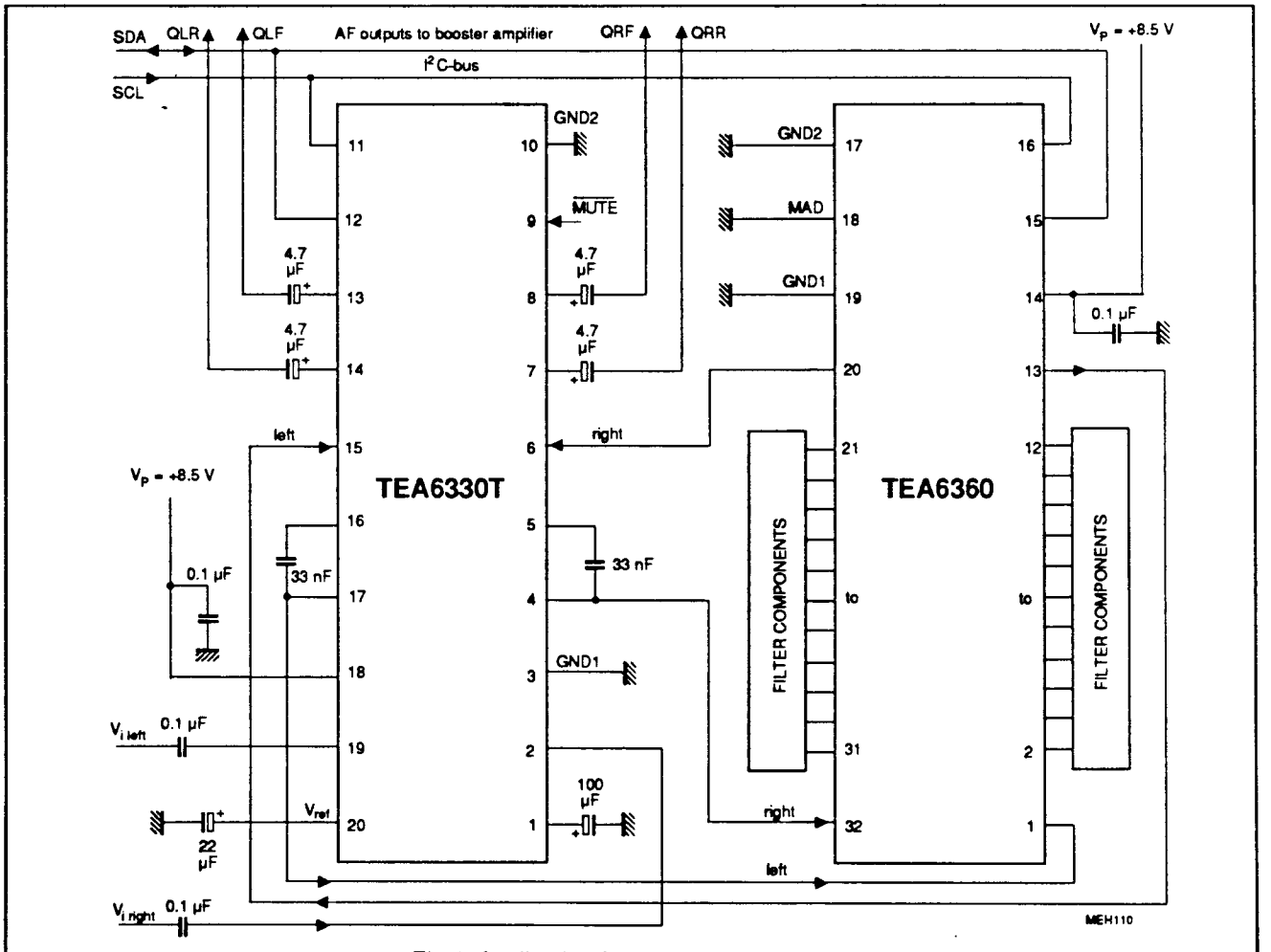


Fig.4 Application for car radio (V_P <8.5 V).

I²C-BUS PROTOCOL

I²C-bus format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

S = start condition
SLAVE ADDRESS = **1000 0100** when pin 18 is set LOW
or **1000 0110** when pin 18 is set HIGH or open-circuit
A = acknowledge, generated by the slave
SUBADDRESS = subadress byte, see Table 1
DATA = data byte, see Table 1
P = stop condition

If more than 1 byte DATA are transmitted, then auto-increment of the subaddress is performed.

Byte organisation

Table 1 I²C-bus subaddress/data

function	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
filter 1 /defeat	0 0 0 0 0 0 0 0	DEF	1B2	1B1	1B0	0	1C2	1C1	1C0
filter 2	0 0 0 0 0 0 0 1	0	2B2	2B1	2B0	0	2C2	2C1	2C0
filter 3	0 0 0 0 0 0 1 0	0	3B2	3B1	3B0	0	3C2	3C1	3C0
filter 4	0 0 0 0 0 0 1 1	0	4B2	4B1	4B0	0	4C2	4C1	4C0
filter 5	0 0 0 0 0 1 0 0	0	5B2	5B1	5B0	0	5C2	5C1	5C0

Function of the bits of Table 1:

1B0	to	1B2	boost control for filter 1
1B0	to	1B2	cut control for filter 1
2B0	to	2B2	boost control for filter 2
2B0	to	2B2	cut control for filter 2
3B0	to	3B2	boost control for filter 3
3B0	to	3B2	cut control for filter 3
4B0	to	4B2	boost control for filter 4
4B0	to	4B2	cut control for filter 4
5B0	to	5B2	boost control for filter 5
5B0	to	5B2	cut control for filter 5

DEF

DEF = 0 (defeat bit): All filters operating.
DEF = 1 : Linear frequency response, input is directly connected to the output of the output amplifier. The filter settings are stored but the internal amplification is controlled to 0 dB, independent on bits nB2 to nB0.

Table 2 Boost control for filter n.

DATA				
position		nB2	nB1	nB0
step 0	(no boost)	0	0	0
step 1		0	0	1
step 2		0	1	0
step 3		0	1	1
step 4		1	0	0
step 5	(maximum boost)	1	0	1
step 5	(maximum boost)	1	1	0
step 5	(maximum boost)	1	1	1

Table 3 Cut control for filter n.

DATA				
position		nB2	nB1	nB0
step 0	(no cut)	0	0	0
step 1		0	0	1
step 2		0	1	0
step 3		0	1	1
step 4		1	0	0
step 5	(maximum cut)	1	0	1
step 5	(maximum cut)	1	1	0
step 5	(maximum cut)	1	1	1

Table 4 Filter control with variable quality factor.

position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nB1	D0 nB0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (–0) = +5
+4	0	1	0	0	0	0	0	0	(+4) + (–0) = +4
+3	0	0	1	1	0	0	0	0	(+3) + (–0) = +3
+2	0	0	1	0	0	0	0	0	(+2) + (–0) = +2
+1	0	0	0	1	0	0	0	0	(+1) + (–0) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (–0) = 0
–1	0	0	0	0	0	0	0	1	(+0) + (–1) = –1
–2	0	0	0	0	0	0	1	0	(+0) + (–2) = –2
–3	0	0	0	0	0	0	1	1	(+0) + (–3) = –3
–4	0	0	0	0	0	1	0	0	(+0) + (–4) = –4
–5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (–5) = –5

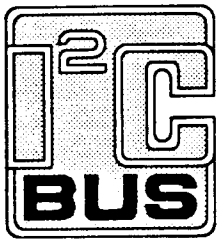
I2C-BUS PROTOCOL (continued).

Table 5 Filter control with constant quality factor.

position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nB1	D0 nB0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (−0) = +5
+4	0	1	0	1	0	0	0	1	(+5) + (−1) = +4
+3	0	1	0	1	0	0	1	0	(+5) + (−2) = +3
+2	0	1	0	1	0	0	1	1	(+5) + (−3) = +2
+1	0	1	0	1	0	1	0	0	(+5) + (−4) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (−0) = 0
−1	0	1	0	0	0	1	0	1	(+4) + (−5) = −1
−2	0	0	1	1	0	1	0	1	(+3) + (−5) = −2
−3	0	0	1	0	0	1	0	1	(+2) + (−5) = −3
−4	0	0	0	1	0	1	0	1	(+1) + (−5) = −4
−5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (−5) = −5

Table 6 Filter control with quasi-constant quality factor.

position	D7 X	D6 nB2	D5 nB1	D4 nB0	D3 X	D2 nC2	D1 nB1	D0 nB0	comment
+5 (maximum boost)	0	1	0	1	0	0	0	0	(+5) + (−0) = +5
+4	0	1	0	1	0	0	0	1	(+5) + (−1) = +4
+3	0	1	0	1	0	0	1	0	(+5) + (−2) = +3
+2	0	1	0	0	0	0	1	0	(+4) + (−2) = +2
+1	0	0	1	1	0	0	1	0	(+3) + (−2) = +1
0 (linear)	0	0	0	0	0	0	0	0	(+0) + (−0) = 0
−1	0	0	1	0	0	0	1	1	(+2) + (−3) = −1
−2	0	0	1	0	0	1	0	0	(+2) + (−4) = −2
−3	0	0	1	0	0	1	0	1	(+2) + (−5) = −3
−4	0	0	0	1	0	1	0	1	(+1) + (−5) = −4
−5 (maximum cut)	0	0	0	0	0	1	0	1	(+0) + (−5) = −5



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.