MA3764

RADIATION HARD 8192 x 8 BIT MASK-PROGRAMMABLE ROM

The MA3764 64k Mask Programmable ROM is configured as 8192x8 bits and manufactured using CMOS-SOS high performance, radiation hard, 1.5µm technology.

The design has fully static operation synchronised to the clock input. There are 3 mask programmable chip-select inputs to enable on chip decoding of the select signals. These may also be programmed so that any or all of them disable the address input buffers to conserve power when the chip is de-selected. An output enable signal is also provided to provide separate tristsate control for the output buffers.

Programming is performed during fabrication by customising the penultimate layer of the process. Programming data may be supplied in EPROM or as a data file in the standard INTEL Hex format.

Operation Mode	*$\overline{E}$	$\overline{C}$	$\overline{G}$	I/O	Power
Precharge	L	H	L	'1'	
Evaluate (Read)	L	L	L	D OUT	ISB 1
Output Disable	L	X	H	High Z	
Standby	H		X	High Z	ISB 2
	X		X	X	

*$\overline{E}$ is a mask programmed NAND function of E1, E2, E3 and their inverses.

Figure 1: Truth Table

FEATURES

- 1.5µm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 45ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset $>10^{11}$ Rad(Si)/sec
- SEU 4.3×10^{-11} Errors/bitday
- Single 5V Supply
- Three State Output
- Low Standby Current 100µA Typical
- -55°C to +125°C Operation
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation
- Programmable at Via Level for Fast Turnaround
- 3 Mask Programmable Chip Selects

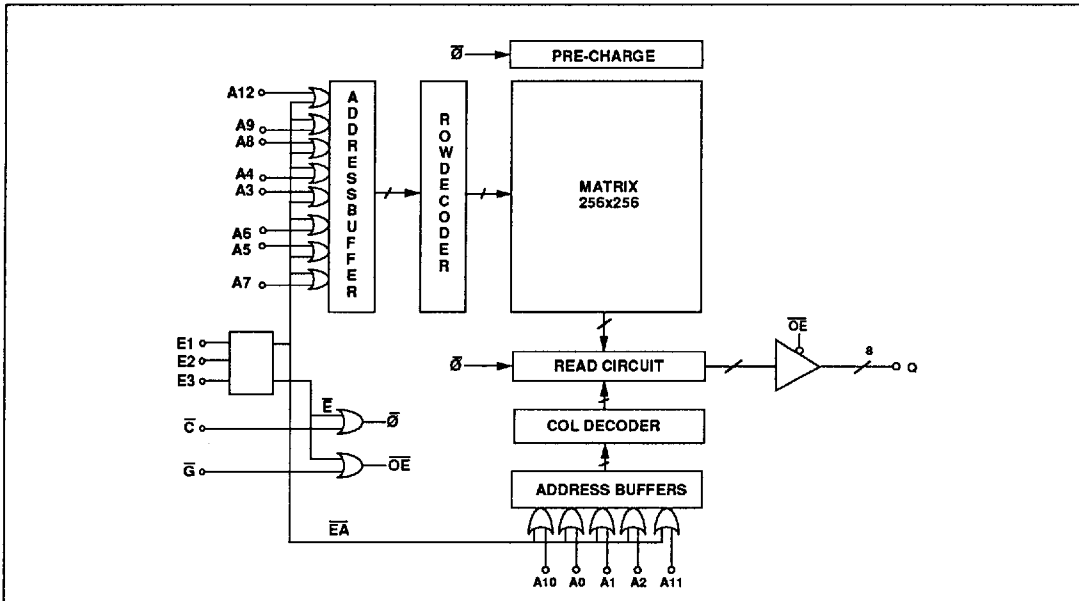

Figure 2: Block Diagram

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SIGNAL DEFINITIONS

A0-A12

Address input pins, these select a particular word within the memory array.

Q0-Q7

Data output pins, these are tristated when $\overline{E}$ is high (chip is de-selected). When the chip is selected, data is available an access time after a falling edge on $\overline{C}$ and is held during the time that $\overline{C}$ is high. This data appears on the output pins if the output enable ($\overline{G}$) is asserted, otherwise the output pins are tristated.

E1, E2, E3

Are mask-programmed to the customer's specification to form the active low chip select function, $\overline{E}$. $\overline{E}$ is driven by a 3-input NAND gate which has E1, E2 and E3 or their inverses as its inputs. Unused NAND gate inputs will be tied high internally. When $\overline{E}$ is at a high level it defaults the ROM to a precharge condition and holds the data output drivers in a high impedance state.

Similarly the E inputs may also be programmed to disable the address buffers when not asserted. This introduces a chip-select to clock-falling setup time for the relevant inputs but also reduces power consumption caused by the address lines changing while the chip is de-selected.

$\overline{C}$

A falling edge on this signal initiates a read operation. The chip is precharging during the time that $\overline{C}$ is high but the data from the previous read is held available for enabling to the output data pins.

$\overline{G}$

Output enable, when at a high level, this holds the data output pins in a high impedance state. When at low level, the data output driver state is defined by $\overline{E}$. If this signal is not used, it must be connected to V_{SS}.

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7.0	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Figure 3: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes for Table 4:
Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request). GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	- (TTL) (CMOS)	V_{DD}/2 0.8 V_{DD}	- -	V_{DD} V_{DD}	V V
V_{IL}	Logical '0' Input Voltage	- (TTL) (CMOS)	V_{SS} V_{SS}	- -	0.8 0.2 V_{DD}	V V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -4mA	2.4	-	-	V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -3mA	V_{DD}-0.5	-	-	V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 5mA	-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} all inputs	-	-	±10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}	-	-	±10	µA
I_{SB1}	Selected Static Current (CMOS)	All inputs = V_{DD}-0.2V except $\overline{E}$ = V_{SS}+0.2V	-	0.1	2	mA
I_{DD}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD}-0.2V	-	3	10	mA
I_{SB2}	Standby Supply Current	$\overline{E}$ = V_{DD}-0.2V	-	0.1	2	mA

Figure 4: Electrical Characteristics

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AC CHARACTERISTICS

Conditions of Test for Table 5:
1. Input pulse = V_{SS} to 4.0V.
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mV from steady state (T_{EVOX}, T_{EXQZ}, T_{GLQX}, T_{GHQZ}).
6. These parameters are sampled and not 100% tested (T_{EVQX}, T_{EXQZ}, T_{GLQX}, T_{GHQZ}).

Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	Min	Max	Units
TEAVCL (Note 1)	Enable 1 valid to clock low	40	-	ns
TEVCL (Note 2)	Enable valid to clock low	5	-	ns
TEVQX	Enable valid to outputs driven	-	30	ns
TCLQV	Access time	-	55	ns
TCLCH	Clock low time	60	-	ns
TCHCL	Clock high time	40	-	ns
TAVCL	Address setup time	40	-	ns
TCHAX	Address hold time	0	-	ns
TCLQX	Data hold time after falling clock	0	-	ns
TEXQZ (Note 2)	Chip disabled to outputs tristate	-	30	ns
TGLQX	Output enable low to outputs driven	-	15	ns
TGHQZ	Output enable high to outputs tristate	-	10	ns

Note 1: Applies to E inputs which are programmed to disable the address inputs. Time is to clock-low from the last of such inputs to be asserted.

Note 2: TEVCL and TEXQZ are timed from the last of the E inputs being asserted. This does not apply to inputs which are used to disable the address inputs in the case of TEVCL.

Figure 5: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 6: Capacitance

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Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 7: Functionality

Subgroup	Definition
1	Static characteristics specified in Table 4 at +25°C
2	Static characteristics specified in Table 4 at +125°C
3	Static characteristics specified in Table 4 at -55°C
7	Functional characteristics specified in Table 7 at +25°C
8A	Functional characteristics specified in Table 7 at +125°C
8B	Functional characteristics specified in Table 7 at -55°C
9	Switching characteristics specified in Table 5 at +25°C
10	Switching characteristics specified in Table 5 at +125°C
11	Switching characteristics specified in Table 5 at -55°C

Figure 8: Definition of Subgroups

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TIMING DIAGRAMS

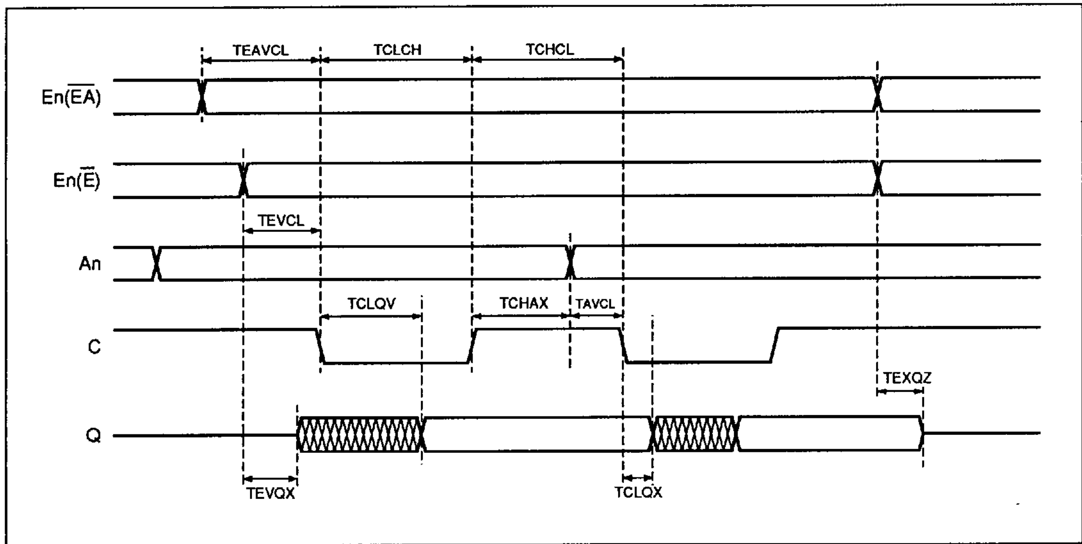

Figure 9: Read Cycles

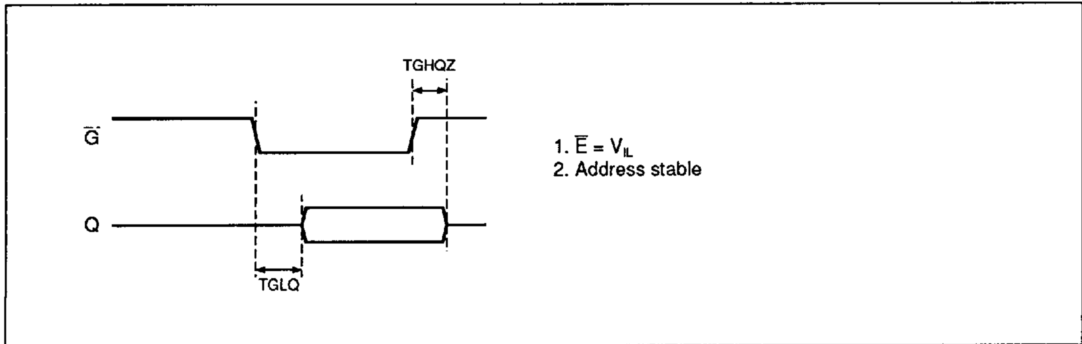

Figure 10: Output Enable Operation

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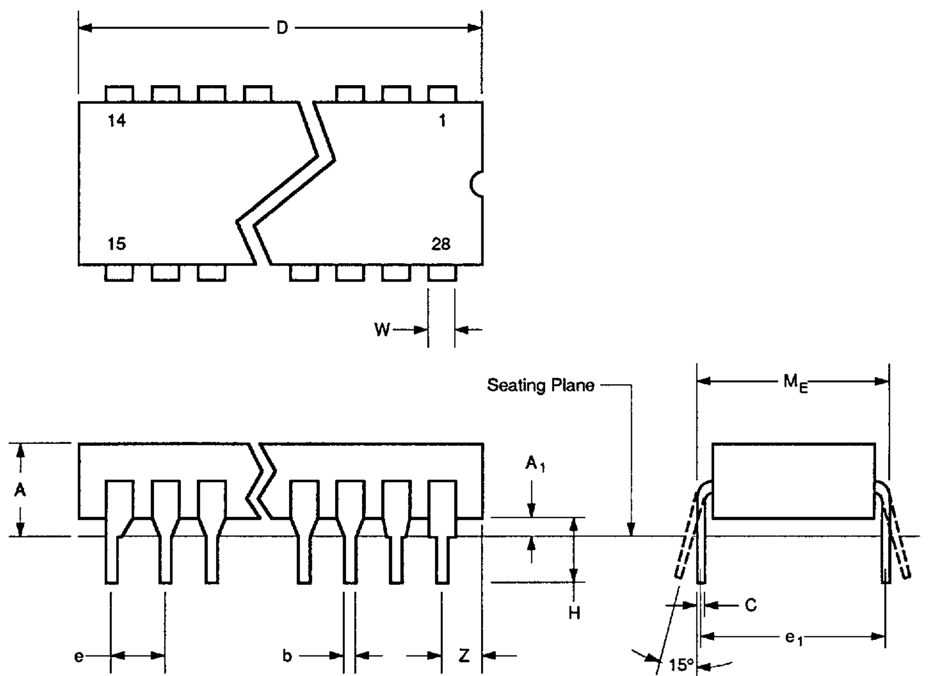
OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	36.02	-	-	1.418
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG404

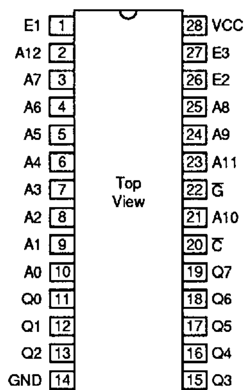


Figure 11: 28-Lead Ceramic DIL (Solder Seal) - Package Style C

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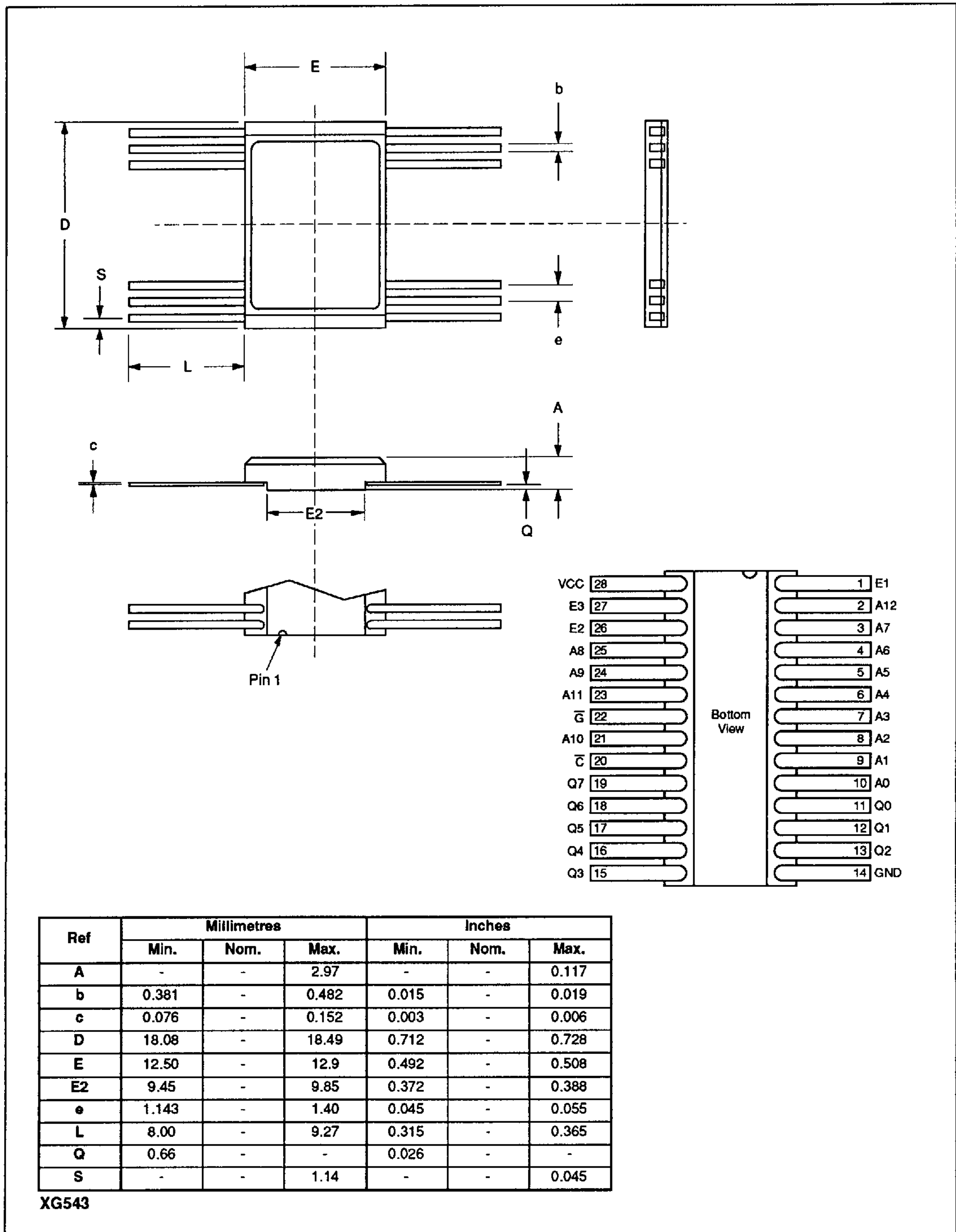

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.97	-	-	0.117
b	0.381	-	0.482	0.015	-	0.019
c	0.076	-	0.152	0.003	-	0.006
D	18.08	-	18.49	0.712	-	0.728
E	12.50	-	12.9	0.492	-	0.508
E2	9.45	-	9.85	0.372	-	0.388
e	1.143	-	1.40	0.045	-	0.055
L	8.00	-	9.27	0.315	-	0.365
Q	0.66	-	-	0.026	-	-
S	-	-	1.14	-	-	0.045

XG543

Figure 12: 28-Lead Ceramic Flatpack (Solder Seal) - Package Style F

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RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

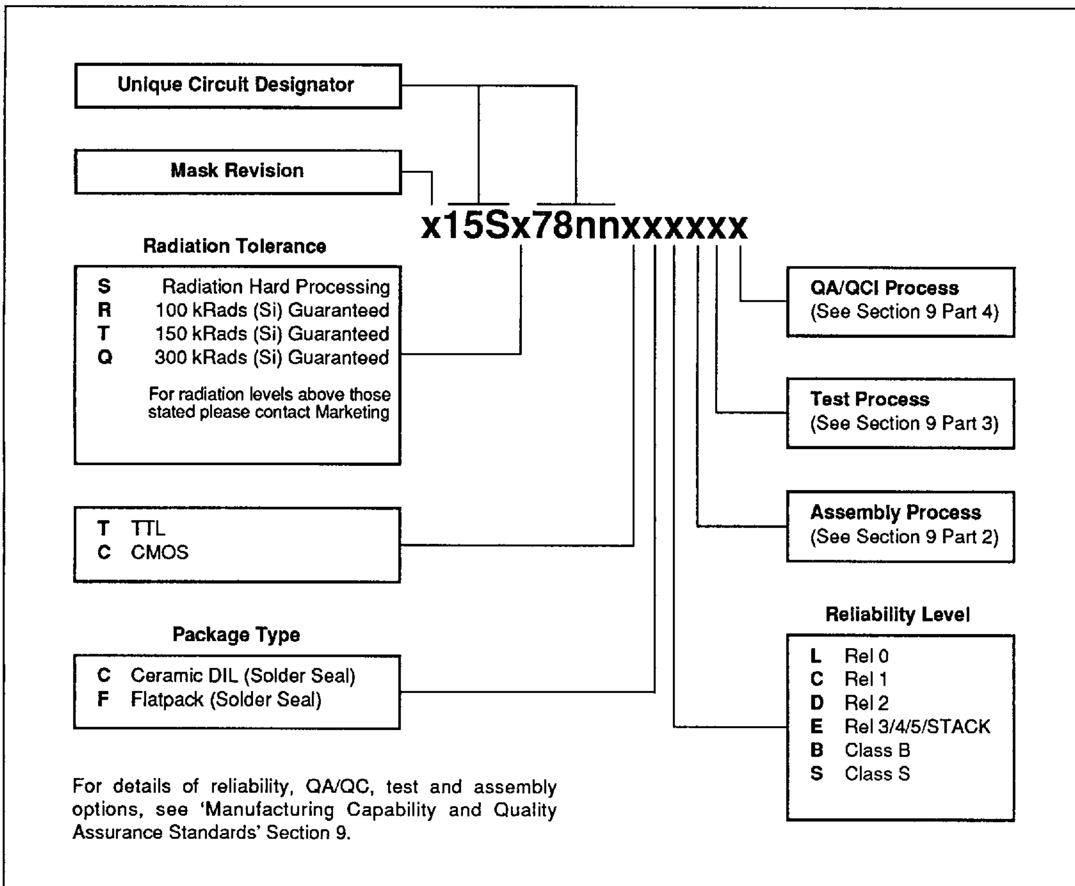
Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-11}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 13: Radiation Hardness Parameters

ORDERING INFORMATION



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