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SC68C92

Dual asynchronous receiver/transmitter (DUART)

DESCRIPTION

The SC68C92 is a pin and function replacement for the SCC68692 with added features and deeper fifos. Its configuration on power up is that of the SCC68692. Its differences from the SCC68692 are: 8 character receiver, 8 character transmit fifos, receiver watch dog timer, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts.

The Signetics SC68C92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is buffered by eight character fifos to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC68C92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

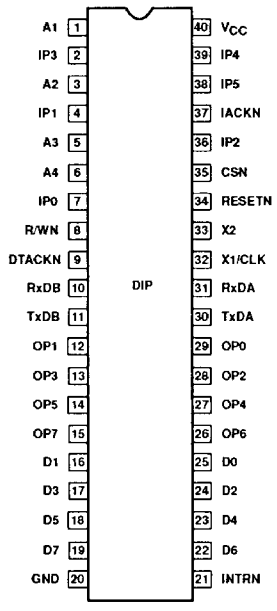
The SC68C92 is available in three package versions: 40-pin and 28-pin, 0.6" wide, DIPs and a 44-pin PLCC.

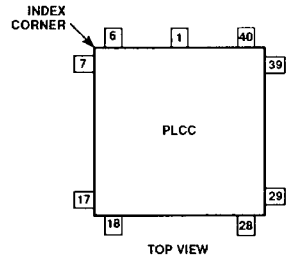
FEATURES

- S6800 bus compatible
- Dual full-duplex independent asynchronous receiver/transmitters
- 8 character fifos for each receiver and transmitter
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Other baud rates to 230.4k baud at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
  - Each fifo can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial, industrial and military temperature range versions
- TTL compatible
- Single +5V power supply

Dual asynchronous receiver/transmitter (DUART) SC68C92

PIN CONFIGURATIONS





PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A1	24	INTRN
3	IP3	25	D6
4	A2	26	D4
5	IP1	27	D2
6	A3	28	D0
7	A4	29	OP6
8	IP0	30	OP4
9	R/WN	31	OP2
10	DTACKN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CSN
18	D1	40	IP2
19	D3	41	IACKN
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

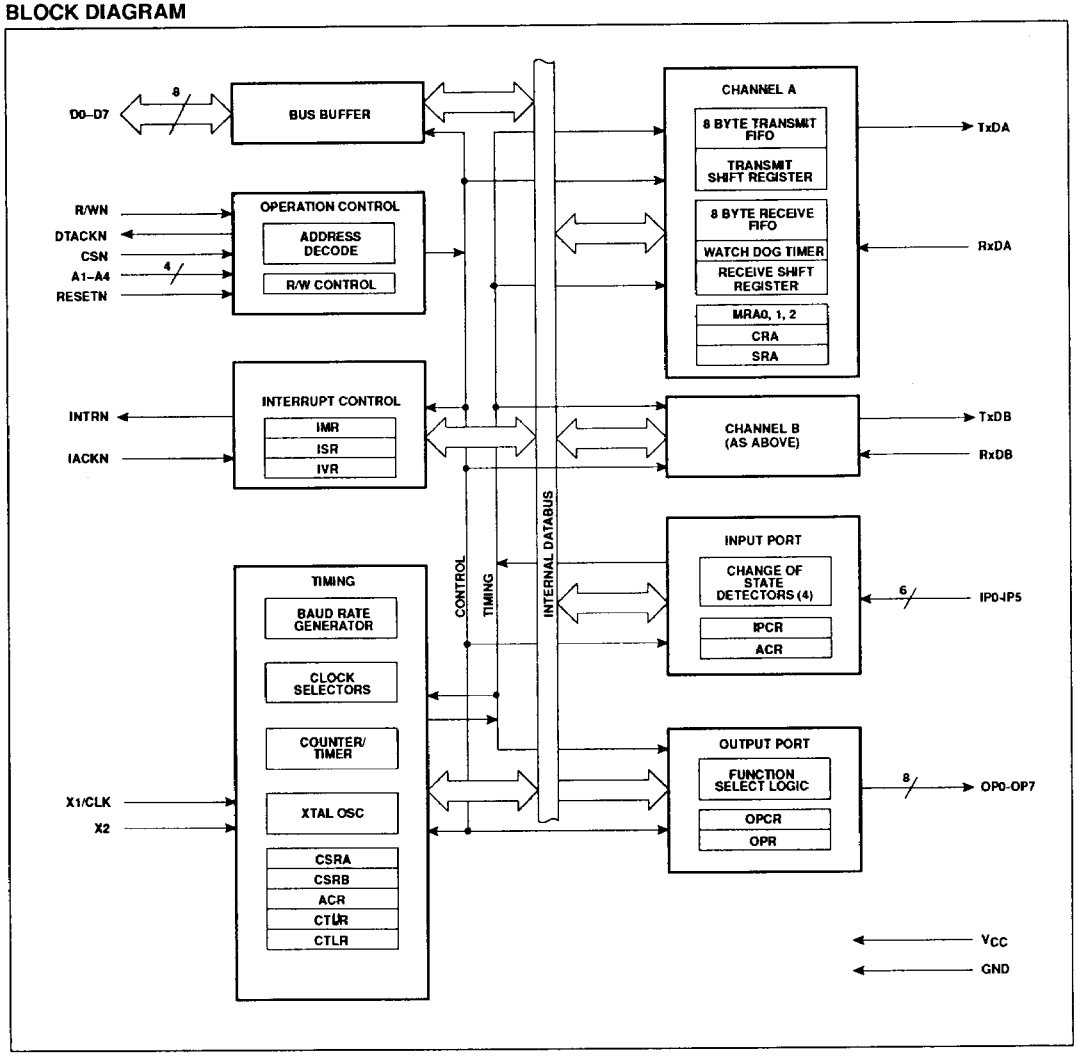
ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C
40-Pin Cerdip	SC68C92C1F40	SC68C92E1F40
40-Pin Plastic DIP	SC68C92C1N40	SC68C92E1N40
44-Pin Plastic LCC	SC68C92C1A44	SC68C92E1A44

Dual asynchronous receiver/transmitter (DUART)

SC68C92

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NO.	TYPE	NAME AND FUNCTION
D0–D7	25,16,24,17 23,18,22,19	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	35	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A1–A4 inputs. When CEN is High, the DUART places the D0–D7 lines in the 3-State condition.
R/WN	8	I	**Read/Write:** A High input indicates a read cycle and a low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1–A4	1,2,5,6	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	34	I	**Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state.
DTACKN	9	O	**Data Transfer Acknowledge:** 3-State active-Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	21	O	**Interrupt Request:** Active-Low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	37	I	**Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	32	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	33	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin can be left open.
RxDA	31	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	10	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	30	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	11	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	29	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	12	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	28	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	13	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	27	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	14	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	26	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	15	O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYBN output.
IP0	7	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	4	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	36	I	**Input 2:** General purpose input or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP3	2	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	39	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	38	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	40	I	**Power Supply:** +5V supply input.
GND	20	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	−0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	−0.5 to V_{CC} +0.5	V
P_D	Power dissipation[5]	750	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. Maximum power dissipation of the chip when outputs are loaded externally. For operating current, see DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[6]		2.0			V
V_{IH}	Input high voltage (except X1/CLK)[7]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		0.8V_{CC}			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = −400µA	V_{CC} −0.5			V
I_{IX1PD}	X1/CLK input current – power down	V_{IN} = 0 to V_{CC}	−10		+10	µA
I_{ILX1}	X1/CLK input low current – operating	V_{IN} = 0	−75		0	µA
I_{IHX1}	X1/CLK input high current – operating	V_{IN} = V_{CC}	0		75	µA
I_{OHX2}	X2 output high current – operating	V_{OUT} = V_{CC}, X1 = 0	0		+75	µA
I_{OHX2S}	X2 output high short circuit current – operating	V_{OUT} = 0, X1 = 0	−10		−1	mA
I_{OLX2}	X2 output low current – operating	V_{OUT} = 0, X1 = V_{CC}	−75		0	µA
I_{OLX2S}	X2 output low short circuit current – operating and power down	V_{OUT} = V_{CC}, X1 = V_{CC}	1		10	mA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	−10		+10	µA
	Input port pins	V_{IN} = 0 to V_{CC}	−20		+10	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			10	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0V	−10			µA
I_{ODL}	Open-drain output low current in off State	V_{IN} = 0	−10			µA
I_{ODH}	Open-drain output high current in off State	V_{IN} = V_{CC}			10	µA
I_{CC}	Power supply current[5]					
	Operating mode	TTL input levels			10	mA
		CMOS input levels			10	mA
		TTL input levels			3.0	mA
	Power down mode	CMOS input levels			TBD	µA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of V_{CC} −0.2V and V_{SS} + 0.2V.
6. $T_A \geq 0°C$
7. $T_A < 0°C$

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ[3]	Max	
Reset Timing						
t_{RES}	1	RESET pulse width	1.0			µs
Bus Timing[5]						
t_{AS}	2,3,4	A1–A4 setup time to CSN Low	10			ns
t_{AH}	2,3,4	A1–A4 hold time from CSN Low	30			ns
t_{RWS}	2,3,4	RWN setup time to CSN High	0			ns
t_{RWH}	2,3,4	RWN holdup time to CSN High	0			ns
t_{CSW}[8]	2,3,4	CSN High pulse width	50			ns
t_{CSD}[9]	2,3,4	CSN or IACKN High from DTACKN Low	20			ns
t_{DD}	2,3,4	Data valid from CSN or IACKN Low			110	ns
t_{DA}	2	RDN Low to data bus active[8]	15			ns
t_{DF}	2,3,4	Data bus floating from CSN or IACKN High[8]			45	ns
t_{DI}	2	RDN High to data bus invalid[8]	20			ns
t_{DS}	2,3,4	Data setup time to CLK High	75			ns
t_{DH}	2,3,4	Data hold time from CSN High	0			ns
t_{DAL}	2,3,4	DTACKN Low from read data valid	0			ns
t_{DCR}	2,3,4	DTACKN Low (read cycle) from CLK High			45	ns
t_{DCW}	2,3,4	DTACKN Low (write cycle) form CLK High			45	ns
t_{DAH}	2,3,4	DTACKN High from CSN or IACKN High			30	ns
t_{DAT}	2,3,4	DTACKN High impedance from CSN or IACKN High			45	ns
t_{CSC}[7]	2,3,4	CSN or IACKN setup time to clock High	30			ns
Port Timing[5]						
t_{PS}	5	Port input setup time to CSN Low	0			ns
t_{PH}	5	Port input hold time from CSN High	0			ns
Interrupt Timing						
t_{IR}	6	INTRN (or OP3–OP7 when used as interrupts) negated from:				
		Read RHR (RxRDY/FFULL interrupt)			100[10]	ns
		Write THR (TxRDY interrupt)			100[10]	ns
		Reset command (break interrupt)			100[10]	ns
		Stop C/T command (counter interrupt)			100[10]	ns
		Read IPCR (input port change interrupt)			100[10]	ns
		Write IMR (clear of interrupt mask bit)			100[10]	ns
Clock Timing						
t_{CLK}	7	X1/CLK High or Low time	80			ns
f_{CLK}	7	X1/CLK frequency	1	3.6864	4	MHz
t_{CTC}	7	CTCLK (IP2) High or Low time	60			ns
f_{CTC}	7	CTCLK (IP2) frequency[9]	100		8	MHz
t_{RX}	7	RxC High or Low time	220			ns
f_{RX}	7	RxC frequency (16X)[9]	100		2	MHz
		(1X)[9]	100		1	MHz
t_{TX}	7	TxC High or Low time	220			ns
f_{TX}	7	TxC frequency (16X)[9]	0		2	MHz
		(1X)[9]	0		1	MHz
Transmitter Timing						
t_{TXD}	8	TxD output delay from TxC Low			120	ns
t_{TCS}	8	Output delay from TxC Low to TxD data output			50	ns
Receiver Timing						
t_{RXS}	9	RxD data setup time to RxC High	100			ns
t_{RXH}	9	RxD data hold time from RxC High	100			ns

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
6. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
7. This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.
8. Guaranteed by characterization of sample units.
9. Minimum frequencies are not tested but are guaranteed by design.
10. 325ns maximum for T_A > 70°C.

BLOCK DIAGRAM

The SC68C92 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR), the Auxiliary Control Register (ACR), and the Interrupt Vector Register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR register on the data bus and asserting DTACKN.

Outputs OP3–OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Programming bit 0 of MR0 to a "1" gives additional baud rates of 57.6kB, 115.2kB and 230.4kB. These will be in the 16X mode. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SC68C92 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 6-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always be read as a logic 1 and D6 will reflect the level of IACKN. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 – 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The

detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

The 8-bit multipurpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also be individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SC68C92 is conditioned to transmit data when the transmitter is enabled through the command register. The SC68C92 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When the transmitter is initially enabled the TxRDY and TxEMPTY bits will be set in the status register. When a character is loaded to the transmit fifo the TxEMPTY bit will be reset. The TxEMPTY will not set until: 1) the transmit fifo is empty and the transmit shift register has finished transmitting the stop bit of the last character written to the transmit fifo, or 2) the transmitter is disabled and then re-enabled. The TxRDY bit is set whenever the transmitter is enabled and the TxFIFO is not full. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first.

Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SC68C92 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7–1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of eight characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all eight stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. Register Addressing

A4	A3	A2	A1	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Reserved	Interrupt Vector Register (IVR)
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

REGISTER DESCRIPTIONS

Mode Registers

MR0 is accessed by setting the MR pointer to 0 via the command register command D.

MR0A

MR0[7] – This bit controls the receiver watch dog timer. 0 = disable, 1 = able. When enabled, the watch dog timer will generate a receiver interrupt if the receiver FIFO has not been accessed within 64 bit times of the receiver 1X clock. This is used to alert the control processor that data is in the RHR that has not been read. This situation may occur when the last part of a message is not large enough to generate an interrupt.

MR0[6] – Bit 2 of receiver FIFO interrupt level. This bit along with Bit 6 of MR1 sets the fill level of the 8 byte FIFO that generates the receiver interrupt.

MR0[6]	MR1[6]	Interrupt Condition
0	0	1 or more bytes in FIFO (Rx RDY)
0	1	3 or more bytes in FIFO
1	0	6 or more bytes in FIFO
1	1	8 or more bytes in FIFO (Rx FULL)

MR0[5:4] – Tx interrupt fill level.

MR0[5]	MR0[4]	Interrupt Condition
0	0	8 bytes empty (Tx EMPTY)
0	1	4 or more bytes empty
1	0	6 or more bytes empty
1	1	1 or more bytes empty (Tx RDY)

MR0[3] – Not used. Should be set to 0.

MR0[2:1] – Test 1 and Test 2. Used for factory test. Set to 0

MR0[0] – Baud rate extend. 0 = Normal baud rates. 1 = Extend baud rate. 57.6kB, 115.2kB, 230.4kB.

Note: MR0[3:0] are not used in channel B. They should be set to 0.

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select

This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the "block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.

2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been retransmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the THR, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR0A MR0B	Rx WATCH DOG 0 = Disable 1 = Enable	RxINT (2)	TxINT (1:0)	DON'T CARE Set to 0	TEST 1 Set to 0	TEST 2 Set to 0	BAUD RATE EXTEND 0 = Normal 1 = Extend

NOTE:
MR0B[3:0] are not implemented. When writing to MR0B set them to 0. A read of MR0B[3:0] returns 1111.

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	RxINT SELECT	ERROR MODE	PARITY MODE	PARITY TYPE	BITS PER CHARACTER
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE	TxRTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CSRA CSRB	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
	See Text				See Text			

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CRA CRB	MISCELLANEOUS COMMANDS				DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
	See Text				0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:

* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	11 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INT
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTUR	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTLR	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
IVR	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	Baud Rate ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3–16X	IP3–16X
1111	IP3–1X	IP3–1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

Table 3. Baud Rate

CSRA[7:4]	MR0[0] = 0		MR0[0] = 1	
	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	50	450
0001	110	110	110	110
0010	134.5	134.5	134.5	230.4K
0011	200	150	200	900
0100	300	300	1800	1800
0101	600	600	3600	3600
0110	1,200	1,200	7200	7,200
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	14.4K	14.4K
1001	4,800	4,800	28.8K	28.8K
1010	7,200	1,800	7,200	1,800
1011	9,600	9,600	57.6K	57.6K
1100	38.4K	19.2K	230.4K	115.2K
1101	Timer	Timer	Timer	Timer
1110	IP4-16X	IP4-16X	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X	IP4-1X	IP4-1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select

This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP6–16X	IP6–16X
1111	IP6–1X	IP6–1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select

This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5–16X	IP5–16X
1111	IP5–1X	IP5–1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7:4] – Miscellaneous Commands

The encoded value of this field may be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.

0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Set MR pointer to 0.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued

1101 Not used.

1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only. Design Note: The part will not output DTACKN while in power down mode. Use automatic DTACKN generation.

1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

CRA[3] – Disable Channel A Transmitter

This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter

Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver

This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver

Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of comamnds "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break

This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In the special multidrop mode, the parity error bit stores the received A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the Channel A transmitter underruns; i.e., both the Transmit Holding Register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

SOPR – Set the Output Port Bits (OPR)

SOPR[7:0] – Ones in the byte written to this register will cause the corresponding bit positions in the OPR to set to 1. Zeros have no effect.

ROPR – Reset Output Port Bits (OPR)

ROPR[7:0] – Ones in the byte written to the ROPR will cause the corresponding bit positions in the OPR to set to 0. Zeros have no effect.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL BAUD RATE	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	–0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	–0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

NOTE:
Duty cycle of 16x clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR [6:4] Field Definition

[6:4]	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or external clock (x1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change In Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

IVR – Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.

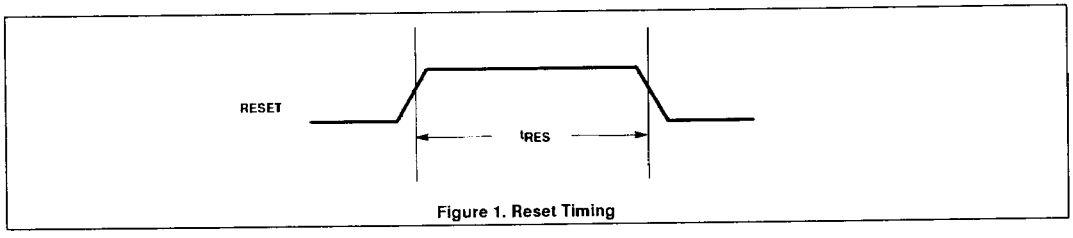


Figure 1. Reset Timing

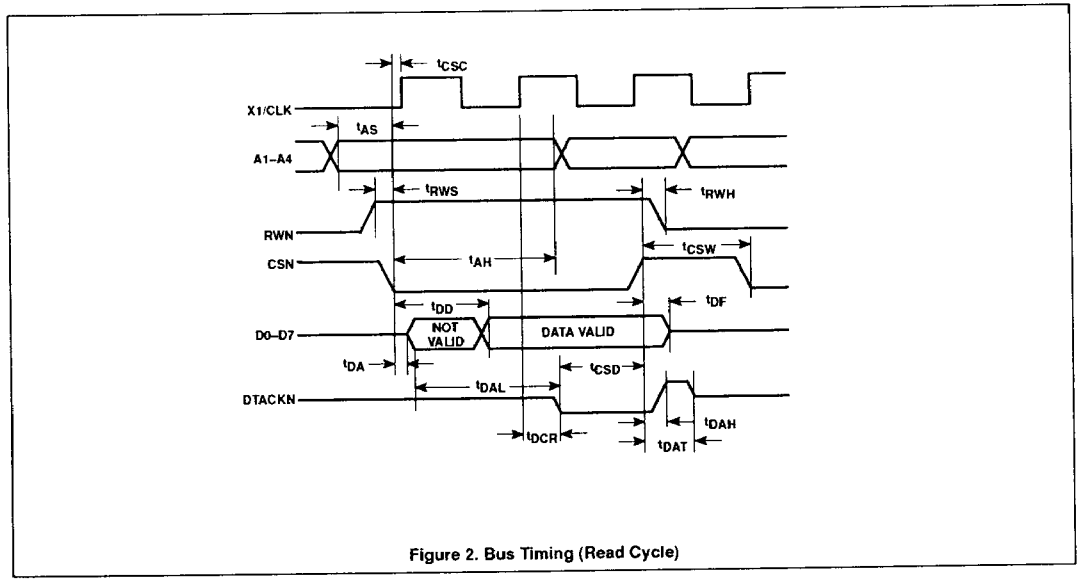


Figure 2. Bus Timing (Read Cycle)

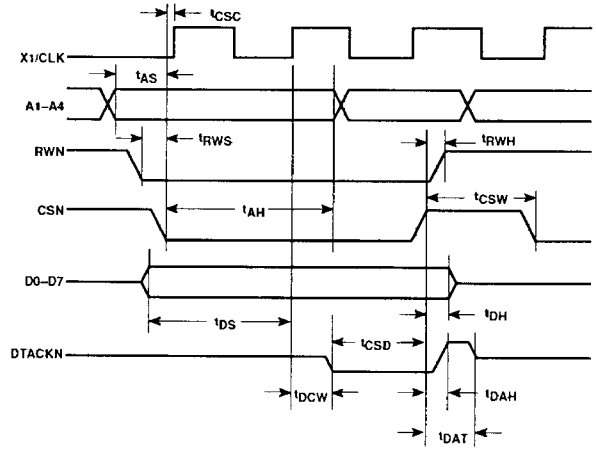


Figure 3. Bus Timing (Write Cycle)

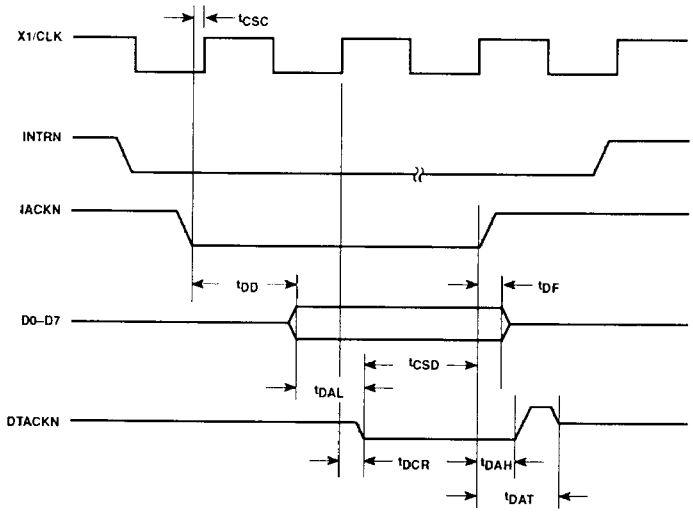


Figure 4. Interrupt Cycle Timing

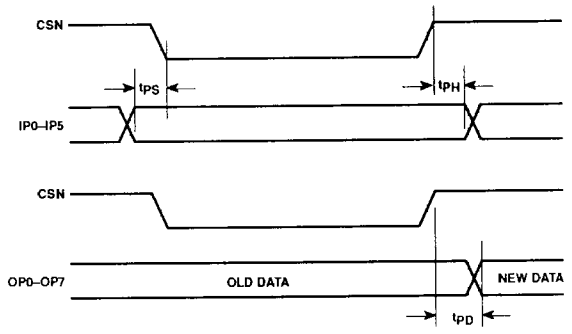
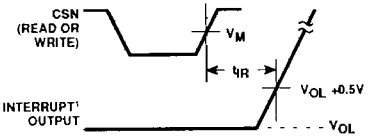


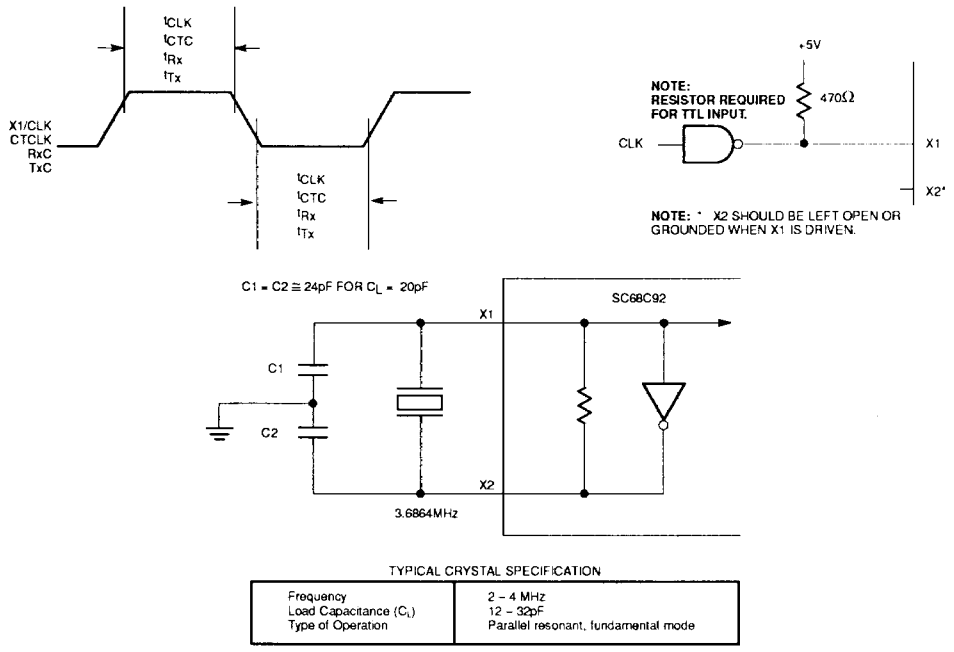
Figure 5. Port Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from thermidpoint of the switching signal, V_M, to a point 0.5 volts above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 6. Interrupt Timing



TYPICAL CRYSTAL SPECIFICATION

Frequency	2 – 4 MHz
Load Capacitance (C_L)	12 – 32pF
Type of Operation	Parallel resonant, fundamental mode

Figure 7. Clock Timing

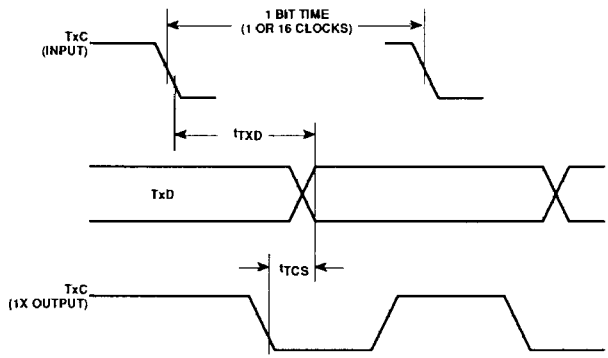


Figure 8. Transmit Timing

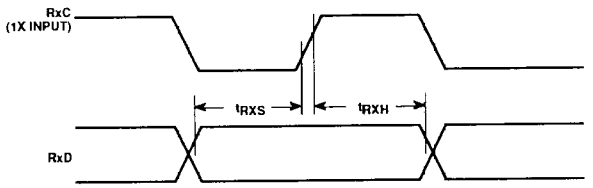
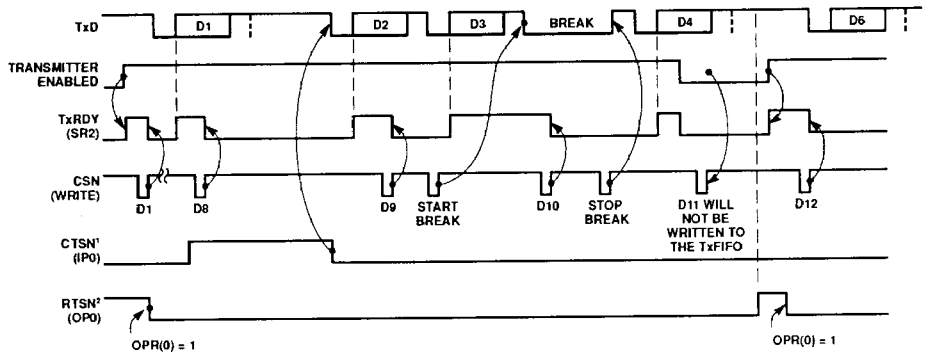
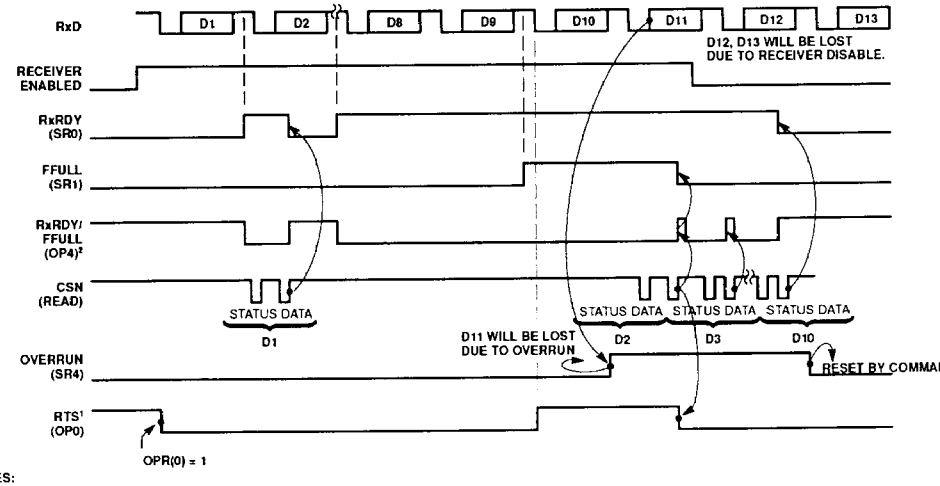


Figure 9. Receive Timing



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 10. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) and MR1(6) = 0.

Figure 11. Receiver Timing

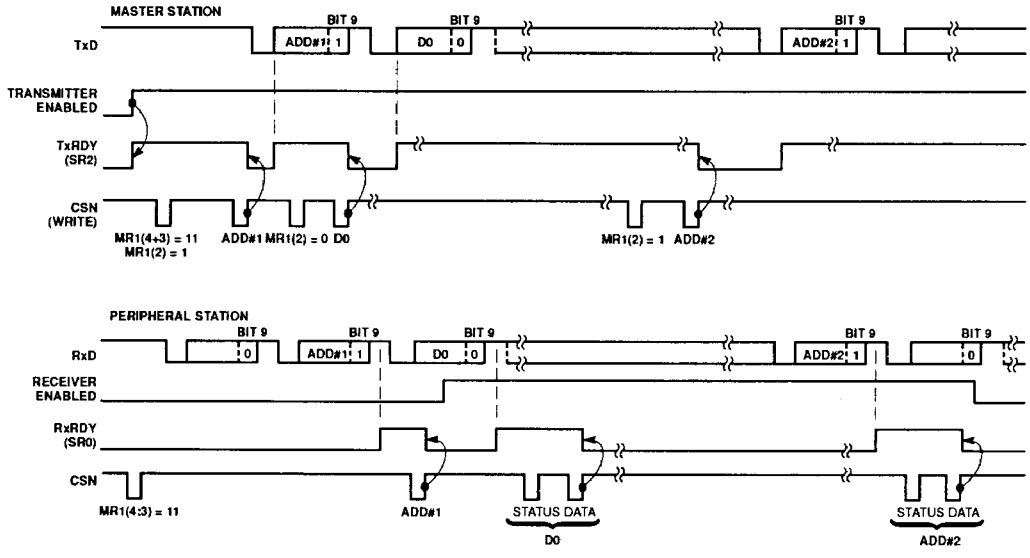


Figure 12. Wake-Up Mode

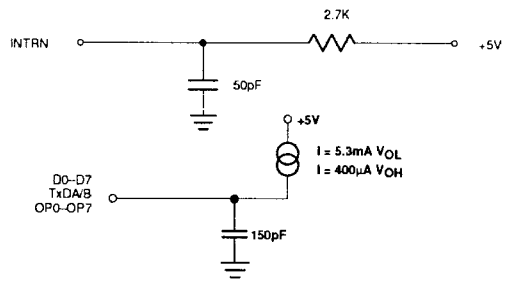


Figure 13. Test Conditions on Outputs