DYNAMIC RAM

OUTLINE

The DRAM series is made up of dynamic random access memory.
Memory capacity is from 1M Bytes to 8M Bytes.

VARIATION

Part Number	Memory Size	Description
DWE100CMD0	1M Bytes	1M × (512K × 16 bits + 2 Parity) DRAM CARD
DWE400CMD0	4M Bytes	4M × (2M × 16 bits + 2 Parity) DRAM CARD
DWE800CMD0	8M Bytes	8M × (4M × 16 bits + 2 Parity) DRAM CARD

SIZE

(1) 54.0 mm wide by 85.6 mm long by 3.5 mm thick

(2) Connector thickness is 3.0 mm

(3) Card type: 60 pin Two-piece type.

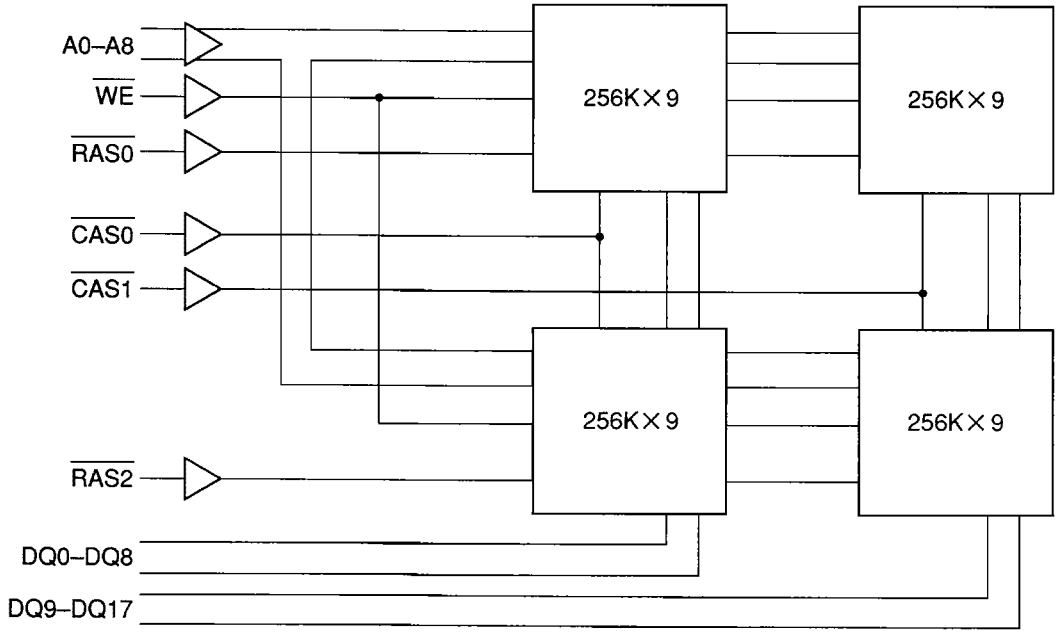
FEATURES

SPEED AND ORGANIZATION

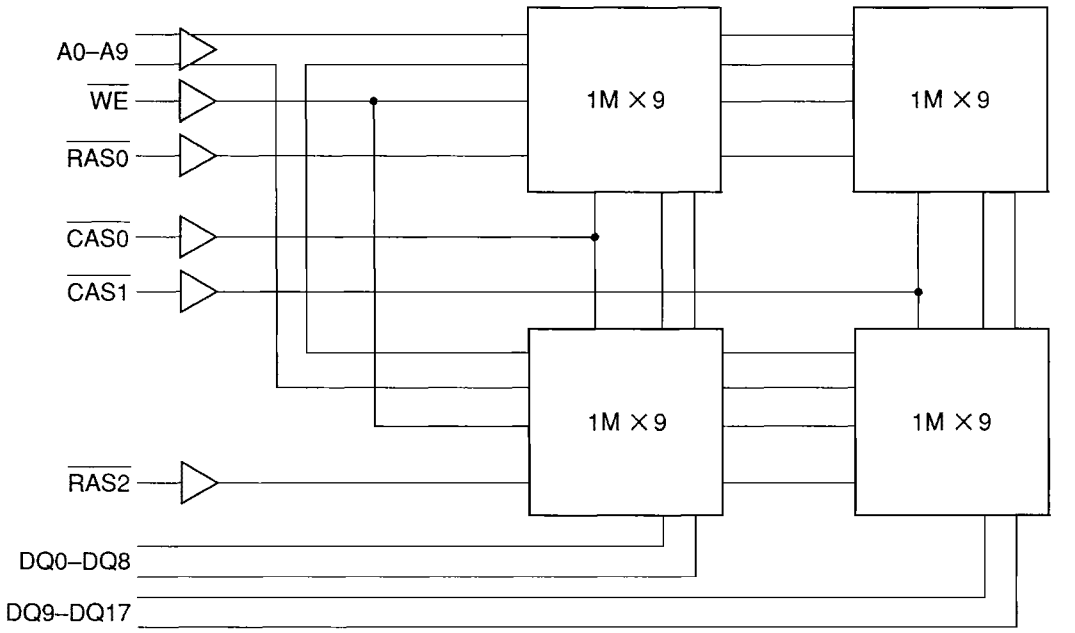
Part No.	t_{RAC} (Max)	Organization
DWE100CMD0	80/100 ns	512K × 18, 2 RAS
DWE400CMD0	80/100 ns	2M × 18, 2 RAS
DWE800CMD0	80/100 ns	4M × 18, 1 RAS

BLOCK DIAGRAM

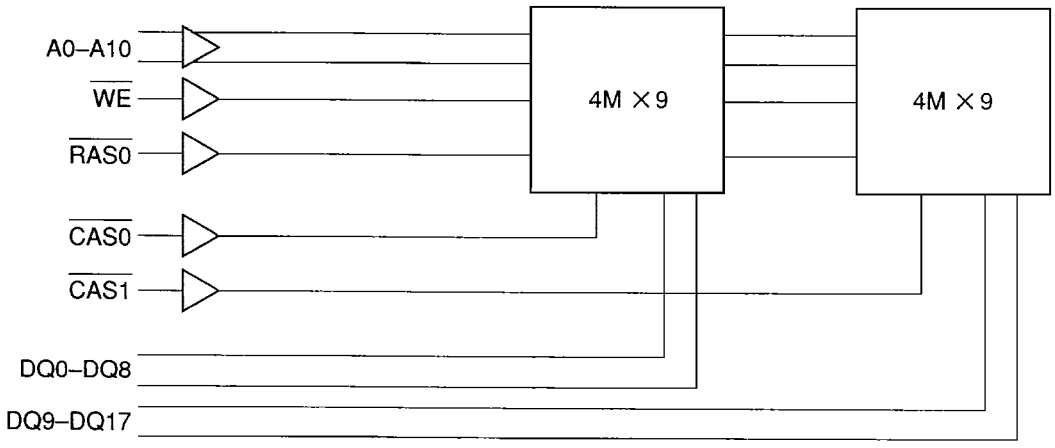
(1) DWE100CMDO



(2) DWE400CMDO



(3) DWE800CMDO



INTERFACE SIGNAL DIRECTION

(1) A0 – A10

Address Inputs
Unused address lines should be "no connect".

(2) DQ0 – DQ17

Data Inputs/Outputs
DQ8 and DQ17 are used for parity.

(3) $\overline{WE}$

Write Enable input (Active LOW)

(4) $\overline{RAS0}$, $\overline{RAS2}$

Row Address Strobe Inputs (Active LOW)
Only one RAS input may be active at any point in time, except during a RAS only refresh cycle or a CAS before RAS refresh cycle.

(5) $\overline{CAS0}$, $\overline{CAS1}$

Column Address Strobe Inputs (Active LOW)
CAS0 for DQ0 – DQ8, CAS1 for DQ9 – DQ17.

(6) PD1 – PD5

Presence Detect Pins
PD1, PD2, and PD3 for configuration, PD4 and PD5 for speed.

(7) V_{CC}

Positive Voltage Supply : +5 V ±5%.

(8) Vss

Device Ground Pin
All voltages are referenced to this pin.

MAXIMUM RATING

Parameter	Min	Max	Unit
Supply Voltage	–0.5	+6.0	V
Signal Voltage	–0.5	+6.0	V
Power Dissipation	—	7.2	W
Storage Temperature	–10	60	°C
Short Circuit Current	—	50	mA

CAPACITANCE (TA = 25°C, f = 1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{I1}	Input Capacitance on Address	—	20	pF
C_{I2}	Input Capacitance on $\overline{RAS}$	—	60	pF
C_{I3}	Input Capacitance on $\overline{CAS}$, $\overline{WE}$	—	20	pF
C_O	Capacitance on DQ0 – DQ17	—	45	pF

Note: The above figures are reference only

DC RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
T_A	Operating Ambient Temperature	0	50	°C
V_{IH}	High Level Input Voltage	2.4	V_{CC} +0.5	V
V_{IL}	Low Level Input Voltage	–0.5	0.8	V

DC OPERATING CHARACTERISTICS

(1) DC OPERATING CHARACTERISTICS

Symbol	Parameter	Test Condition	Variation	Min	Max	Unit
I_{LI}	Input Leakage Current	At any Input, All other Inputs not under test = 0 V	All	–1	–1	µA
		$\overline{RAS}$ Input	1M Bytes 4M Bytes 8M Bytes	–60 –60	–60 –60	
I_{LO}	Output Leakage Current	Output Disabled	All	–20	–20	µA
V_{OH}	High Output Voltage	I_{OH} = –5.0 mA	All	2.4	—	V
V_{OL}	Low Output Voltage	I_{OL} = 4.2 mA	All	—	0.4	V

(2) SUPPLY CURRENT

Symbol	Parameter	Test Condition	Variation	Min	Max	Unit
I_{CC1}	Average Supply Current	$\overline{RAS}$, $\overline{CAS}$, ADDRESS Cycling; t_{RC} = t_{RC} min; only one $\overline{RAS}$ active at any time	1M Bytes 4M Bytes 8M Bytes	— — —	550 600 1800	mA
I_{CC2}	Standby Current	I_{OUT} = 0 mA $\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	1M Bytes 4M Bytes 8M Bytes	— — —	25 25 40	mA
I_{CC3}	Average RAS Only Refresh Current	$\overline{RAS}$ = VIL; $\overline{CAS}$, Address Cycling; t_{RC} = t_{RC} min	1M Bytes 4M Bytes 8M Bytes	— — —	500 600 1800	mA
I_{CC4}	Average Supply Current, Page Mode	$\overline{RAS}$ = VIL; $\overline{CAS}$, Address Cycling; t_{PC} = t_{PC} min	1M Bytes 4M Bytes 8M Bytes	— — —	450 600 1800	mA
I_{CC5}	Standby Current	$\overline{RAS}$ = $\overline{CAS}$ = V_{CC} –0.2	1M Bytes 4M Bytes 8M Bytes	— — —	13 13 20	mA
I_{CC6}	CAS Before RAS Refresh Current	$\overline{RAS}$, $\overline{CAS}$, Cycling; t_{RC} = t_{RC} min	1M Bytes 4M Bytes 8M Bytes	— — —	500 600 1800	mA

AC OPERATING CHARACTERISTICS

(1) SWITCHING CHARACTERISTICS

Symbol	Parameter	Note	Variation	Min	Max	Unit
tRAC	Access Time from $\overline{RAS}$	1, 2	All	—	80	ns
tCAC	Access Time from $\overline{CAS}$	1, 2	All	—	27	ns
tAA	Access Time from Column Address	1, 2	All	—	47	ns
tCPA	Access Time from $\overline{CAS}$ Prechange	1, 2	All	—	52	ns
tCLZ	Output Buffer Low Impedance		All	0	—	ns
tOFF	Output Buffer Turnoff Time		All	0	27	ns

(2) TIMING REQUIREMENTS

Symbol	Parameter	Variation	Min	Max	Unit
tRC	Random Read or Write Cycle Time	All	160	—	ns
tRP	$\overline{RAS}$ Prechange Time	All	70	—	ns
tPC	Page Mode Cycle Time	All	57	—	ns
tCP	$\overline{CAS}$ Prechange Time	All	10	—	ns
tRAS	$\overline{RAS}$ Pulsewidth	All	80	10,000	ns
tRASP	$\overline{RAS}$ Pulsewidth (Page Mode)	All	80	100,000	ns
tCAS	$\overline{CAS}$ Pulsewidth	All	27	10,000	ns
tCRP	$\overline{CAS}$ to $\overline{RAS}$ Prechange Time	All	17	—	ns
tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	All	25	53	ns
tRAD	$\overline{RAS}$ to Column Address Delay Time	All	20	33	ns
tRAL	Column Address to $\overline{RAS}$ Lead Time	All	47	—	ns
tRSH	$\overline{RAS}$ Hold Time	All	27	—	ns
tCSH	$\overline{CAS}$ Hold Time	All	80	—	ns
tASR	Row Address Setup Time	All	7	—	ns
tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Prechange	All	52	—	ns
tASC	Address Setup Time	All	0	—	ns
tRAH	Row Address Hold Time	All	15	—	ns

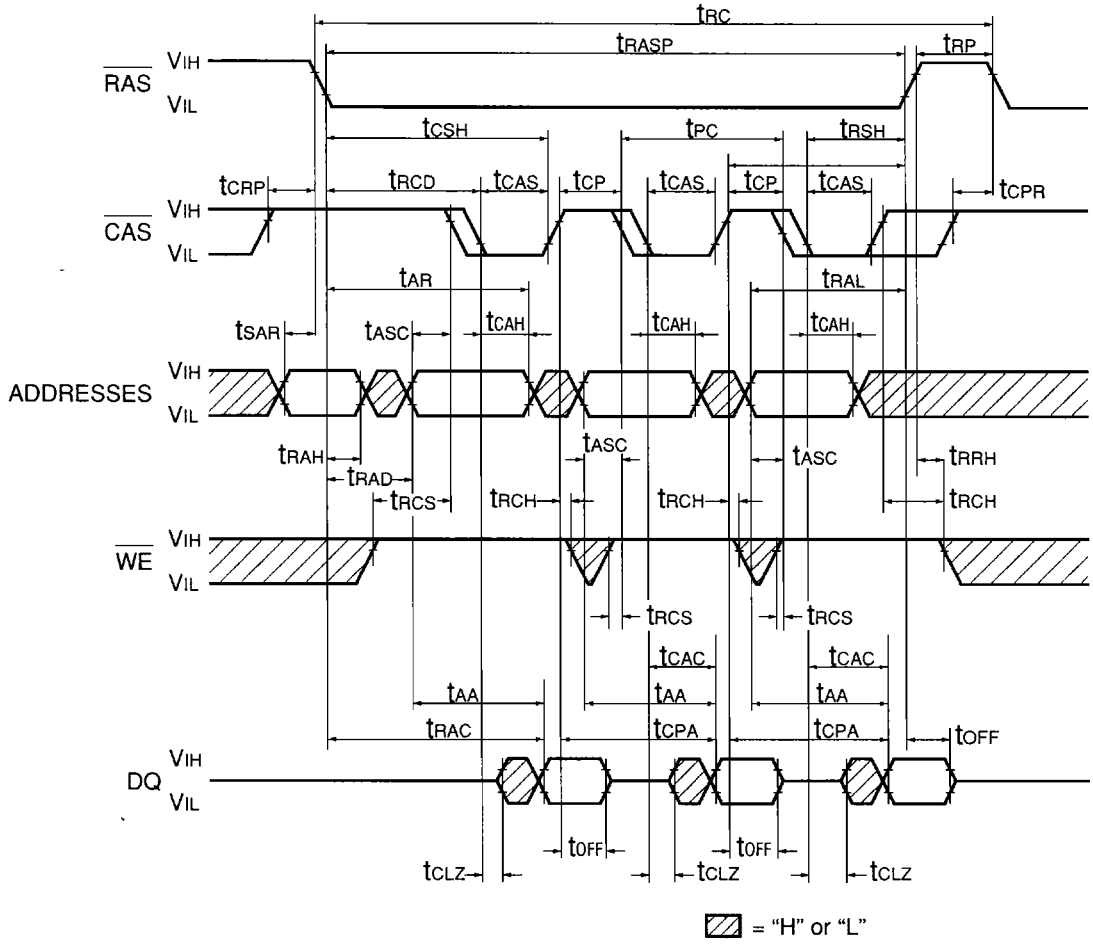
(2) TIMING REQUIREMENTS (Continued)

Symbol	Parameter	Variation	Min	Max	Unit
tCAH	Column Address Hold Time	All	18	—	ns
tAR	Column Address Hold Time from $\overline{RAS}$	All	60	—	ns
tT	Transition Time	All	3	50	ns
tRCS	Read Command Setup Time	All	0	—	ns
tRCH	Read Command Hold Time	All	0	—	ns
tRRH	Read Command Hold Time from $\overline{RAS}$ High	All	5	—	ns
tWCS	Write Command Setup Time	All	0	—	ns
tWCH	Write Command Hold Time	All	18	—	ns
tWCR	Write Command Hold Time from $\overline{RAS}$ Low	All	60	—	ns
tRWL	Write Command Setup Time to $\overline{RAS}$ High	All	27	—	ns
tCWL	Write Command Setup Time to $\overline{CAS}$ High	All	20	—	ns
tWP	Write Command Pulsewidth	All	15	—	ns
tDS	Data Setup Time	All	0	—	ns
tDH	Data Hold Time	All	22	—	ns
tDHR	Data Hold Time from $\overline{RAS}$	All	60	—	ns
tREF	Refresh Interval (512 Cycles) (1024 Cycles) (1024 Cycles)	1M Bytes 4M Bytes 8M Bytes	8 16 16	— — —	ns
tRPC	$\overline{RAS}$ to $\overline{CAS}$ Prechange Time	All	10	—	ns
tCSR	$\overline{CAS}$ Setup Time	All	17	—	ns
tCHR	$\overline{CAS}$ Hold Time	All	30	—	ns

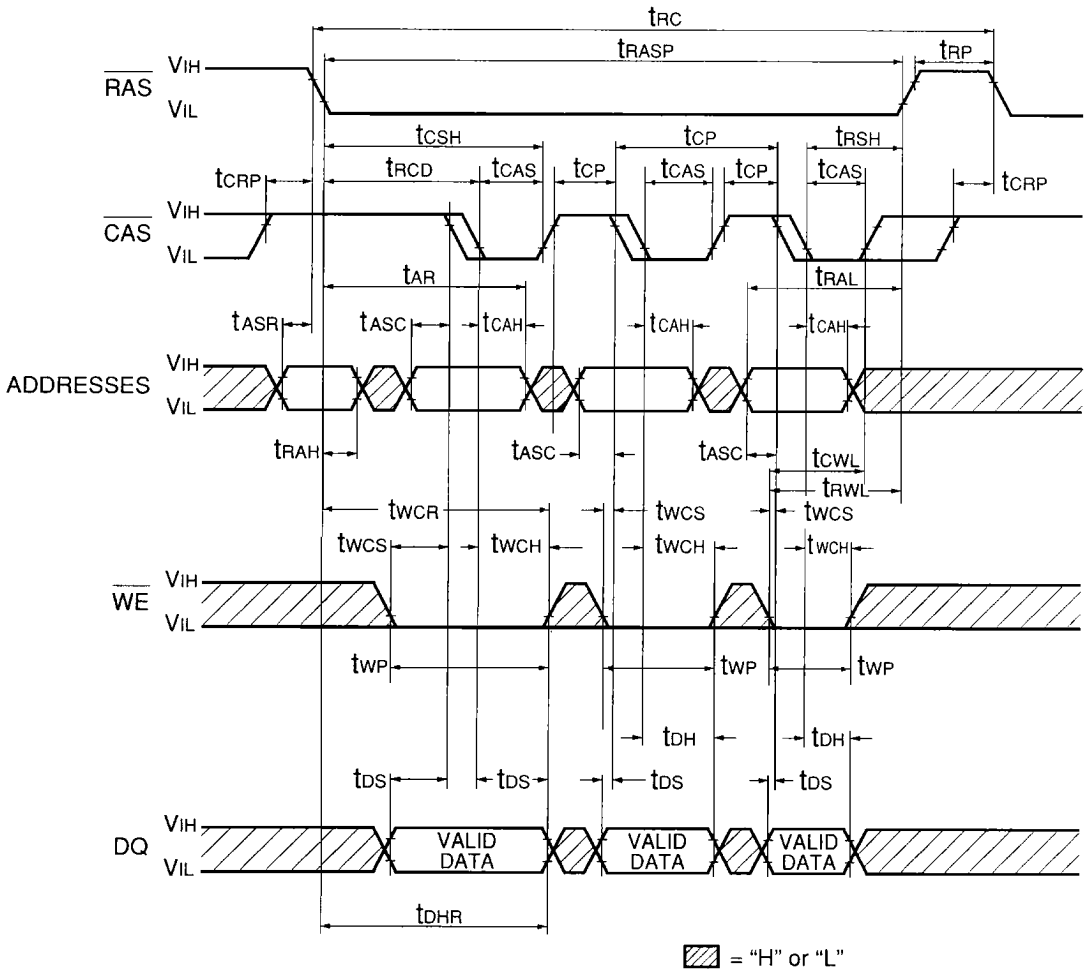
Notes:
1. Access Time is limited by all four parameters; tRAC, tCAC, tCPA, and tAA any single memory cycle, the actual access time is determined by whichever occurs last.
2. Output load equivalent to 2 TTL loads + 100 pF.
3. An initial pause at 200 uS is required after power-up followed by 8 refresh cycles before proper device operation is achieved. If the internal refresh counter is used, the cycles must be $\overline{CAS}$ before $\overline{RAS}$ refresh cycles.
4. Input pulse levels are from 0 to 3.0 volts. All timing measurements are referenced from VIL max and VIH min, with transition time tT = 5 nS.

WAVEFORMS

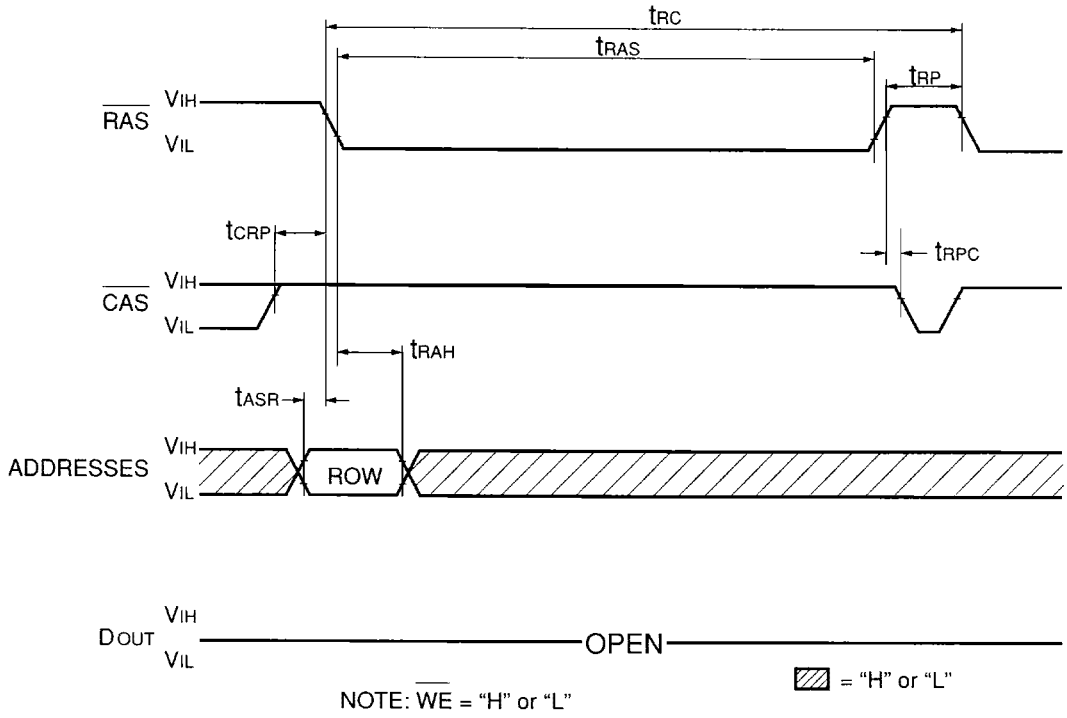
(1) FAST PAGE MODE READ CYCLE



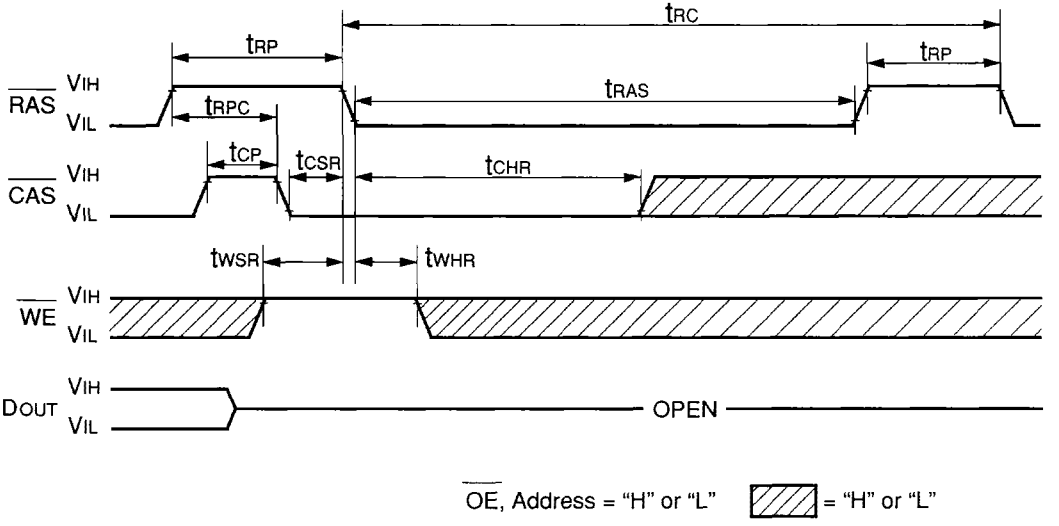
(2) FAST PAGE MODE WRITE CYCLE



(3) $\overline{RAS}$ ONLY REFRESH CYCLE



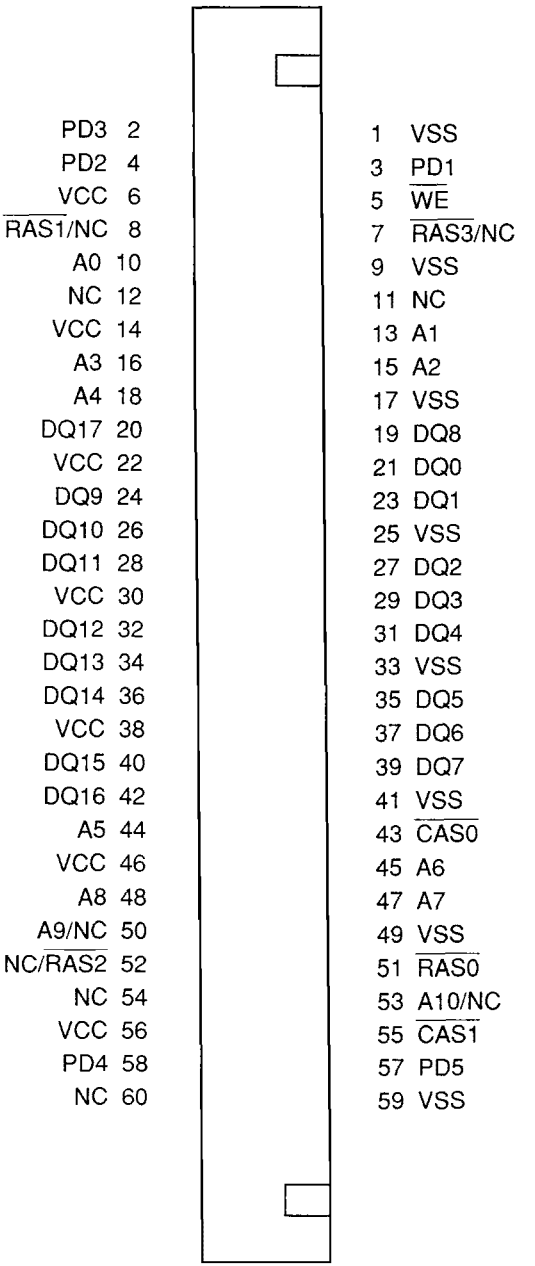
(4) $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



$\overline{OE}$, Address = "H" or "L" = "H" or "L"

PIN ASSIGNMENT

(1) PIN ASSIGNMENT



(2) VARIABLE ADDRESS AND RAS PINS

Variation	Pin Number				
	50	53	52	8	7
1M Bytes	NC	NC	$\overline{RAS2}$	NC	NC
4M Bytes	A9	NC	$\overline{RAS2}$	NC	NC
8M Bytes	A9	A10	NC	NC	NC

(3) PRESENCE DETECT PINS

Variation	(Configuration)			(Speed)	
	PD1	PD2	PD3	PD4	PD5
1M Bytes	Vss	NC	Vss	Vss	Vss
4M Bytes	NC	Vss	Vss	Vss	Vss
8M Bytes	NC	NC	Vss	Vss	Vss

Note: NC = No connect