Enhanced Memory Systems Inc.

168-pin Enhanced SDRAM DIMM
8/16/32 MB

Features

- JEDEC Standard 168-pin DIMMs
- PC-100 Spec Compliant - Lowest Latency
- Single 3.3V ± 0.3V Power Supply
- Unbuffered
- Fully Synchronous Operation
- Sustained Random Burst Reads (Same Bank Access)
  * 1-1-1-1 at 66MHz (CL=1)
  * 2-1-1-1-1 at 133MHz (CL=2)
- Programmable Burst Lengths — 1,2,4,8 or Full Page
- Early Auto-Precharge and Auto-/Refresh Modes
- 64ms, 2048-Cycle Refresh
- LVTTL Compatible Inputs and I/Os
- On-board Serial Presence-Detect (SPD) EEPROM with Write Protect Input

Part Numbers

Capacity	Part Number	Organization	# Physical Banks
8MB	SM1M64DT	1Mx64	1
8MB	SM1M72DT	1Mx72 ECC	1
16MB	SM2M64DT	2Mx64	1
16MB	SM2M72DT	2Mx72 ECC	1
32MB	SM4M64DT	4Mx64	2
32MB	SM4M72DT	4Mx72 ECC	2

Speed Grade

Speed Grade	Clock Frequency			Access Time		
	CL=1	CL=2	CL=3	CL=1	CL=2	CL=3
-7.5	66MHz	133MHz	133 Mhz	12ns	4.5ns	4.5ns
-10	50 MHz	100MHz	100MHz	15ns	5.0ns	5.0ns

Description

The Enhanced SDRAM (ESDRAM) DIMMs are low latency, high performance memory modules of 8, 16, and 32 MB capacities and are organized as x64 and x72 bits wide. The DIMMs are 100% pin, function, and timing compatible with the JEDEC standard 168-pin SDRAM DIMMs. The 8MB and 16MB DIMMs employ a single physical bank of memory while the 32MB DIMMs are built as two physical banks. Within each physical bank of memory are two logical banks of memory which are accessed through the use of BA0 (pin 122). All control, access, and data input signals are registered into each of the Enhanced SDRAM components with the use of an external clock, CK0-

Pin Assignment

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vdd	48	DU	90	Vdd	132	RFU
7	DQ4	49	Vdd	91	DQ36	133	Vdd
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2*	94	DQ39	136	CB6*
11	DQ8	53	CB3*	95	DQ40	137	CB7*
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vdd	101	DQ45	143	Vdd
18	Vdd	60	DQ20	102	Vdd	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0*	63	CKE1	105	CB4*	147	NC
22	CB1*	64	Vss	106	CB5*	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vdd	68	Vss	110	Vdd	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#	156	DQ59
31	DU	73	Vdd	115	RAS#	157	Vdd
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10/AP	80	NC	122	BA0	164	NC
39	RFU	81	WP	123	RFU	165	SA0
40	Vdd	82	SDA	124	Vdd	166	SA1
41	Vdd	83	SCL	125	CK1	167	SA2
42	CK0	84	Vdd	126	RFU	168	Vdd

*Used on x72 ECC DIMMs only.

CK3. The rising edge of the CK clock is used as the timing reference for all inputs and outputs.

ESDRAM DIMMs provide pipelined burst SRAM performance up to 66MHz and nearly the same at bus speeds up to 133MHz. The speed grade of a given DIMM has specifications defined to accommodate the DIMM operating at the rated module speed in a real system. Ne derating needs to be applied. That is, the -10ns DIMMs are specified to operate at 100MHz in CL=2 mode. The -7.5ns DIMMs will operate at 66MHz in CL=1 mode and up to 133MHz bus speed in CL=2 mode.

All standard SDRAM functionality and commands are supported with some enhancements available to boost memory system performance. The advanced features include 1) the ability to quickly close a read page by performing a READ/AP and 2) the ability to have four open pages through the use of the No Write Transfer mode.

Feature 1) Since the ESDRAM incorporates an SRAM row cache for each internal bank, a read page may be opened and loaded
(latched) into cache and the page quickly closed in preparation for another activate to the same bank. This is an inherent functional difference the ESDRAM DIMMs possess over standard SDRAM DIMMs. If it is not desired to quickly close read pages, a manual precharge (PRECH) may be performed at the end of the read cycle.

Feature 2) As an option the memory controller can maintain four open pages (a read and a write page per physical bank) for fast read/write cycles. If bit A9 is set = 1 during the Mode Register Set (MRS) command, the ESDRAM DIMM will not write data to the row cache during write cycles. Because the cache is not updated, read pages (two per physical bank) have been left open for fast read accesses (row hit) to subsequent READ commands.

A 2Kbit serial presence detect (SPD) EEPROM is mounted on all DIMMs and contains 256 bytes of information on the DIMM itself. The first 128 bytes are programmed by Enhanced Memory Systems to identify the module type and organization, component speed, and other attributes relevant to the system controller.

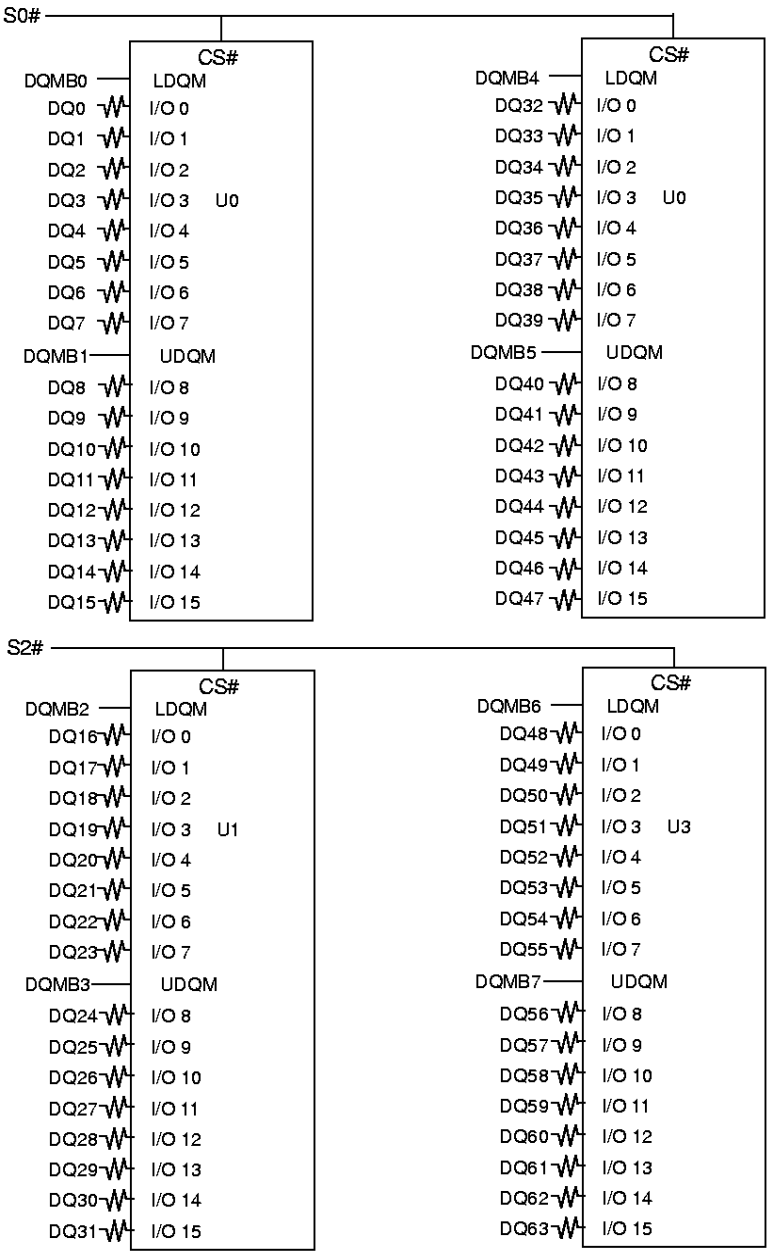
All ESDRAM DIMMs operate from a 3.3V power supply, and all inputs and outputs are LVTTL compatible.

See the ESDRAM component datasheet (16Mbit ESDRAM Datasheet) for more details on ESDRAM specifications and functional operation.

Serial Presence-Detect Operation

This module incorporates Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes is programmed by Enhanced to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide 8 unique DIMM/ EEPROM addresses.

Functional Block Diagram - 1Mx64 (8MB) - SM1M64DT

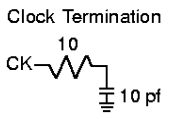


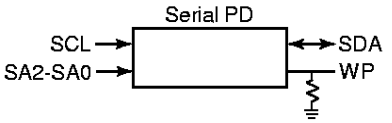
BA0 → A11(BS) ESDRAMs UO-U3
A0-A10 → A0-A10: ESDRAMs U0-U3
Vdd → ESDRAMs U0-U3
Vss → ESDRAMs U0-U3

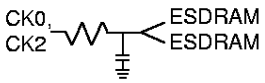
RAS# → RAS#: ESDRAMs U0-U3
CAS#: → CAS#: ESDRAMs U0-U3
WE# → WE#: ESDRAMs U0-U3
CKE0 → CKE: ESDRAMs U0-U3

Clock Wiring	
Clock Input	SDRAMs
CK0	2 ESDRAMs + 15pf
CK1	Termination
CK2	2 EDSRAMs + 15pf
CK3	Termination

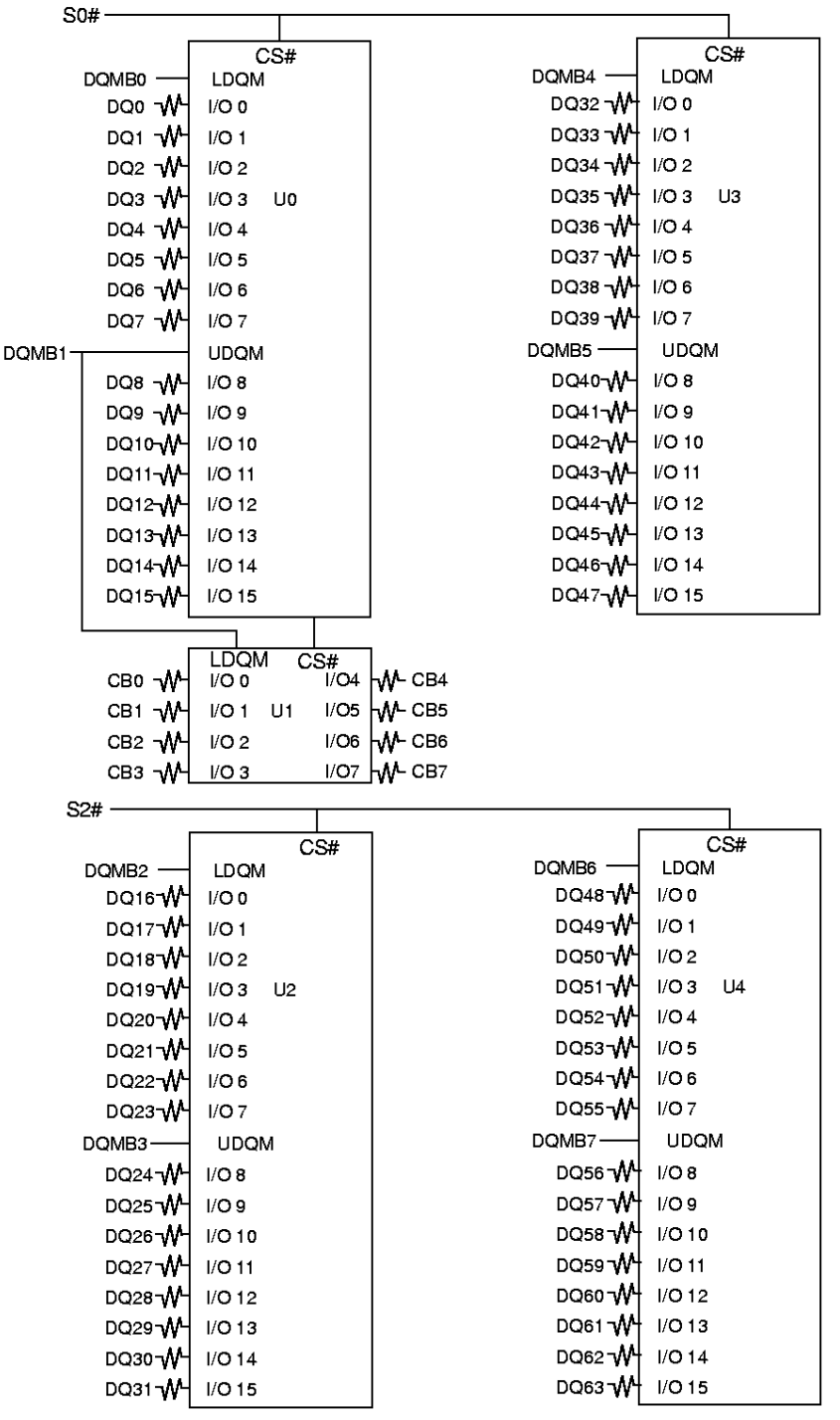
Note: All DQ resistor values are 10 Ohms.
All CK resistor values are 10 Ohms.
U0-U3 = SM2404T ESDRAMs.

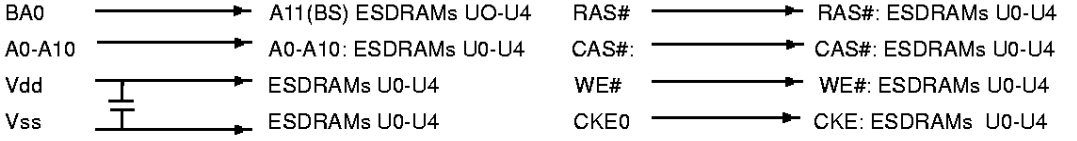






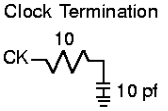
Functional Block Diagram - 1Mx72 (8MB)- SM1M72DT

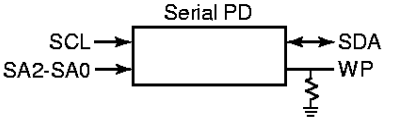


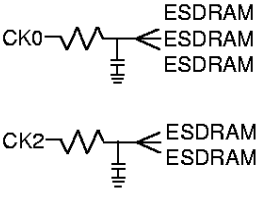


Clock Wiring	
Clock Input	SDRAMs
CK0	3 ESDRAMs + 10pf
CK1	Termination
CK2	2 EDSRAMs + 15pf
CK3	Termination

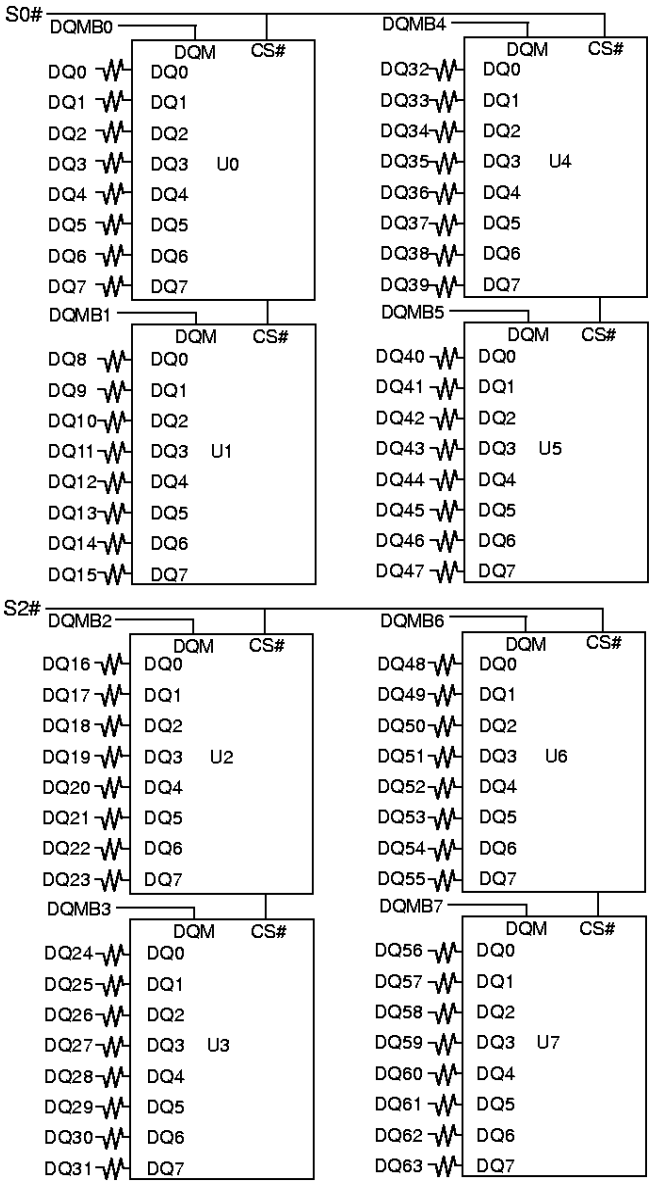
Note: All DQ resistor values are 10 Ohms.
All CK resistor values are 10 Ohms.
U0-U4 = SM2404T ESDRAMs.







Functional Block Diagram - 2Mx64 (16MB)- SM2M64DT

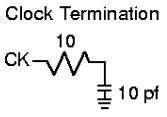


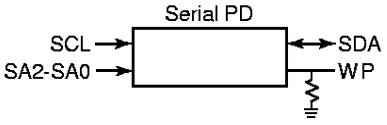
BA0 → A11(BS) ESDRAMs UO-U7
A0-A10 → A0-A10: ESDRAMs U0-U7
Vdd → ESDRAMs U0-U7
Vss → ESDRAMs U0-U7

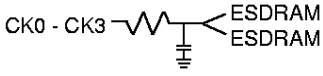
RAS# → RAS#: ESDRAMs U0-U7
CAS#: → CAS#: ESDRAMs U0-U7
WE# → WE#: ESDRAMs U0-U7
CKE0 → CKE: ESDRAMs U0-U7

Note: All DQ resistor values are 10 Ohms.
All CK resistor values are 10 Ohms.
U0-U7 = SM2403T ESDRAMs.

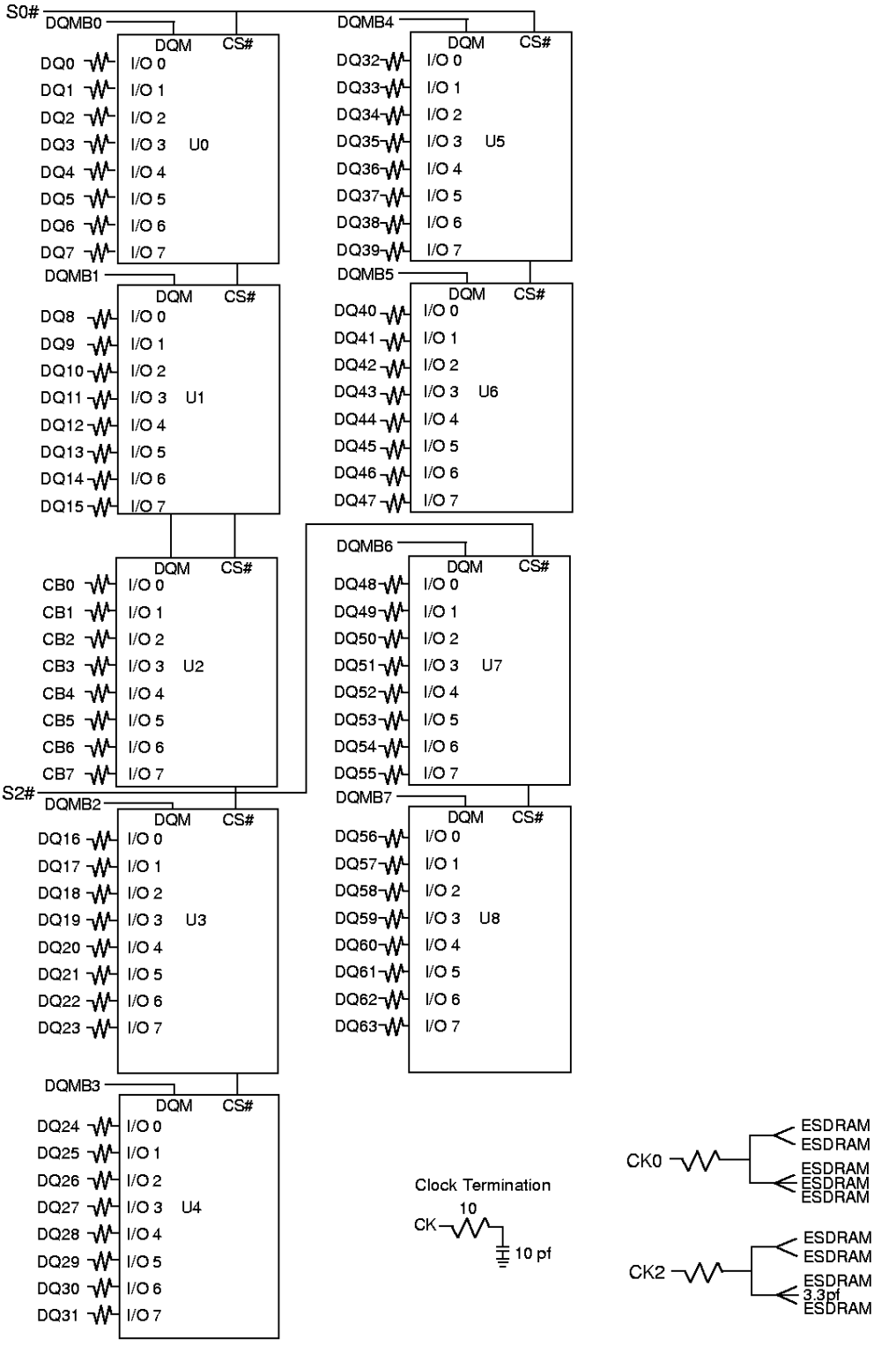
Clock Wiring	
Clock Input	SDRAMs
CK0	4 ESDRAMs + 3.3pf
CK1	Termination
CK2	4 EDSRAMs + 3.3pf
CK3	Termination







Functional Block Diagram - 2Mx72 ECC (16MB) - SM2M72DT



BA0 → A11(BS) ESDRAMs U0-U8

A0-A10 → A0-A10: ESDRAMs U0-U8

Vdd → ESDRAMs U0-U8

Vss → ESDRAMs U0-U8

RAS# → RAS#: ESDRAMs U0-U8

CAS#: → CAS#: ESDRAMs U0-U8

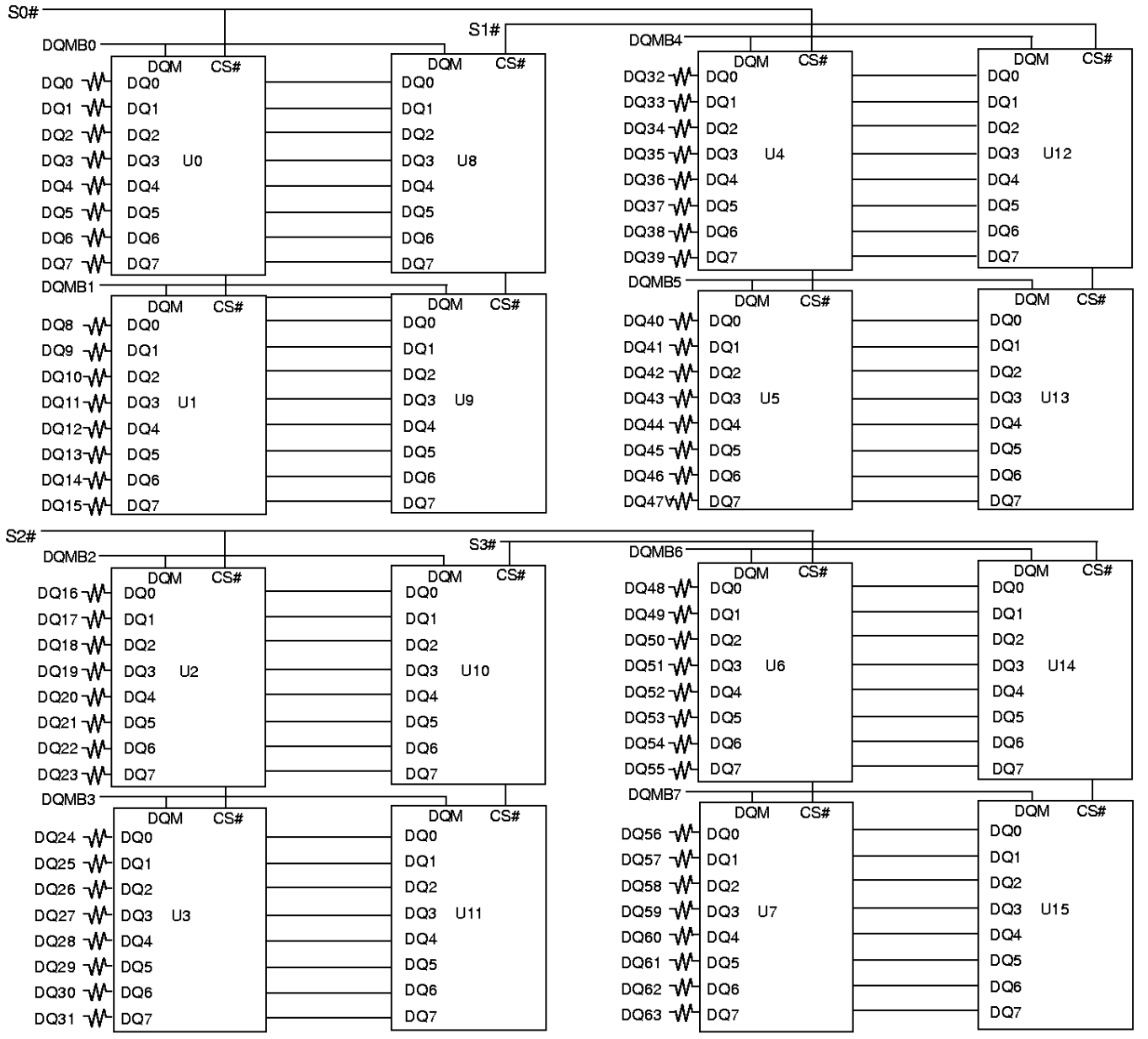
WE# → WE#: ESDRAMs U0-U8

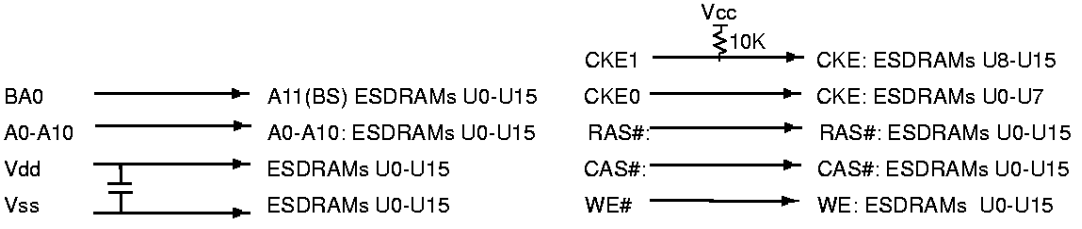
CKE0 → CKE: ESDRAMs U0-U8

Clock Wiring	
Clock Input	SDRAMs
CK0	5 ESDRAMs
CK1	Termination
CK2	4 EDSRAMs + 3.3pf
CK3	Termination

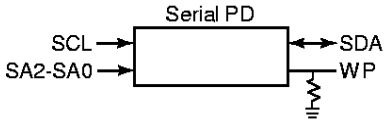
Note: All DQ resistor values are 10 Ohms.
All CK resistor values are 10 Ohms.
U0-U8 = SM2403T ESDRAMs.

Functional Block Diagram - 4Mx64 (32MB) - 2M4M64DT

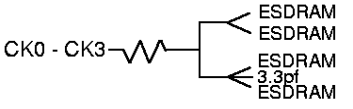




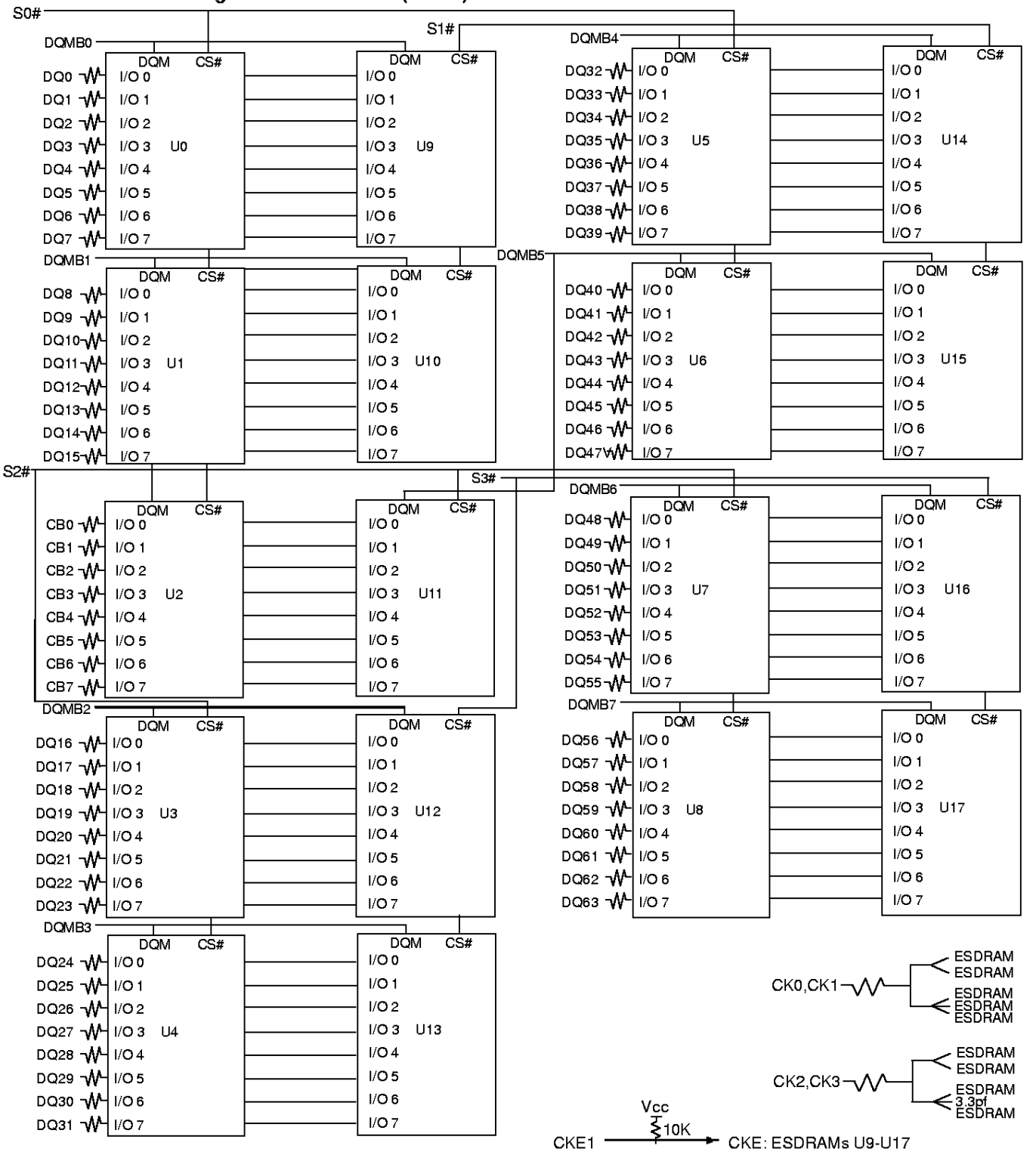
Note: All DQ resistor values are 10 Ohms.
All CK resistor values are 10 Ohms.
U0-U15 = SM2403T ESDRAMs.



Clock Wiring	
Clock Input	SDRAMs
CK0	4 ESDRAMs + 3.3pf
CK1	4 ESDRAMs + 3.3pf
CK2	4 EDSRAMs + 3.3pf
CK3	4 EDSRAMs + 3.3pf



Functional Block Diagram - 4Mx72 ECC (32MB) - SM4M72DT



Note: All DQ resistor values are 10 Ohms.
All CK resistor values are 10 Ohms.
U0-U17 = SM2403T ESDRAMs.

Clock Wiring	
Clock Input	SDRAMs
CK0	5 ESDRAMs
CK1	5 ESDRAMs
CK2	4 EDSRAMs + 3.3pf
CK3	4 EDSRAMs + 3.3pf

Pin Description

Symbol	Type	Description
RAS#, CAS#, WE#	Input	Command Inputs: Sampled at the rising edge of CK, RAS#, CAS#, and WE# (along with SO#-S3#) define the command to be executed.
CKO-CK3	Input	Clock: CK0-CK3 are driven by the system clock. All ESDRAM input signals are sampled on the positive edge of CK.
CKE0, CKE1	Input	Clock Enable: CKE0-CKE1 activate (HIGH) and deactivate (LOW) the CK0-3 signals. Deactivating the clock provides Power-Down and Self Refresh operation (all banks idle), or Clock Suspend operation. CKE0-CKE1 are synchronous except after the device enters Power-Down and Self Refresh modes, where CKEO-CKE1 become asynchronous until after exiting these modes.
SO#, S2# S1#, S3#	Input	Chip Select: SO#-S3# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are ignored when the appropriate S# is registered HIGH. SO#-S3# are considered part of the command code.
DQMB0-DQMB7	Input	Data I/O Mask: DQMB inputs an input mask signal for write accesses and an output enable singal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during READ cycles.
BA0	Input	Bank Address: BA0 defines to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 is also used to program the A11 bit of the MODE REGISTER.
A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A10 with A10 defining Auto Precharge) to select one location out of the 1 Meg available in the respective bank. A10 is sampled during a precharge command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
CB0-CB7	Input/Output	ECC check bits.
DQ0-DQ63	Input/Output	Data I/O: Data bus.
Vdd	Supply	Power Supply: +3.3V ± 0.3V
Vss	Supply	Ground
SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
WP	Input	Serial Presence - Detect Write Protect : Active high inhibits writes to the SPD EEPROM. WP must be driven low for normal read/write operations.
RFU	-	Reserved for Future Use: These pins should be left unconnected.
DU	-	Do not use.
NC	-	No connect - open pin.

Capacitance

Parameter/Condition	Symbol	8MB		16MB		32MB		UNITS	NOTES
		x64	x72	x64	x72	x64	x72		
A0-A10,BA0,RAS#,CAS#,WE#	C_{in1}	32	35	47	52	80	87	pF	
S0#, S2#	C_{in2}	20	20	28	32	28	32	pF	
CK0,CK3	C_{in3}	28	32	28	32	28	32	pF	
CKE0, CKE1	C_{in4}	28	32	45	48	45	48	pF	
DQMB0 - DQMB7	C_{in5}	14	14	14	14	18	18	pF	
SCL,SA0-SA2	C_{in6}	14	14	14	14	14	14	pF	
SDA	$C_{I/O1}$	15	15	15	15	15	15	pF	
DQ0-DQ63, CB0-CB7	$C_{I/O2}$	15	15	15	15	20	20	pF	

DC Electrical Characteristics and Operating Conditions

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{DD}	3.0	3.6	V	
Input High (Logic1) Voltage, all inputs		V_{IH}	2.0	Vcc + 0.3	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-0.3	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ Vin ≤ Vcc	CK0-CK3, S0# - S3#	I_{in1}	—	±10	µA	
(All other pins not under test = 0V)	CKE0-1	I_{in2}	—	±15	µA	
	RAS#, CAS#, A0-A10, BA0, WE#	I_{in3}	—	±20	µA	
OUTPUT LEAKAGE CURRENT (DQs ARE DISABLED; OV≤ Vout≤ Vcc)	DQ0-DQ63,CB0-CB7 DQMB0-7,SCL,SA0-2, SDA	I_0 I_{in4}	— —	±5 ±10	µA µA	
OUTPUT LEVELS Output High Voltage (Iout = -2mA)		V_{OH}	2.4	—	V	
Output Low Voltage (Iout = -2mA)		V_{OH}	—	0.4	V	

AC Functional Characteristics (-7.5 Speed Grade)

Symbol	Parameter	Clock Frequency (MHz)				Units
		66	83	100	133	
t_{CK}	Clock Cycle Time	15	12	10	8	ns
t_{AA}	/CAS Latency	1	2	2	2	t_{CK}
t_{RCD}	/RAS to /CAS Delay	1	2	2	2	t_{CK}
t_{RL}	/RAS Latency	2	4	4	4	t_{CK}
t_{RC}	Bank Cycle Time	3	5	5	5	t_{CK}
t_{RAS}	Minimum Bank Active Time	2	3	3	3	t_{CK}
t_{RP}	Precharge Time	1	2	2	2	t_{CK}
t_{DPL}	Data In to Precharge	1	1	1	1	t_{CK}
t_{DAL}	Data In to Active/Refresh	2	3	3	3	t_{CK}
t_{RRD}	Bank to Bank Delay Time	1	1	2	2	t_{CK}
t_{CCD}	/CAS to /CAS Delay Time	1	1	1	1	t_{CK}

Absolute Maximum Ratings*

Description	Rating
Voltage on Vdd Supply Relative to Vss	-1V to +4.6V
Voltage on Inputs, NC, or I/0 Pins Relative to Vss	-1V to +4.6V
Operating Temperature, T_A (Ambient)	0°C to +70°C
Storage Temperature (Plastic)	-55°C to +125°C
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended may affect reliability.

ESDRAM Component AC Characteristics

			-7.5		-10			
PARAMETER	CAS Latency	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (positive edge)	3	t_{AC3}		4.5		5	ns	
	2	t_{AC2}		4.5		5	ns	
	1	t_{AC1}		12		15	ns	
Address setup time		t_{AS}	2		2.5		ns	
Address hold time		t_{AH}	1		1		ns	
CLK high level width		t_{CH}	3		3.5		ns	
CLK low level width		t_{CL}	3		3.5		ns	
Clock time cycle	3	t_{CK}	7.5		10		ns	
	2	t_{CK}	7.5		10		ns	
	1	t_{CK}	15		20		ns	
CKE setup time		t_{CKS}	2		2.5		ns	
CKE hold time		t_{CKH}	1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		t_{CMS}	2		2.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		t_{CMH}	1		1		ns	
Data-in setup time		t_{DS}	2		2.5		ns	
Data-in hold time		t_{DH}	1		1		ns	
Data-out high-impedance time		t_{HZ}		4.5		5	ns	
Data-out low-impedance time		t_{LZ}	0		0		ns	
Data-out hold time		t_{0H}	2		2.5		ns	
ACTIVE to PRECHARGE command period		t_{RAS}	22.5	120K	30	120K	ns	
ACTIVE to ACTIVE command period		t_{RC}	37.5	120K	50	120K	ns	
ACTIVE to READ or WRITE delay		t_{RCD}	15		20		ns	
Refresh period (2048 cycles)		t_{REF}		64		64	ms	
PRECHARGE command period		t_{RP}	15		20		ns	
ACTIVE to ACTIVE alternate bank command period		t_{RRD}	15		20		ns	
Transition time		t_T		4		4	ns	
Exit SELF REFRESH to ACTIVE command		t_{XSR}	96		100		ns	

*Specifications for the ESDRAM components used on the module.

Serial Presence Detect (SPD) Table

Byte #	Description		SPD Entry 8MB 1Mx16 (4)	SPD Entry 16MB 2Mx8 (8)	SPD Entry 32MB 2 x 2Mx8 (8)	Hex Code 8MB 1Mx16 (4)	Hex Code 16MB 2Mx8 (8)	Hex Code 32MB 2 x 2Mx8 (8)
0	Number of bytes written into EEPROM		128	128	128	80	80	80
1	Total number of SPD bytes		256	256	256	08	08	08
2	Memory Type		SDRAM	SDRAM	SDRAM	04	04	04
3	Number of Row Addresses		11	11	11	0B	0B	0B
4	Number of Column Addresses		8	9	9	08	09	09
5	Number of Module Banks		1	1	2	01	01	02
6	Module Data Width		x64 x72	x64 x72	x64 x72	40 48	40 48	40 48
7	Module Data Width (cont'd)		0 0	0 0	0 0	0 0	0 0	0 0
8	Voltage Interface Levels		LVTTL	LVTTL	LVTTL	01	01	01
9	Cycle Time at Max CAS Latency	-7.5 -10	7.5 ns 10.0 ns	7.5 ns 10.0 ns	7.5 ns 10.0 ns	75 A0	75 A0	75 A0
10	ESDRAM Clock Access Time	-7.5 -10	4.5 ns 5.0 ns	4.5 ns 5.0 ns	4.5 ns 5.0 ns	45 50	45 50	45 50
11	DIMM config. (non-parity, parity, ECC)	x64 x72	--- Non-parity --- --- ECC---			00 02	00 02	00 02
12	Refresh Rate and Type		--- 31.25us/Self ---			83	83	83
13	Primary ESDRAM Width		x16	x8	x8	10	08	08
14	Error Checking Data Width	x64 x72	N/A x8	N/A x8	N/A x8	00 10	00 08	00 08
15	Min. CAS-to-CAS Delay (tCCD)		1 clk	1 clk	1 clk	01	01	01
16	Burst Lengths Supported		--- 1, 2, 4, 8, Full Pg. ---			8F	8F	8F
17	Number of Banks on ESDRAM Device		2	2	2	02	02	02
18	CAS Latencies Supported		1,2,3	1,2,3	1,2,3	07	07	07
19	CS Latency		0	0	0	01	01	01
20	Write Latency		0	0	0	01	01	01
21	ESDRAM Module Attributes		---- Unbuffered ---			00	00	00
22	ESDRAM Device Attributes	Early RAS Precharge, +/-10% Vdd, Precharge All				07	07	07
23	Min. Clock Cycle Time at CL=2	-7.5 -10	7.5 ns 10.0 ns	7.5 ns 10.0 ns	7.5 ns 10.0 ns	75 A0	75 A0	75 A0
24	Clock Access Time at CL=2 (tAC2)	-7.5 -10	4.5 ns 5.0 ns	4.5 ns 5.0 ns	4.5 ns 5.0 ns	45 50	45 50	45 50
25	Min. Clock Cycle Time at CL=1	-7.5 -10	15.0 ns 20.0 ns	15.0 ns 20.0 ns	15.0 ns 20.0 ns	3C 50	3C 50	3C 50
26	Clock Access Time at CL=1 (tAC1)	-7.5 -10	12.0 ns 10.0 ns	12.0 ns 10.0 ns	12.0 ns 10.0 ns	30 3C	30 3C	30 3C
27	Min. Row Precharge Time (tRP)	-7.5 -10	15 ns 20 ns	15 ns 20 ns	15 ns 20 ns	0F 14	0F 14	0F 14
28	Min. Row-to-Row Delay (tRRD)	-7.5 -10	15 ns 20 ns	15 ns 20 ns	15 ns 20 ns	0F 14	0F 14	0F 14
29	Min. RAS-to-CAS Delay (tRCD)	-7.5 -10	15 ns 20 ns	15 ns 20 ns	15 ns 20 ns	0F 14	0F 14	0F 14
30	Min. RAS Pulse Width (tRAS)	-7.5 -10	23 ns 30 ns	23 ns 30 ns	23 ns 30 ns	17 1E	17 1E	17 1E
31	Module Bank Density		8MB	16MB	32MB	02	04	08
32-59	Reserved							
60	ESDRAM Attributes		See Appendix H			03	03	03
61	ESDRAM Superset Information		See Appendix B			01	01	01

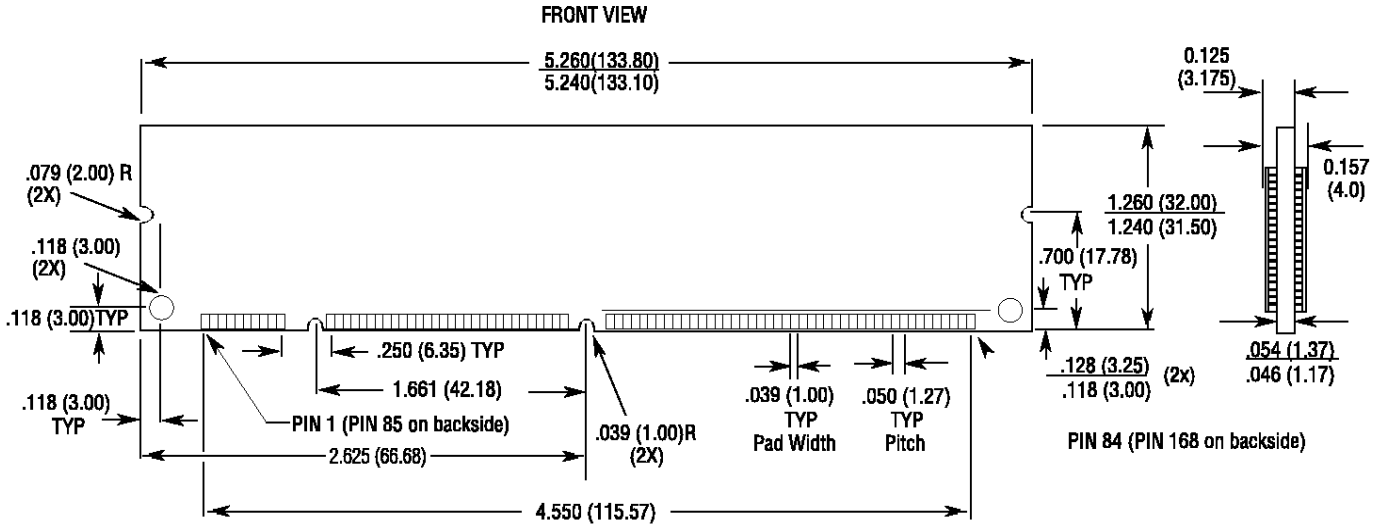
Appendix B - Superset Technology

Device	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
ESDRAM	0	0	0	0	0	0	0	1

Appendix H - ESDRAM Attributes

Device	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	Supports CL=1mode	No Write Transfer mode
ESDRAM	0	0	0	0	0	0	0 or 1	0 or1

168-PIN DIMM



Dimensions: inches (mm)