# STARTECH

# ST78C36

Printed September 8, 1994

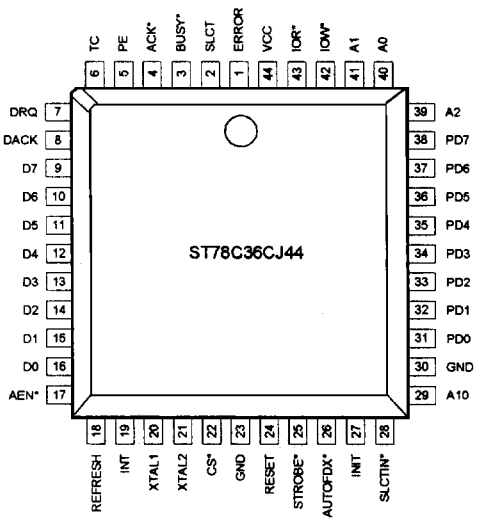
## ECP/EPP PARALLEL PRINTER PORT WITH 16 BYTE FIFO

## DESCRIPTION

The ST78C36 is a monolithic Bidirectional ECP/EPP Parallel port designed to operate as a general purpose I/O port. It contains all the necessary input/output signals to be configured as a CENTRONICS printer port, MicroSoft/HP ECP, IBM EPP smart printer port. The ST78C36 is a general purpose input/output controller with 16 byte internal FIFO. FIFO operation can be enabled or disabled. For CENTRONICS printer operation, all registers are mapped to IBM printer port registers.

The ST78C36 is designed to operate as normal printer interface without any additional settings.

**PLCC Package**




## FEATURES

- 16 bytes of printer output FIFO
- Bi-directional parallel port
- Bi-directional I/O ports
- Register compatible to IBM XT, AT, compatible 386, 486
- MicroSoft ECP compatible.

## ORDERING INFORMATION

| Part number | Package | Operating temperature |
|---|---|---|
| ST78C36CJ44 | PLCC | 0° C to + 70° C |
| ST78C36IJ44 | PLCC | -40° C to + 85° C |
| ST78C36CQ48 | TQFP | 0° C to + 70° C |

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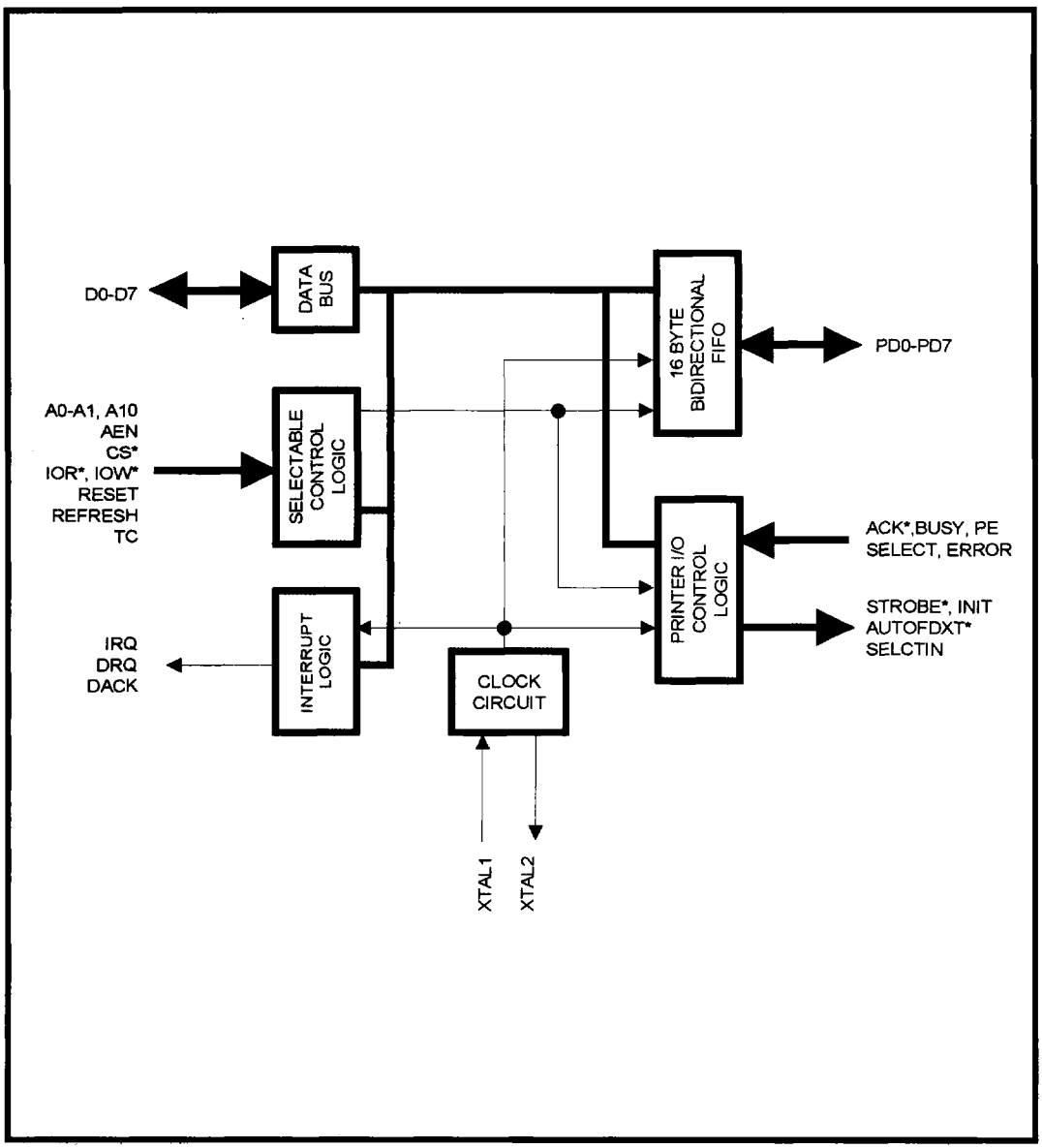
## BLOCK DIAGRAM



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| Symbol | Pin | Signal Type | Pin Description |
|---|---|---|---|
| ERROR* | 1* | I | General purpose input or line printer error (active low). This is an output from the printer to indicate an error by holding it low during error condition. |
| SLECET | 2* | I | General purpose input or line printer selected (active high). This is an output from the printer to indicate that the line printer has been selected. |
| BUSY* | 3* | I | General purpose input or line printer busy (active low). An output from the printer to indicate printer is not ready to accept data. |
| ACK* | 4* | I | General purpose input or line printer acknowledge (active low). This input is pulsed low by the printer to indicate that data has been accepted successfully. |
| PE | 5* | I | General purpose input or line printer paper empty (active high). An output from the printer to indicate out of paper. |
| TC | 6 | I | Terminal Count (active high). This signal indicates to ST78C36 that data transfer is complete. If DMA operation mode is selected for command execution, TC will be qualified by DACK*, but not in the programmed I/O execution. |
| DRQ | 7 | O | Direct Memory Access Request (three state, active high). DMA request for byte transfers of data. |
| DACK* | 8 | I | DMA ACKNOWLEDGE (active low). Used by DMA controller to transfer data from the ST78C36 onto the bus. |
| D7-D0 | 9-16 | I/O | Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus. |
| AEN* | 17 | I | Host address enable (active low). All decoded addresses are valid when AEN* is low. |
| REFRESH | 18 | I | Referesh cycle. |
| IRQ | 19 | O | Printer interrupt output (active low). To signal the state of the printer port. This pin tracks the ACK* input pin, When ACK* is low IRQ is low and when ACK* is high IRQ is high |
| XTAL1 | 20 | I | Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal |

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| Symbol | Pin | Signal Type | Pin Description |
|---|---|---|---|
| | | | oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates. |
| XTAL2 | 21 | I | Crystal input 2 or buffered clock output. See XTAL1. |
| CS* | 22 | I | Parallel printer port chip select (active low). A low at this pin enables the parallel port / CPU data transfer operation. |
| RESET | 24 | I | Master reset. (active high) A high on this pin will reset all the outputs and internal registers. |
| STROBE* | 25* | I/O | General purpose I/O or data strobe output (open drain active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7). |
| AUTOFDXT* | 26* | I/O | General purpose I/O or automatic line feed (open drain active low). When this signal is low the printer should automatically line feed after each line is printed. |
| INIT | 27* | I/O | General purpose I/O or initialize line printer (open drain active low). When this signal is low, it causes the printer to be initialized. |
| SLCTIN* | 28* | I/O | General purpose I/O or line printer select (open drain active low). When this signal is low, it selects the printer. |
| A10 | 29 | I | Address select line. To select internal registers. |
| PD0-PD7 | 31-38 | I/O | Bi-directional parallel ports (three state). To transfer data in or out of the ST78C36 parallel port. PD7-PD0 are latched during output mode. |
| A0-A2 | 39-41 | I | Address select lines. To select internal registers. |
| IOW* | 42 | I | Write strobe (active low). A low on this pin will transfer the contents of the CPU data bus to the addressed register. |
| IOR* | 43 | I | Read strobe (active low). A low level on this pin transfers the contents of the ST78C36 data bus to the CPU. |
| GND | 23,30 | O | Signal and power ground. |
| VCC | 44 | I | Power supply input. |

* Have internal pull-up resistor on inputs

## INTRODUCTION

This parallel interface is designed to provide all of the signals and registers needed to communicate through a standard parallel printer port as found in the IBM PC, AT, PS/2 and Centronics systems. The address decoding of the registers utilizing A0, A1 and A10 is shown in Table 1. All bits in these registers are located in the same positions and have the same functions as the registers of the systems listed above.

| NAME | ADDRESS | R/W | SIZE | MODE | FUNCTION |
|---|---|---|---|---|---|
| DATA | Port+0 Hex | R/W | byte | 000 | Data Register |
| DATA | Port+0 Hex | R/W | byte | 001 | Data Register |
| AFIFO | Port+0 Hex | R/W | byte | 011 | ECP FIFO |
| STR | Port+1 Hex | R | byte | ALL | Status Register |
| CTR | Port+2 Hex | R/W | byte | ALL | Control Register |
| CFIFO | 400 Hex | R/W | PWord | 010 | Parallel Port Data FIFO |
| DFIFO | 400 Hex | R/W | PWord | 011 | ECP FIFO |
| TFIFO | 400 Hex | R/W | PWord | 110 | Test FIFO |
| CNFGA | 400 Hex | R/W | byte | 111 | Configuration Register A |
| CNFGB | 401 Hex | R/W | byte | 111 | Configuration Register B |
| ECR | 402 Hex | R/W | byte | ALL | Extended Control Register |

## REGISTER DEFINITIONS

### DATA REGISTER (Mode 000, 001)

This is a bi-directional data port that transfers 8-bit data to or from PD7-0. The CTR-5 bit will determine the data direction in conjunction with the Read and Write strobes.

### AFIFO (Mode 011)

ECP Add FIFO register. Write only. In the forward direction a byte written into this register is pushed into the FIFO and tagged as a ECP Address / RLE command. Reading this register has no effect and the data read is undefined. Writes to this register during backward direction have no effect and the data is ignored.

**Bit-7:**

1 = AFIFO bits 0-6 are ECP address.

0 = AFIFO bits 0-6 is a run length (RLE), indicating how many times the next data byte is to appear.

000000 = 1 time.
000001 = 2 time.
000010 = 3 time.
and so on.

**Bit 0-6:**

Address or RLE fields.

### STATUS REGISTER

This register provides status for the signals listed below. It a read only register. Writing to it is an invalid operation that has no effect.

**Bit-0:**

When in EPP mode, this is the time-out status bit. When this bit is "1", time-out occurred on EPP cycle (min. 10μs). It is cleared to "0" after STR is read. Consecutive reads(after the first read) always return "0". It is also cleared to "0" when EPP is enabled. When not in EPP mode, this bit is "1".

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**Bit-1:**
Reserved, this bit is always "1".

**Bit-2:**
In the compatible mode, or in ECP and EPP mode with bit-4 of PCR = 0, this bit is always "1". In the Extended Mode (PTR-7 bit is "1"), or in ECP and EPP with bit-4 of PCR = 1 this bit is the status bit. In the Extended mode, If CTR-4 = 1 , then this bit is latched low when the ACK* signal makes a transition from low to high. Reading this bit sets it to a "1".

**Bit-3:**
This bit represents the current state of the printer error signal. The printer sets this bit low when there is a printer error. This bit follows the state of the error pin.

**Bit-4:**
This bit represents the current state of the printer select signal (SLCT). The printer sets this bit high when it is selected. This bit follows the state of the SLCT pin.

**Bit-5:**
This bit represents the current state of the printer paper end signal (PE). The printer sets this bit high when it detects the end of the paper. This bit follows the state of the PE pin.

**Bit-6:**
This bit represents the current state of the printer acknowledge signal (ACK*). The printer pulses this signal low after it has received a character and is ready to receive another one. This bit follows the state of the ACK* pin.

**Bit-7**
:This bit represents the current state of the printer BUSY* signal. The printer sets this bit low when it is BUSY* and cannot accept another Characters. This bit is the inverse of the (BUSY*) pin.

**CONTROL REGISTER**
This register provides all output signals to control the printer. Except for bit-5, it is a read and write register. Normally when the Control Register is read, the bit values are provided by the internal output data latch. These bit values can be superseded by the logic level of the STROBE*, AFD*, INIT, and SLIN* pins, if These pins are forced high or low by an external voltage. In order to force these pins high or low the corresponding bits should be set to their Inactive state.

**Bit-0:**
This bit directly controls the data STROBE* signal to the printer via the STROBE* pin. This bit is the inverse of the pin.

**Bit-1:**
This bit directly control the automatic feed XT signal to the printer the AFD* pin. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the AFD* pin.

**Bit-2:**
This bit directly controls the signal to initialize the printer via the INIT pin. Setting this bit to low initializes the printer. This bit follows the INIT signal pin.

**Bit-3:**
This bit directly controls the select in signal to the printer via the SLIN* pin. Setting this bit high selects the printer. It is the inverse of the SLIN* pin.

**Bit-4:**
This bit enables the parallel port interrupt. Setting this bit low puts IRQ into THREE-STATE and clears any pending interrupts. In the AT Compatible Mode, or in EPP or ECP modes when this bit is set high, the IRQ signal follows the ACK* signal transitions (pulse interrupt). In the Extended Mode, or in either EPP or ECP modes when this bit is set high, The IRQ signal should set high on the low to high transition of the ACK* signal.

**Bit-5:**
This bit determines the parallel port direction. The default condition results in the parallel pin being in the output mode. This is a Read/Write bit in EPP mode. In compatible mode it is a write only bit; a read from it will return "1".

**Bits 6-7:**
Reserved. These bits are always.

**CFIFO (Mode 010)**
Parallel Port FIFO Register. Write only. A byte written, or DMA-ed, to this registers pushed into The FIFO and tagged as data. Reading this register has no effect and the data read is undefined.

**DFIFO (Mode 011)**
ECP Data FIFO Register. In the forward direction a byte written, or DMA-ed, to this register is pushed into the FIFO and tagged as data. Reading this register has no effect and the data read is undefined. In the backward direction the ECP automatically issues ECP read cycles to fill the FIFO. Reading this register pops a byte from the FIFO. Writing this register has no effect and the data written is ignored.

**TFIFO (Mode110)**
Test FIFO Register. A byte written into this register is pushed into the FIFO. A byte read from this register is popped from the FIFO The ECP does not issue a ECP cycle to transfer the data to or from the peripheral device. The TFIFO is readable and writ able in both directions. In the forward direction PD7-0 is driven, but the data is undefined. The FIFO does not stall when overwritten or under-run (access is ignored). Bytes are always read from the top of the FIFO, regardless of the direction bit.

**CNFGA(Mode 111)**
Configuration Register A. Read only. Reading this register always returns 10Hex. Writing this register has no effect and the data is ignored.

**CNFGB (Mode111)**
Configuration Register B. Read only. Reading this register returns the configuration parallel port interrupt line, and its state.

**ECR**
Extended Control Register. This register controls the ECP and parallel port functions. Upon reset this register is Initialized to 16Hex.

**Bit 5-7:**
**Mode 000:**
Standard mode. Write cycles are performed under software control. Bit-5 of CTR is forced to "0" and PD7-0 is driven. The FIFO is reset (empty).

**Mode 001:**
PS/2 mode. Read and write cycles are performed under software control. The FIFO is reset.

**Mode 010:**
Parallel Port FIFO mode. Write cycles are performed under hardware control (STROBE* is controlled by hardware). Bit-5 of CTR is forced to "0" and PD7-0 are driven.

**Mode 011:**
ECP FIFO mode. The FIFO direction is controlled by bit-5 of CTR. Read and write cycle to the device are performed under hardware control (STROBE* and AFD* are controlled by hardware).

**Mode 100:**
Reserved.

**Mode 101:**
Reserved.

**Mode 110:**
FIFO test mode. The FIFO is accessible via the TFIFD register. The ECP does not issue ECP cycles to fill/empty the FIFO.

**Mode 111:**
Configuration mode. The CNFGA and CNFGB registers are accessible in this mode.

**Bit-4:**
ECP Interrupt Mask bit. When this bit is "0" an interrupt is generated on ERROR assertion. An interrupt is also generated when ERROR is asserted while this bit is changed from "1" to "0"; this prevents the loss of an interrupt between ECR read and ECR write. When this bit is "1", no interrupt is generated.

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**Bit-3:**
ECP DMA Enable bit. When this bit is "0", DMA is disabled and the PDRQ pin is in TRI-STATE. When this bit is "1" , DMA is enabled and DMA starts when bit-2 of ECR is "0".

**Bit-2:**
ECP Service bit. When this bit is "0", and one of the following three interrupt events occur, an interrupt is generated and this bit is set to "1" by hardware.

a. Bit-9 of ECR is "1", and terminal count is reached during DMA.
b. Bit-3 of ECR is "0" and bit-5 of CTR is "0", and there are eight or more bytes free in the FIFO.
c. Bit-3 of ECR is "0" and bit-5 of CTR is "1", and there are eight or more bytes to be read from the FIFO. When this bit is "1", DMA and the above three interrupts are disabled. Writing "1" to this bit does not cause an interrupt. When the ECP clock is stopped this bit is read as "0", regardless of its actual value.

**Bit-1:**
FIFO Full bit. Read only. This bit is "0" when the FIFO has at least one free byte. This bit is "1" when the FIFO is full. This bit continuously reflects the FIFO state, and therefore can only be read. Data written to this bit is ignored. When the ECP clock is stopped the bit is read as "1", regardless of the actual FIFO state.

**Bit-0:**
FIFO Empty bit. Read only. This bit is "0" when the FIFO has at least one byte of data. This bit is "1" when the FIFO is empty. This bit continuously reflects the FIFO state, and therefore can only be read. Data written to this bit is ignored. When the ECP clock is stopped, this bit is read as "1", regardless of the actual FIFO state.

**EXTENDED CAPABILITIES PARALLEL PORT (ECP)**
The ECP support includes a 16-byte FIFO that can be configured for either direction, command / data FIFO, a FIFO threshold interrupt for both directions, FIFO empty and full status bits, automatic generation of strobes (by hardware) to fill or empty the FIFO, transfer of commands and data, and a Run Length Encoding (RLE) expanding /decompression) as explained below.

The Extended Capabilities Port (ECP) is enabled when bit-2 of PCR is "1". Once enabled, its mode is controlled via the mode field of ECR-bits 5, 6, 7 of ECR register.

The ECP has ten registers:
The AFIF0, CFIF0, DFIFO and TFIFO registers access the same ECP FIFO. The FIFO is accessed at Base + 000Hex, or Base + 400Hex, depending on the mode field of ECR and the register. FIFO can be accessed by host DMA cycles, as well as host PIO cycles.

When DMA is configured and enabled (bit-3 of ECR is "1" and bit-2 of ECR is "0") the ECP automatically issues DMA requests to fill the FIFO (in the forward direction when bit-5 of CTR is "0") or to empty the FIFO (in the backward direction when bit-5 of CTR is "1"). All DMA transfers are to or from these registers. The ECP does not assert DMA request for more than 32 consecutive DMA cycles. The ECP stops requesting DMA when TC is detected during an ECP DMA cycle.

Writing into a full FIFO, and reading from an empty FIFO, are ignored. The written data is lost, and the read data is undefined. The FIFO empty and full status bits are not latched by such access. Some registers are not accessible in all modes of operation, or may be accessed in one direction only. Accessing a non-accessible register has no effect: Data read is undefined, data written is ignored, the FIFO does not update. The ST78C36 Parallel Port registers (DTR, STR and CTR) are not accessible when ECP is enabled.

To improve noise immunity in ECP cycles, The state machine does not examine the control handshake response lines until the data has had time to switch.

a. The software should enable ECP after bits 0-

3 of the parallel port control register (CTR) are "0".

b. When ECP is enabled, and the software wishes to switch modes, it should switch only through modes 000 or 001.

c. When ECP is enabled, The software should change direction only in mode 001.

d. The software should switch from mode 010, or 011, to mode 000, or 001 , only when the FIFO is empty.

e. The software should switch to mode 011 when bits 0,1 of CTR are "0".

f. The software should switch to mode 010 when bit-0 of CTR is "0".

g. The software should disable ECP only when in mode 000 or 001.

Software may switch from mode 011 backward direction to modes 000 or 001 when there is an on-going ECP read cycle. In this case the read cycle is aborted by deasserting AFD*. The FIFO is reset and a potential byte expansion is automatically terminated since the new mode is 000 or 001.

The ECP uses the Xtal1 clock. This clock can be stopped for power down mode. When this power-down mode occurs, the DMA is disabled, all interrupts ( except ACK*) are masked, and the FIFO registers are not accessible. The other ECP registers are always accessible when the ECP is enabled. During this period the FIFO status and contents are not lost, although the host reads bit-2 of ECR as "0", bit-1 of ECR as "1" and bit-0 of ECR as "1", regardless of the actual values of these bits. When the clock starts toggling again these bits resume their original functions.

When the clock is stopped, an on going ECP cycle may be corrupted but the next ECP cycle will not start even if in forward direction the FIFO is not empty, and in backward direction the FIFO is not full. If the ECP clock starts or stops toggling during a host cycle that accesses the FIFO, the cycle may yield wrong data.

**SOFTWARE CONTROLLED DATA TRANSFER**
(MODES 000 AND 001)
Software controlled data transfer is supported in modes 000 and 001. The software generates peripheral device cycle by modifying the DATA and CTR registers and reading the STR, CTR and DATA registers. The negotiation phase and nibble mode transfer, as defined in the IEEE 1284 standard, are performed in these modes. In these modes the FIFO is reset and is not
Mode 000 is for the forward direction only; the direction bit is forced to "0" and PD7-0 is driven. Mode 001 is for both the forward and backward directions. The direction bit controls whether PD7-0 are driven.

**AUTOMATIC DATA TRANSFER (Modes 010 and 011)**
Automatic data transfer (ECP cycles generated by hardware) is supported only in modes 010 and 011. Automatic DMA access to fill or empty the FIFO is supported in modes 010, 011 and 110. Mode 010 is for the forward direction only; the direction bit is forced to "0" and PD7-0 is driven. Mode 011 is for both the forward and backward directions. The direction bit controls whether PD7-0 is driven.
Automatic Run Length Expanding (RLE) is supported in the backward direction.

**Forward Direction (Bit-5 of CTR = 0)**
When the ECP is in forward direction and the FIFO is not full
(bit-1 of ECR is "0") the FIFO can be filled by software writes to the FIFO registers (AFIFO and DFIFO in mode 011, and CFIFO in mode 010).
When DMA is enabled (bit-3 of ECR is "1" and bit-2 of ECR is "0") the ECP automatically issues DMA requests to till the FIFO with normal data bytes. When the ECP is in forward direction and the FIFO is not empty the ECP pops a byte from the FIFO write cycle to the peripheral device. The ECP drives AFD* according to the operation mode (ECR bits 5-7) and according to the tag of the popped byte as follows: In Parallel Port FIFO mode (mode 010) AFD* is

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controlled by bit "1" of CTR. In ECP mode (mode 011 ) AFD* is controlled by the popped tag. AFD* is driven high for normal data byte and driven low for command byte.

**ECP (Forward) Write Cycle**
An ECP write cycle starts when the ECP drives the popped tag onto AFD* and popped byte onto PD7-0. When BUSY* is low the ECP asserts STROBE*. In 010 mode the ECP deasserts STROBE* to terminate the write cycle. In 011 mode the ECP waits for BUSY* to be high. When BUSY* is high the ECP deasserts STROBE* and changes AFD* and PD7-0 only after BUSY* is low.

**Backward Direction (Bit-5 of CTR is "1")**
When the ECP is in the backward direction, and the FIFO is not full (bit-1 of ECR is "0"), the ECP issues a read cycle from the peripheral device and monitors the BUSY* signal. If BUSY* is high the byte is a data byte and it is pushed into the FIF0. If BUSY* is low the byte is a command byte.

The ECP checks bit-7 of the command byte, if it is high the byte is ignored, if it is low the byte is tagged as an RLC byte (not pushed into the FIFO but used as a Run Length Count to expand The next byte read). Following an RLC read the ECP issues a read cycle from the peripheral device to read The data byte to be expanded. This byte is considered a data byte, regardless of its BUSY* state. This byte is pushed into the FIFO (RLC+ 1) times.
When The ECP is in the backward direction, and the FIFO is not empty (bit-0 of ECR is "0"), the FIFO can be emptied by software reads from the FIFO register (only DFIFO in mode 011, no AFIFO and CFIFO read). When DMA is enabled (bit-9 of ECR is "1" and bit-2 of ECR is "0") the ECP automatically issues DMA requests to empty the FIFO (only in mode 011).

**ECP (Backward) Read Cycle**
An ECP read cycle starts when the ECP drives AFD* low. The peripheral device drives BUSY* high for a normal data read cycle, or drives BUSY* low for a command read cycle, and drives the byte to be read onto PD7-0.
When ACK* is asserted the ECP drives AFD* high then reads the PD7-0 byte. When AFD* is high the peripheral device deasserts ACK* and may change BUSY* and PD7-0 states in preparation for the next cycle.

**FIFO TEST ACCESS (MODE 110)**
Mode 110 is for testing the FIFO in PIO and DMA cycles. Both read and write operations (pop and push) are supported, regardless of the direction bit. In the forward direction PD7-0 are driven, but the data is undefined This mode can be used to measure the host ECP cycle throughput, usually with DMA cycles. This mode can also be used to check the FIFO depth and its interrupt threshold, usually with PIO cycles.

**CONFIGURATION REGISTERS ACCESS (MODE 111)**
The two configuration registers, CNFGA and CNFGB, are accessible only in this mode.

**Interrupt**
Interrupt is generated when any of the following events occur.

a. When bit-2 of ECR is "0", bit-3 of ECR is "1" and TC is asserted during the ECP DMA cycle.
b. When bit-2 of ECR is "0", bit-3 of ECR is "0", bit-5 of CTR is "0" and There are eight or more bytes free in the FIF0. It includes the case when bit-2 of ECR is cleared to "0" and there are already eight or more bytes free in the FIFO (modes 010, 011 and 110 only).
c. When bit-2 of ECR is "0", bit-3 of ECR is "0", bit-5 of CTR is "1" and there are eight or more bytes to be read from the FIF0. It includes the case when bit-2 of ECR is cleared to "0" and there are already eight or more bytes to be read from the FIFO (modes 011 and 110 only).
d. When bit-4 of ECR is "0" and ERROR is asserted (high to low edge) or ERROR is asserted when bit-4 of ECR is modified from "1" to "0".
e. When bit-4 of CTR is "1" and ACK* is deasserted (low-to-high edge). The interrupt is generated according to bits 4, 5 and 6 of PCR.

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Special circuitry provides protection against damage that might be caused when the printer is powered but the ST78C36 is not.

Enhanced Parallel Port (EPP) modes of operation and one Extended Capabilities Port (ECP) mode to complete a full IEEE 1286 parallel port. In Compatible mode a write operation causes the data to be presented on pins PD7-0. A read operation In this mode causes the Data Register to present the last data written to it by the CPU.

In the Extended mode a write operation to the data register causes the data to be latched. If the Data Port Direction bit (CTR-5) is "0", the latched data is presented to the pins; if it "1" the data is only latched. When Data Port Direction bit (CTR-5) is "0", a read operation from this register allows the CPU to read the last data it written to the port. In the Extended Mode with the Data Port Direction bit set to "1" (read), a read from this register causes the port to present the data on pins PD7-0.