MOTOROLA

MC14422

Advance Information

CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

REMOTE CONTROL TRANSMITTER

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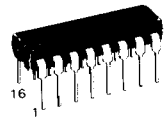
The MC14422 is a remote control transmitter circuit designed for use in television receivers, security controls, toys, industrial remote controls, and remote control locks. The circuit is intended for use with the MC6525 or MC6526 NMOS remote control receiver.

Using digital frequency multiplexing, the MC14422 generates five frequencies which are transmitted sequentially to form a code corresponding to a particular function in the receiver circuit. The wide channel spacing between these frequencies eliminates problems due to doppler effect. The frequency multiplex system inherently provides a good degree of noise immunity.

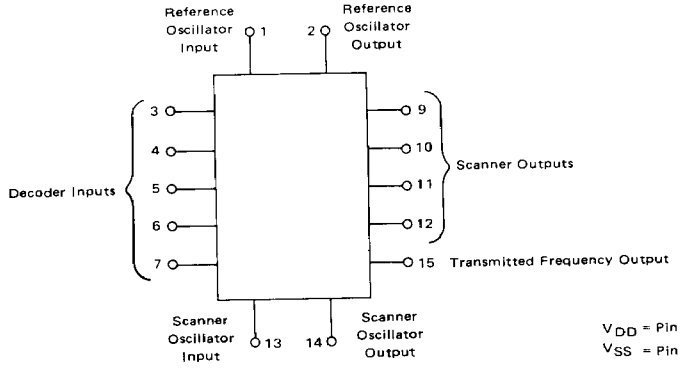
- 22 Channel Capacity
- Transmission of Information Is Achieved by Time Multiplexing Five Frequencies
- No Possibility of Doppler Effect Interference
- Extremely Low External Component Count
- Low Power Consumption
- Designed for Use with the MC6525 or MC6526 Remote Control Receiver



P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +10	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +55	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{DD}	5.0	–	8.0	Vdc
Supply Current		I_{DD}				
(V_{DD} = 8.0 Vdc)	Idle		–	0.4	100	µAdc
	Operating		–	–	10	mAdc
Output Drive Current		I_{OH}				
(V_{OH} = 4.0 Vdc, V_{DD} = 5.0 Vdc	Source					
Scanner Output			-50	–	–	µAdc
Transmitted Frequency Ouptut			-0.5	–	–	mAdc
Scanner Oscillator Output			-0.1	–	–	mAdc
Reference Oscillator Output			-0.3	–	–	mAdc
(V_{OL} = 1.0 Vdc, V_{DD} = 5.0 Vdc)	Sink	I_{OL}				
Scanner Output			50	–	–	µAdc
Transmitted Frequency Output			0.2	–	–	mAdc
Scanner Oscillator Output			0.1	–	–	mAdc
Reference Oscillator Output			0.3	–	–	mAdc
Input Current		I_{IH}				µAdc
(V_{IH} = 8.0 Vdc, V_{DD} = 8.0 Vdc)	Sink					
Scanner Oscillator Input			–	–	1.0	
Reference Oscillator Input			4.0	–	400	
(V_{IH} = 7.0 Vdc, V_{DD} = 8.0 Vdc)	Source					
Decoder Input			-1.0	–	–	
(V_{IL} = 0 Vdc, V_{DD} = 8.0 Vdc)	Source	I_{IL}				µAdc
Scanner Oscillator Input			–	–	1.0	
Reference Oscillator Input			-4.0	–	-400	
(V_{IL} = 1.0 Vdc, V_{DD} = 5.0 Vdc)	Sink					
Decoder Input			–	–	-25	
Reference Oscillator Frequency (V_{DD} = 5.0 Vdc)		f_{ref}	–	–	1.0	MHz

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CIRCUIT OPERATION

As shown in Figure 1, until a matrix switch is depressed, the decoder inputs (pins 3 through 7) are high, all scanner outputs (pins 9 through 12) are low, and both the scanner and reference oscillators, as well as the output gate control circuit, are switched off. This is referred to as the "idle" mode. In this mode, with a significant part of the circuit switched off, current consumption is reduced to a minimum. The decoder section, however, remains in continuous operation so that a switch matrix command can be recognized. When a switch is depressed, the decoder will set the five latches in accordance with the correct code (see Figure 2). At the same time, a latch is triggered which activates the idle line and turns on the reference oscillator, the scanner oscillator, the row enable, and the output gate control.

When the switch is operated just prior to time period t1, the following happens:

1. The scanner outputs become active and take up their respective code corresponding to t1 when the next negative going edge of the scanner oscillator occurs.
2. The reference oscillator is switched on.
3. The output gate control idle input is enabled.

Note: No output can occur at the transmitted frequency output (pin 15) until the negative going edge of the pin 12 scanner output signal has occurred at the end of time t4.

The timing example of Figure 1 uses the matrix connection of pin 4 connected to pin 11. Table 1 shows that the code for this connection is f_a transmitted in time period t2 and f_b transmitted in time period t3. After the negative going edge of the pin 12 scanner pulse has enabled the output gate control, an output cycle can begin. Therefore, in this case no output occurs in the time period t1, f_a and f_b are transmitted in time periods t2 and t3 respectively, and no output occurs during time t4.

The code is repeated continuously at pin 15 until the matrix switch is released. At this point the circuit completes the scan cycle and the trailing edge of the pin 12 scanner signal returns the circuit to its "idle" position.

The transmitted frequencies are generated by dividing a reference oscillator frequency by a variable divider circuit which is controlled by the decoder outputs.

TABLE 1 – TRANSMITTED FREQUENCY CODE

Channel Number	Matrix Connections Pin to Pin		Transmitted Frequencies t1	t2	t3	t4
1	7	12	f_e			
2	7	9	f_e	f_a		
3	7	10	f_e		f_b	
4	7	11	f_e	f_a	f_b	
5	6	12	f_e			f_c
6	6	9	f_e	f_a		f_c
7	6	10	f_e		f_b	f_c
8	6	11	f_e	f_a	f_b	f_c
9	5	12	f_e			f_d
10	5	9	f_e	f_a		f_d
11	5	10	f_e		f_b	f_d
12	5	11	f_e	f_a	f_b	f_d
13	4	12			f_b	
14	4	11		f_a	f_b	
15	3	9				f_c
16	3	10		f_a		f_c
17	4	9			f_b	f_c
18	4	10		f_a	f_b	f_c
19	3	12				f_d
20	3	11		f_a		f_d
21	3,4	12			f_b	f_d
22	3,4	11		f_a	f_b	f_d

TABLE 2 – OUTPUT FREQUENCIES

Frequencies	Output Frequency	Division Ratio
f_a	34.688 kHz	f2/26.5
f_b	36.048 kHz	f2/25.5
f_c	37.519 kHz	f2/24.5
f_d	39.116 kHz	f2/23.5
f_e	42.755 kHz	f2/21.5

f2 = 919.222 kHz reference frequency

FIGURE 1 – TIMING DIAGRAM
(Pin 4 Connected to Pin 11)

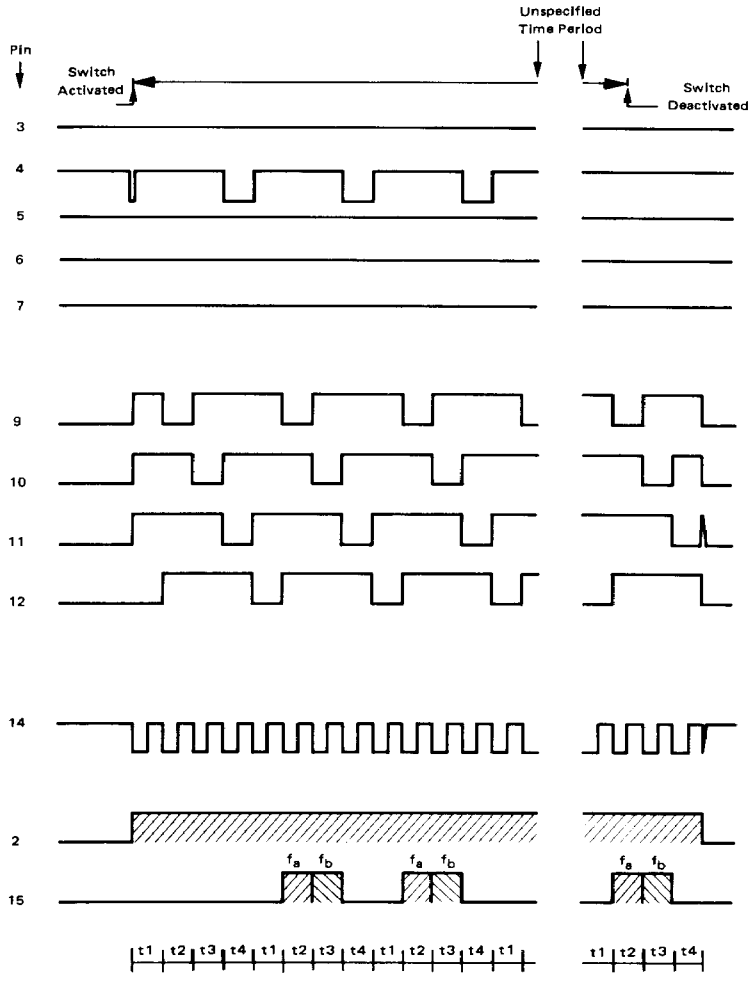


FIGURE 2 – TYPICAL APPLICATION

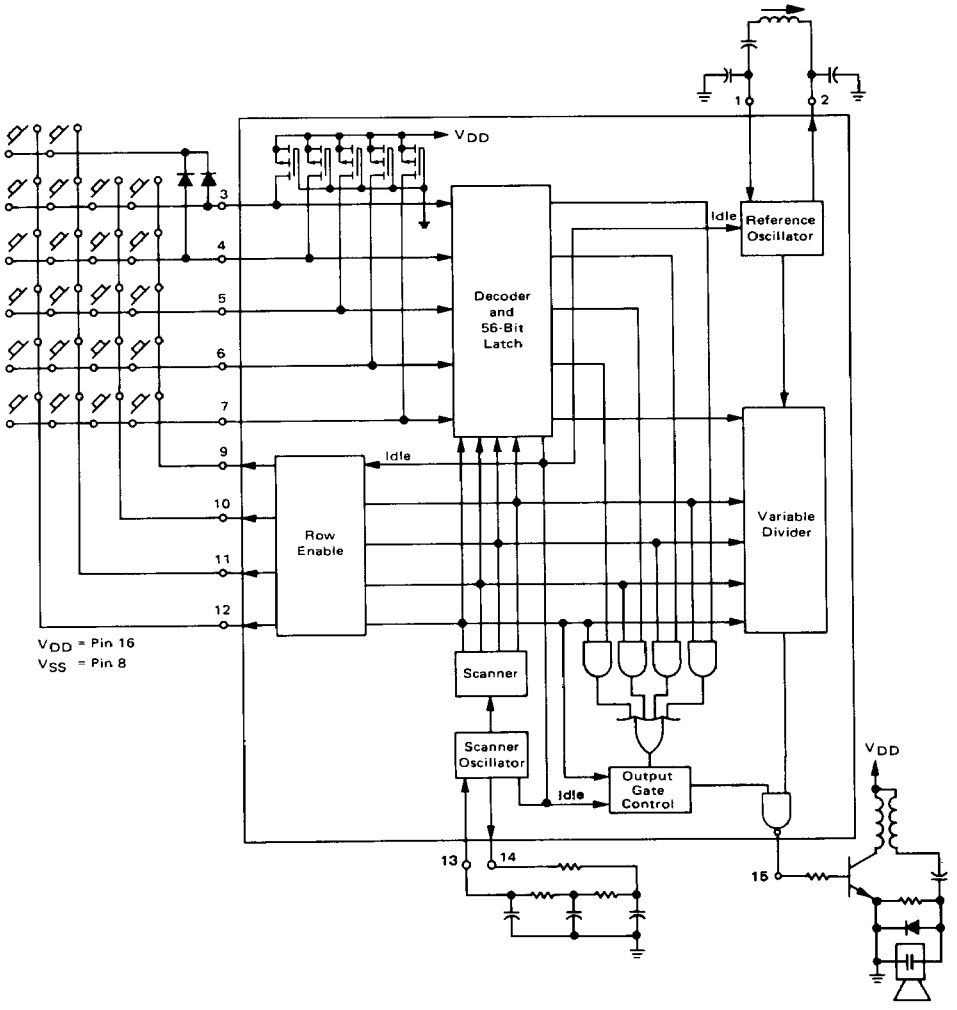
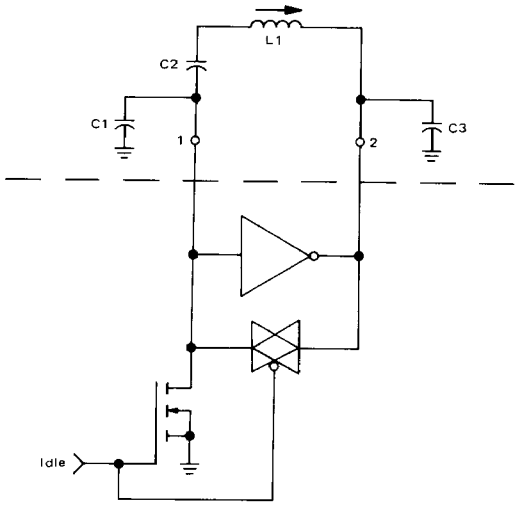


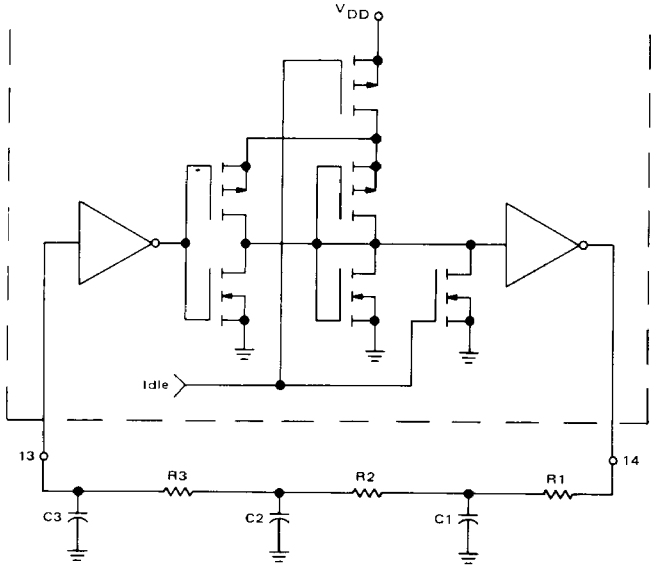
FIGURE 3 - REFERENCE OSCILLATOR EXTERNAL COMPONENTS



Recommended values for f2 = 1 MHz:

C1 = 820 pF
C2 = 180 pF
C3 = 120 pF
L1 = 160 μH, Q = 60

FIGURE 4 - SCANNER OSCILLATOR EXTERNAL COMPONENTS



The scanner ocsillator frequency can be calculated using the following formula :

$$f14 = \frac{\sqrt{3}}{2\pi RC}$$

Recommended values for F14 = 100 Hz:

R1 = 47 kΩ	C1 = 0.069 μF
R2 = 100 kΩ	C2 = 0.033 μF
R3 = 180 kΩ	C3 = 0.015 μF

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