SMART Modular Technologies

SM5321002
Sept 1991
Rev 0

SM5321002
4MByte (1M x 32) CMOS DRAM Module (*Static Column Mode*)

General Description

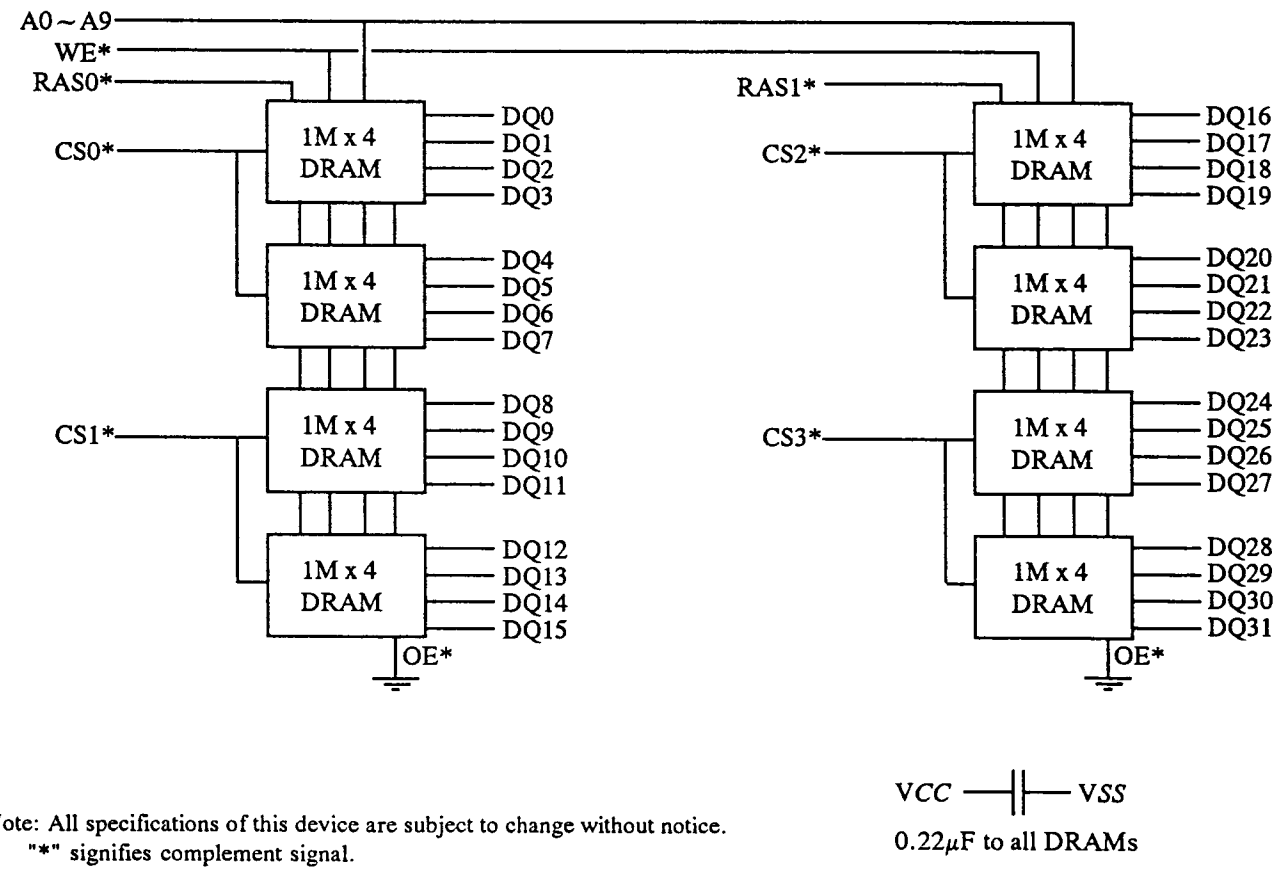
The SM5321002 is a high performance, 4-megabyte dynamic RAM module organized as 1,048,576 words by 32 bits, in a 72-pin, single-in-line memory module (SIMM) package. It offers static column mode capability at fast access times.

The module utilizes eight CMOS 1M x 4 dynamic RAMs in surface mount package on an epoxy laminate substrate. Each device is accompanied by a 0.22μf decoupling capacitor for improved noise immunity.

Features

- JEDEC standard pinout
- Fast Access Time of 60/70/80ns (max.)
- Low Power :
  4.62/4.20/3.78W (max.) - Active (60/70/80ns)
  84mW (max.) - Standby (TTL)
  42mW(max.) - Standby (CMOS)
- TTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 5V $\pm$ 5%

Functional Diagram



Note: All specifications of this device are subject to change without notice.
"*" signifies complement signal.

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Pin Name

A0 ~ A9	Address
DQ0 ~ DQ31	Data Input/Output
CS0* ~ CS3*	Column Address Strobe
RAS0*, RAS1*	Row Address Strobe
WE*	Read/Write
PD1 ~ PD4	Presence Detect
VCC	Power Supply
VSS	Ground
NC	No Connection

Presence Detect Pins

Pin	60ns	70ns	80ns
PD1	-	*VSS*	*VSS*
PD2	-	*VSS*	*VSS*
PD3	-	*VSS*	NC
PD4	-	NC	*VSS*

Ordering Information

Part Number	Speed
SM5321002-6	60ns
SM5321002-7	70ns
SM5321002-8	80ns

Pin No.	Pin Designation	Pin No.	Pin Designation
1	*VSS*	37	NC
2	DQ0	38	NC
3	DQ16	39	*VSS*
4	DQ1	40	CS0*
5	DQ17	41	CS2*
6	DQ2	42	CS3*
7	DQ18	43	CS1*
8	DQ3	44	RAS0*
9	DQ19	45	NC
10	*VCC*	46	NC
11	NC	47	WE*
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	NC	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	*VCC*
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	NC	65	DQ15
30	*VCC*	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	RAS1*	70	PD4
35	NC	71	NC
36	NC	72	*VSS*

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Voltage on any pin relative to VSS	VT	- 1 to +7.0	V
Power Dissipation	PT	8	W
Operating Temperature	TA	0 to +70	°C
Storage Temperature	Tstg	- 55 to +125	°C
Short Circuit Output Current	IOS	50	mA

Recommended DC Operating Conditions

(Ta = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Supply Voltage	4.75	5.0	5.25	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	2.4	-	6.5	V
VIL	Input Low Voltage	-1	-	0.8	V

DC Characteristics

(VCC = 5V±5%, VSS = 0V, Ta = 0 to +70 °C)

Parameter	Symbol	Test Conditions	SM5321002-6		SM5321002-7		SM5321002-8		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	ICC1	tRC = min.	-	880	-	800	-	720	mA	1, 2
Standby Current	ICC2	TTL Interface RAS*, CS*=VIH, DOUT =High Z	-	16	-	16	-	16	mA	
		CMOS Interface RAS*, CS*≥VCC - 0.2V DOUT =High Z	-	8	-	8	-	8	mA	
RAS*-Only Refresh Current	ICC3	tRC = min.	-	880	-	800	-	720	mA	2
Standby Current	ICC5	RAS*=VIH, CS*=VIL, DOUT =Enable	-	40	-	40	-	40	mA	1
CS*-Before-RAS* Refresh Current	ICC6	tRC = Min.	-	880	-	800	-	720	mA	
Static Column Mode Current	ICC9	tPC = Min.	-	880	-	800	-	720	mA	1,3,4

DC Characteristics (contd.)

Parameter	Symbol	Test Conditions	SM5321002-6		SM5321002-7		SM5321002-8		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Input Leakage Current	*ILI*	0V≤*VIN*≤7V	-80	80	-80	80	-80	80	μA
Output Leakage Current	*ILO*	0V≤*VOUT*≤7V	-10	10	-10	10	-10	10	μA
Output High Voltage	*VOH*	High *IOUT*= -5mA	2.4	*VCC*	2.4	*VCC*	2.4	*VCC*	V
Output Low Voltage	*VOL*	Low *IOUT*=4.2mA	0	0.4	0	0.4	0	0.4	V

Notes:
1. *ICC* depends on output load condition when the device is selected. *ICC* (max.) is specified at the output open condition.
2. Address can be changed once or less while RAS* = *VIL* .
3. Address can be changed once or less while CS* = *VIH* .
4. Invalid address is not permitted during static column mode cycle.

Capacitance

(*Ta* =+25°C, *VCC* = 5V±5%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	*CI1*	-	43	pF	1
Input Capacitance (WE*)	*CI2*	-	59	pF	1
Input Capacitance (RAS0*, RAS1*)	*CI3*	-	31	pF	1
Input Capacitance (CS0*~CS3*)	*CI4*	-	17	pF	1
Output Capacitance (Data-In, Data-Out)	*CI/O*	-	13	pF	1, 2

Notes:
1. Capacitance is measured with Boonton Meter or effective capacitance method.
2. CS*=*VIH* to disable D*OUT*.

AC Characteristics (1)

(*Ta* = 0 to +70 °C, *VCC* = 5.0V±5%, *VSS* = 0V)

Parameter	Symbol	SM5321002-6		SM5321002-7		SM5321002-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t*RC*	110	-	130	-	150	-	ns	
Access time from RAS*	t*RAC*	-	60	-	70	-	80	ns	2, 3
Access time from CS*	t*ACS*	-	15	-	20	-	20	ns	3, 4
Access time from address	t*AA*	-	30	-	35	-	40	ns	3, 5
Output buffer turn-off time	t*OFF*	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	t*T*	3	50	3	50	3	50	ns	7
RAS* precharge time	t*RP*	40	-	50	-	60	-	ns	
RAS* pulse width	t*RAS*	60	10000	70	10000	80	10000	ns	

AC Characteristics (contd.)

Parameter	Symbol	SM5321002-6		SM5321002-7		SM5321002-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
RAS* hold time	t*RSH*	15	-	20	-	20	-	ns	
CS* hold time	t*CSH*	60	-	70	-	80	-	ns	
CS* pulse width	t*SP*	15	10000	20	10000	20	10000	ns	
RAS* to CS* delay time	t*RCD*	20	45	20	50	20	60	ns	8
RAS* to column address delay time	t*RAD*	15	30	15	35	15	40	ns	9
CS* to RAS* precharge time	t*SRS*	10	-	10	-	10	-	ns	
Row address set-up time	t*ASR*	0	-	0	-	0	-	ns	
Row address hold time	t*RAH*	10	-	10	-	10	-	ns	
Column address set-up time	t*ASW*	0	-	0	-	0	-	ns	
Column address hold time	t*AHW*	15	-	15	-	15	-	ns	
Column address to RAS* lead time	t*RAL*	30	-	35	-	40	-	ns	
Read command set-up time	t*RCS*	0	-	0	-	0	-	ns	
Read command hold time to CS*	t*RCH*	0	-	0	-	0	-	ns	12
Read command hold time to RAS*	t*RRH*	0	-	0	-	0	-	ns	12
Write command hold time	t*WCH*	15	-	15	-	15	-	ns	
Write command pulse width	t*WP*	10	-	10	-	10	-	ns	
Write command to RAS* lead time	t*RWL*	15	-	20	-	20	-	ns	
Write command to CS* lead time	t*CWL*	15	-	20	-	20	-	ns	
Data-in set-up time	t*DS*	0	-	0	-	0	-	ns	11
Data-in hold time	t*DH*	15	-	15	-	15	-	ns	11
Refresh period (1024 cycles)	t*REF*	-	16	-	16	-	16	ms	
Write command set-up time	t*WCS*	0	-	0	-	0	-	ns	10
CS* set-up time (CBR refresh)	t*CSR*	10	-	10	-	10	-	ns	
CS* hold time (CBR refresh)	t*CHR*	10	-	10	-	10	-	ns	
RAS* precharge to CS* hold time	t*ZRH*	10	-	10	-	10	-	ns	
Static column mode cycle time	t*SC*	35	-	40	-	45	-	ns	
CS* precharge time (Static column)	t*SI*	10	-	10	-	10	-	ns	
RAS* pulse width (Static column)	t*RASC*	-	100000	-	100000	-	100000	ns	

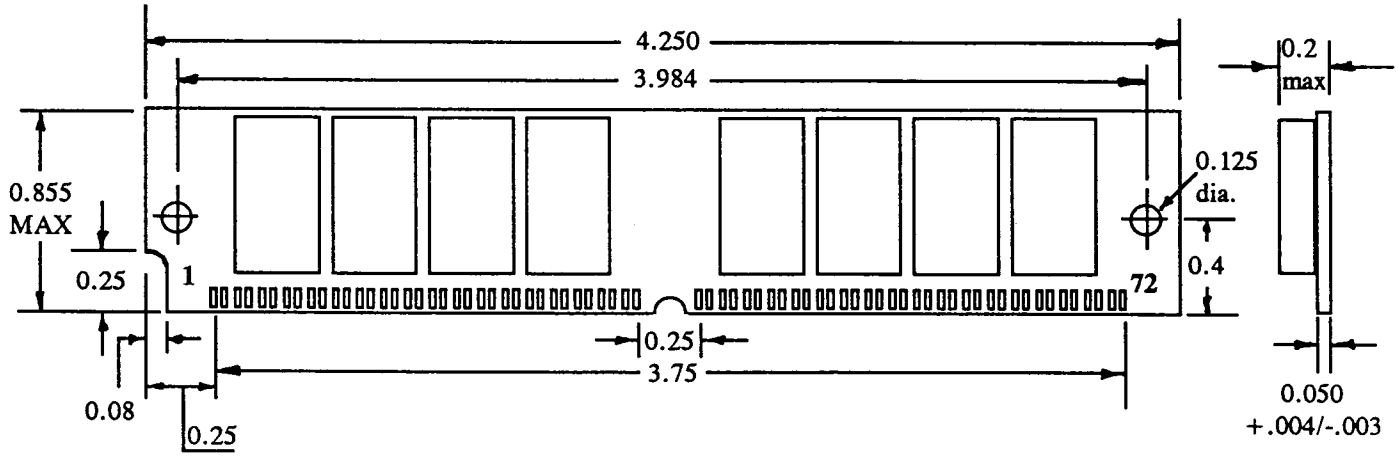
Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that t*RCD* $\leq$ t*RCD* (max) and t*RAD* $\leq$ t*RAD* (max). If t*RCD* or t*RAD* is greater than the maximum recommended value shown in this table, t*RAC* exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that t*RCD* $\geq$ t*RCD* (max) and t*RAD* $\leq$ t*RAD* (max).
5. Assumes that t*RCD* $\leq$ t*RCD* (max) and t*RAD* $\geq$ t*RAD* (max).
6. t*OFF* (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V*IH* (min) and V*IL* (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V*IH* and V*IL*.
8. Operation with the t*RAD* (max) limit ensures that t*RAC* (max) can be met. t*RCD* (max) is specified as a reference point

Notes (contd.):

only. If t*RCD* is greater than the specified t*RCD* (max) limit, then access time is controlled exclusively by t*ACS*.

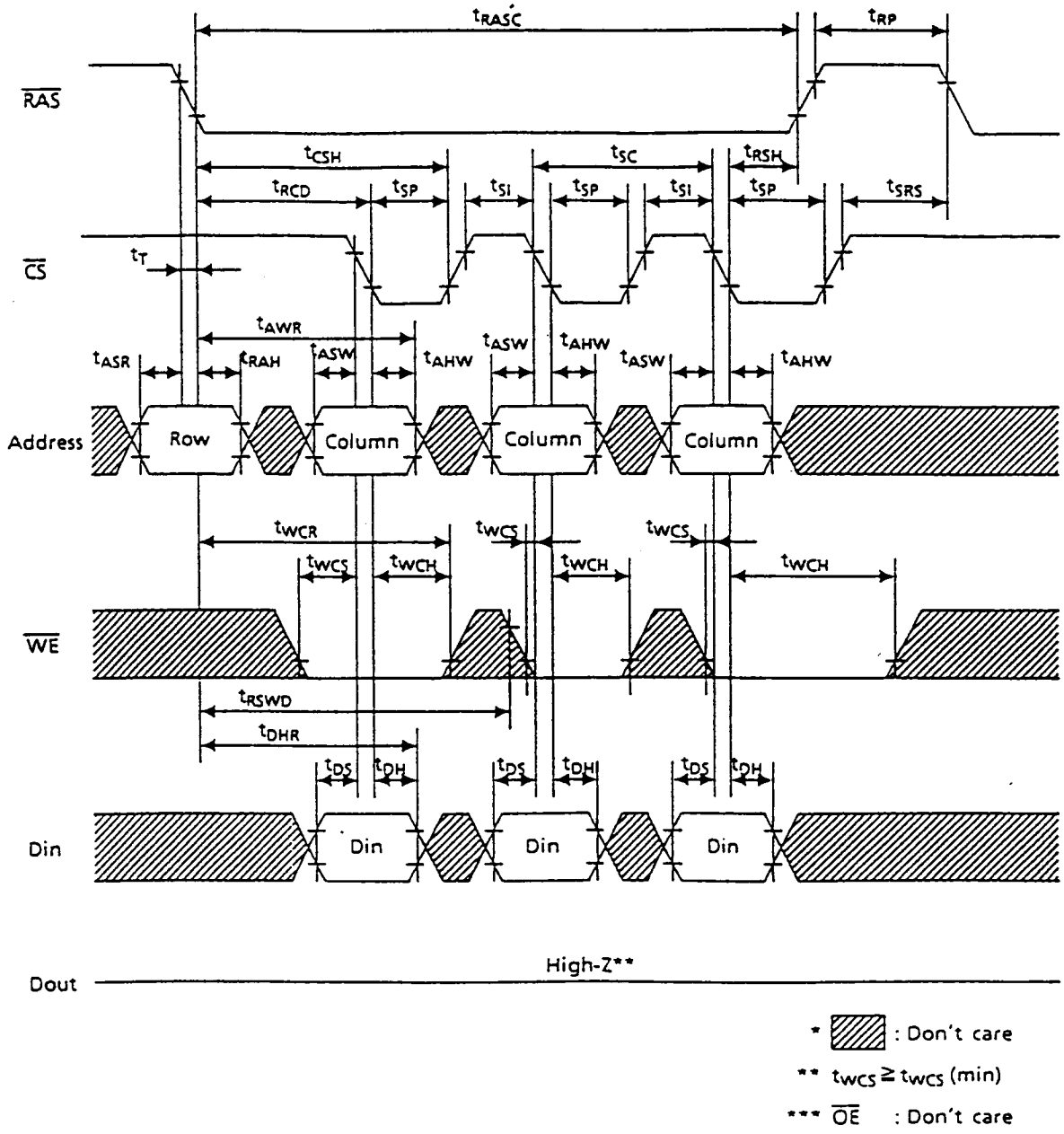
9. Operation with the t*RAD* (max) limit ensures that t*RAC* (max) can be met. t*RAD* (max) is specified as a reference point only. If t*RAD* is greater than the specified t*RAD* (max) limit, then access time is controlled exclusively by t*AA*.
10. t*WCS* is not a restrictive parameter. It is included in the datasheet as a electrical characteristic only: If *WCS* $\geq$ t*WCS* (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
11. These parameters are referenced to CS* leading edge in an early write cycle and to WE* leading edge in a delayed write or a read-modify-write cycle.
12. Either t*RCH* or t*RRH* shall be satisfied.

Physical Dimensions

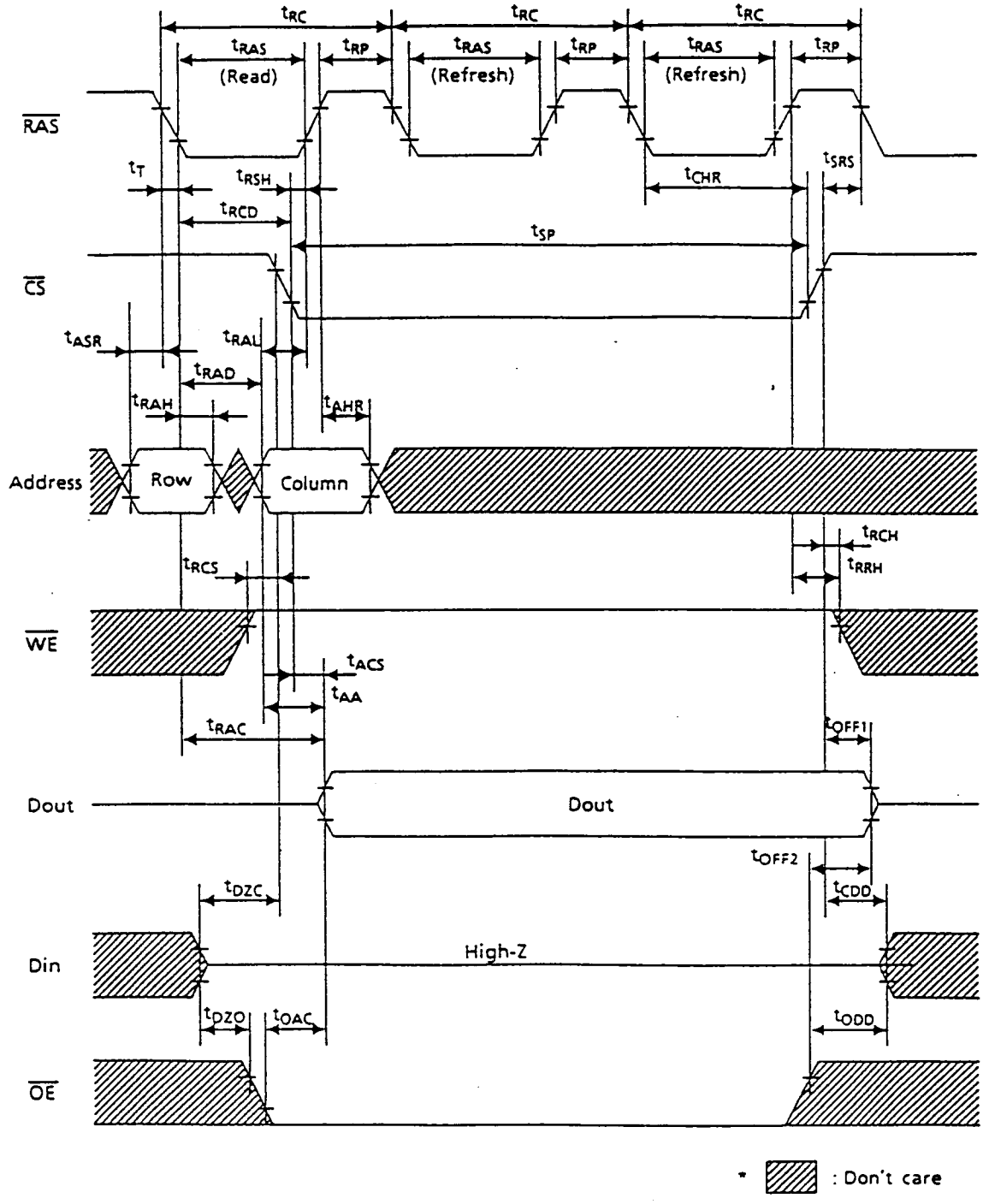


(All dimensions are in inches with ±0.005" tolerance unless otherwise specified)

Static Column Mode Write Cycle (2)

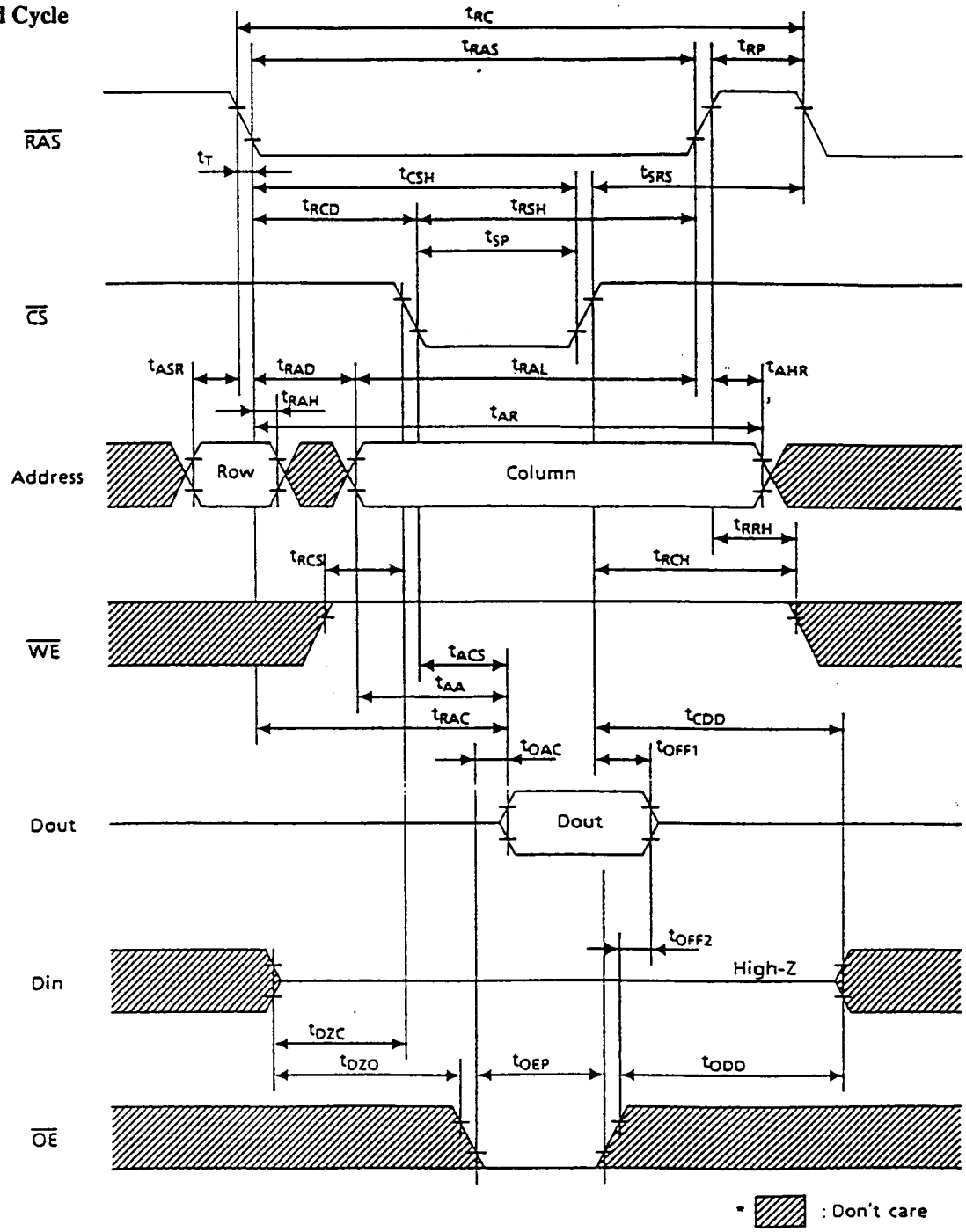


Hidden Refresh Cycle

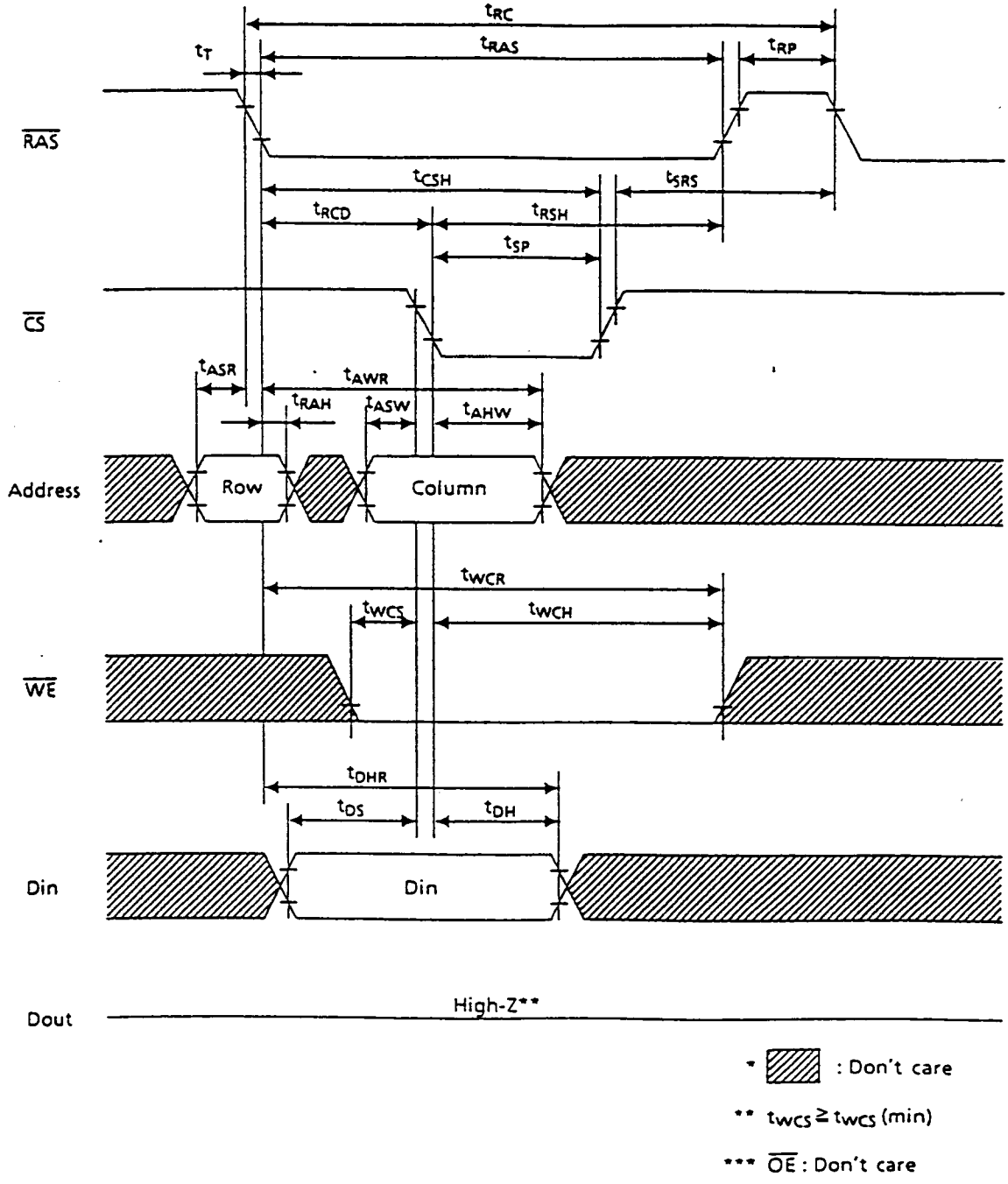


TIMING WAVEFORMS

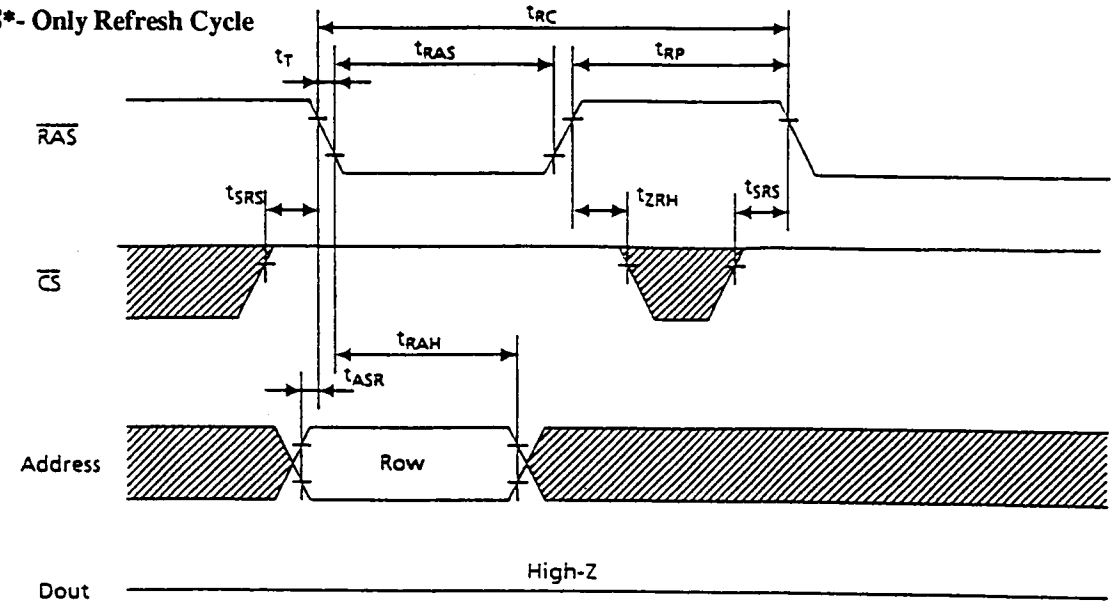
Read Cycle



Early Write Cycle

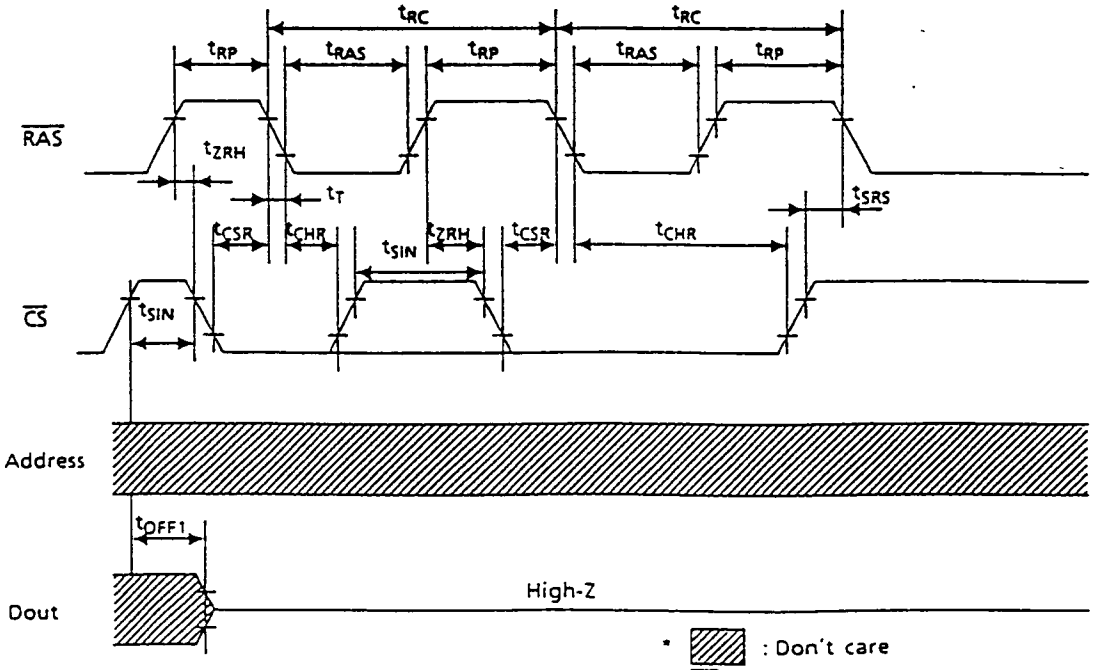


RAS*- Only Refresh Cycle



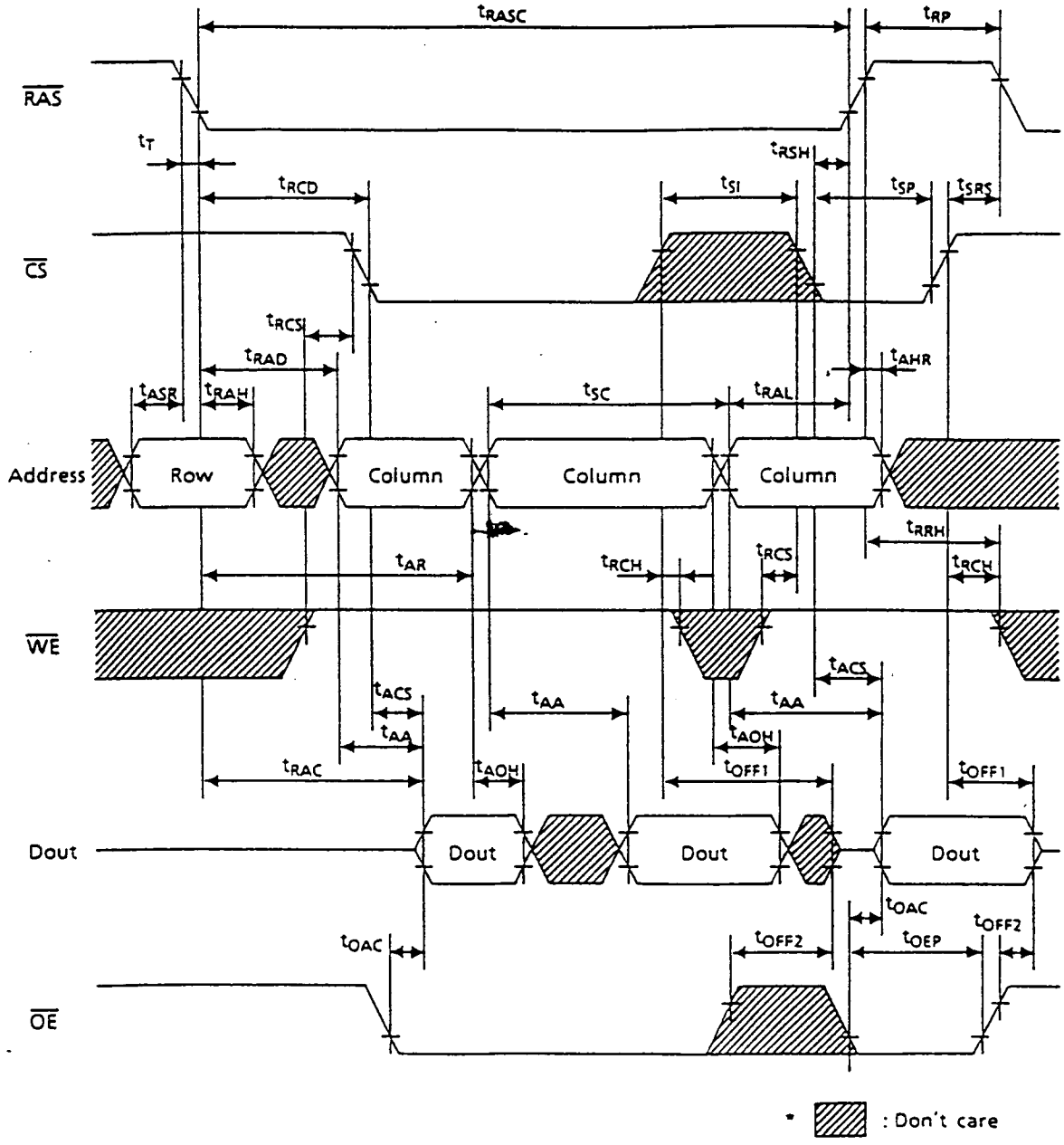
* OE, WE : Don't care
** ▨ : Don't care
*** Refresh address : A0 – A9 (AX0 – AX9)

CS*-Before-RAS* Refresh Cycle



* ▨ : Don't care
** OE : Don't care
*** WE : V_{IH}

Static Column Mode Read Cycle



Static Column Mode Write Cycle (1)