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PLESSEY
Semiconductors

SP1692

QUAD LINE RECEIVER

Four differential amplifiers with emitter follower outputs are provided.

The device can be configured as a differential line receiver or by using the internal V_{BB} reference single ended ECL signals can be received. The SP1692 is also ideally suited for use in expanding the fan out of ECL circuits, or inverting ECL logic.

FEATURES

- ECL 10000 Compatible
- 50Ω Line Driving Capability
- Single or Differential Operation
- Operating Temperature Range -30°C to +85°C

ORDERING INFORMATION

SP1692DG (Industrial - Ceramic DIL package)
SP1692BB DG (Plessey High Reliability Ceramic DIL package)

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\lvert V_{CC} - V_{EE} \rvert$ 8V
Input voltages	0V to V_{EE}
Output source current	<40mA
Storage temperature range	-65°C to +150°C
Junction operating temperature	<175°C

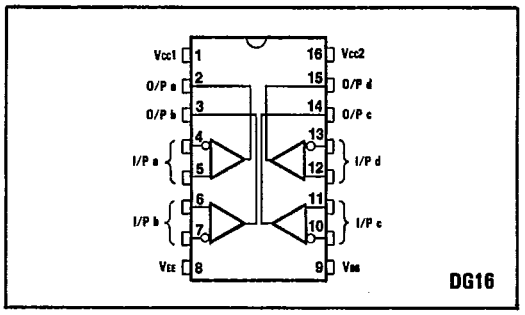

Fig.1 Pin connections (top view)

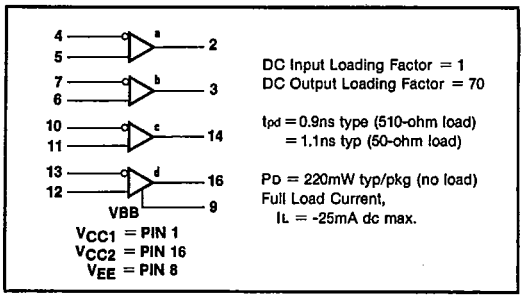

Fig.2 Logic diagram of SP1692

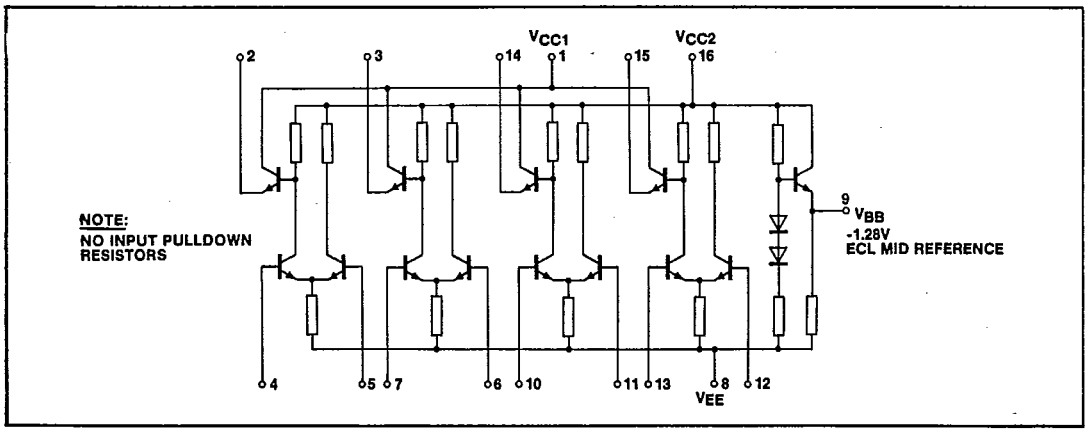

Fig.3 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0V dc.

Test temp.	TEST VOLTAGE (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{BB}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	From	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	Pin	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	9	-5.2

Characteristic	Symbol	Pin under test	SP1692 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{BB}	V_{EE}	V_{CC} (GND)
POWER SUPPLY																
Drain current	I_{EE}	8	-	-	-	50	-	-	mAdc	-	4,7,10,13	-	-	5,6,11,12	8	1,16
Input current	I_{INH}	4	-	-	-	250	-	-	µAdc	4	7,10,13	-	-	5,6,11,12	8	1,16
Input leakage current	I_{INL}	4	-	-	-	100	-	-	µAdc	-	7,10,13	-	-	5,6,11,12	8,4	1,16
Logic '1' output voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	-	-	5,6,11,12	8	1,16
Logic '0' output voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	7,10,13	-	-	5,6,11,12	8	1,16
Logic '1' threshold	V_{OHA}	2	-1.065	-	-0.980	-	-0.910	-	Vdc	-	7,10,13	-	4	5,6,11,12	8	1,16
voltage																
Logic '0' threshold	V_{OLA}	2	-	-1.630	-	-1.600	-	-1.555	Vdc	-	7,10,13	4	-	5,6,11,12	8	1,16
voltage																
Reference voltage	V_{BB}	9	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	Vdc	-	-	-	-	5,6,11,12	8	1,16
SWITCHING TIMES (50 ohm load)										Pulse in		Pulse out			-3.2V	+2.0V
Propagation delay	t_{4-2+}	2	-	1.6	-	1.5	-	1.7	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	-	1.8	-	1.7	-	1.9	ns	4		2		5,6,11,12	8	1,16
Rise time	t_{2+}	2	-	2.2	-	2.1	-	2.3	ns	4		2		5,6,11,12	8	1,16
Fall time	t_{2-}	2	-	2.2	-	2.1	-	2.3	ns	4		2		5,6,11,12	8	1,16

Thermal characteristics θ_{JA} = 120° C/W
θ_{JC} = 40° C/W

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