SED1522

■ DESCRIPTION

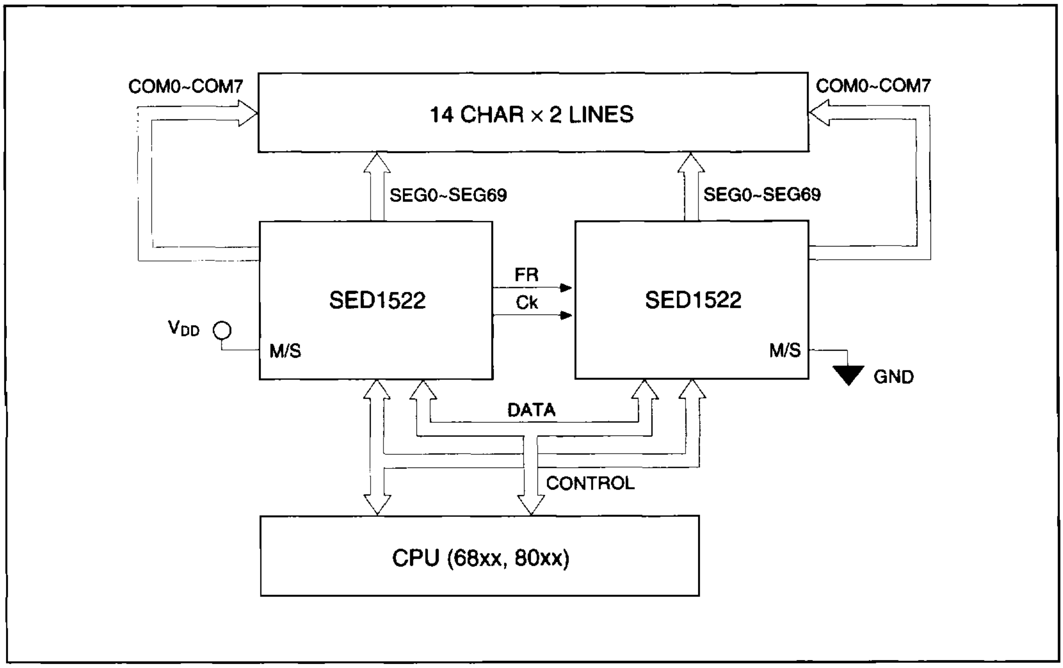
The SED1522 is a graphic LCD controller driver designed for use in a dot matrix LCD (Liquid Crystal Display) system capable of displaying characters and graphics. The bit-addressable display data which is sent from an 8-bit microcomputer is stored in a built-in display RAM which generates the signals required for driving the LCD. The circuitry has been designed to ensure low power consumption and a wide range of operating voltages, for use in high-performance handheld systems that run on batteries.

The SED1522 can use a single chip to drive an LCD of 13 characters by one line each plus an indicator. The SED1522 can be used in master-slave combination. Moreover, the SED1521 segment driver is available for expanding a system to enable 80-port output in order to construct mid-capacity displays using a minimal number of drivers.

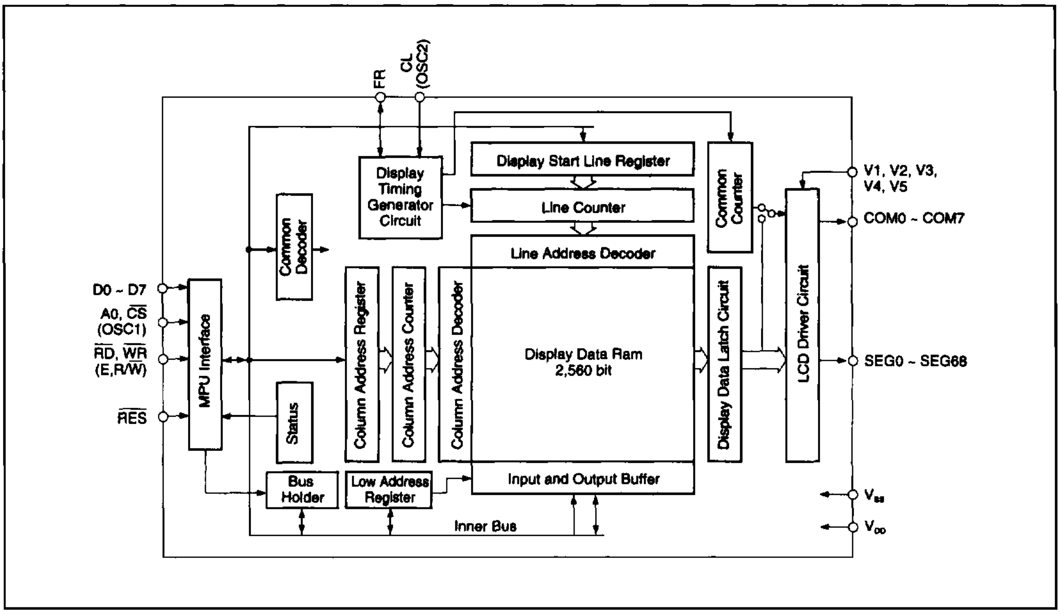
■ FEATURES

- Low-power CMOS technology 30µW
- Fast CPU 8-bit data interface (80xx, 68xx)
- 1/8 to 1/16 duty cycle
- Built-in LCD driver circuit .... 69 segments
  8 commons
- Built-in display data RAM .... 2560 bits
- Rich display command setting
- On-chip CR oscillation circuit
- Master/slave operation is supported
- LCD voltage ....–3.5 to –13V
- Single power supply .... 2.4 to 7.0V
- Package .... QFP5-100 pin (FOA, FAA)
  QFP15-100 pin (FOC, FAC)
  Al pad (DOA, DAA)
  Au bump (DOB, DAB)

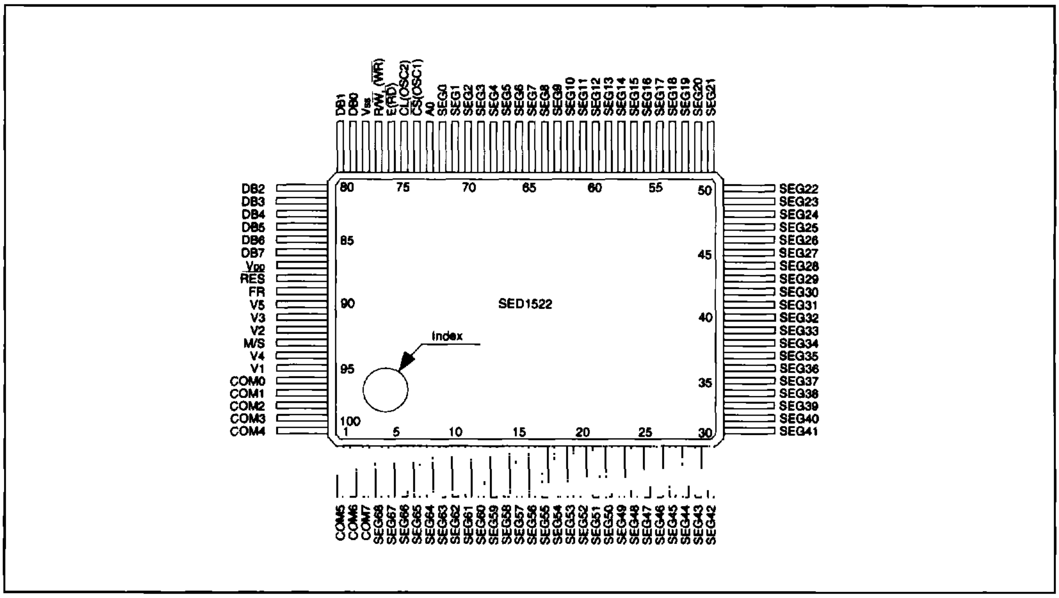
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



Model Name	Terminal No.	
	74	75
SED1522FOA	OSC1	OSC2
SED1522FAA	$\overline{\text{CS}}$	CL

* The Common output COM0 to COM7 of the Master LSI corresponds COM15 to COM8 on the Slave LSI.

■ PIN DESCRIPTION

Terminal Name	Function
DB0~DB7	Data input
A0	Selects display data or instructions. HIGH: Display data. LOW: Instructions.
$\overline{RES}$	Resets the system and selects the interface type for a 68-port/80-port MPU. HIGH: 68-port MPU interface. LOW: 80-port MPU interface.
$\overline{CS}$	Chip Select input. LOW: Active level sensing.
E ($\overline{RD}$)	Read/Write Enable signal when a 68-port MPU is connected. (Active-LOW Read Enable signal when an 80-port MPU is connected.)
R/$\overline{W}$ ($\overline{WR}$)	Read/Write Select signal when a 68-port MPU is connected. HIGH: Read Select LOW: Write Select (Active-LOW Write Enable input when an 80-port MPU is connected. Rising edge sensing.)
CL	External clock input (only effective with external clock types).
FR	LCD Frame (AC-conversion) signal input/output.
SEG0~SEG68	Segment output for driving the LCD.
COM0~COM7 (COM15~COM8)	Common output for driving the LCD.
M/S	Master/Slave Select signal.
V_{DD}	5V power supply.
V_{SS}	0V power supply (GND level).
V1, V2, V3, V4, V5	Power supplies for driving the LCD. $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

■ CLOCK OPTIONS

Model Name	Operating Clock		Connectable Drivers	Package
	Internal oscillator	External clock		
SED1522FOA	18kHz	18kHz	SED1522FOA, SED1521FOA	QFP5-100pin
SED1522DOA			SED1522DOA, SED1521DOA	AL pad chip
SED1522DOB			SED1522DOB, SED1521DOB	Au Bump chip
SED1522FAA	—	2kHz	SED1522FAA, SED1521FAA	QFP5-100pin
SED1522DAA			SED1522DAA, SED1521DAA	AL pad chip
SED1522DAB			SED1522DAB, SED1521DAB	Au Bump chip

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0V, V_{DD} ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5)

Parameter		Symbol	Ratings	Unit
Supply voltage (1)		V_{SS}	–8.0 to 0.3	V
Supply voltage (2)		V5	–16.5 to 0.3	V
Supply voltage (3)		V1, V2 V3, V4	V5 to 0.3	V
Input voltage		V_I	V_{SS}–0.3 to 0.3	V
Output voltage		V_O	V_{SS}–0.3 to 0.3	V
Permissable loss		P_D	250	mW
Operating temperature		T_{opr}	–30 to 85	°C
Storage temperature	FP	T_{stg}	–65 to 150	°C
	Die		–55 to 125	
Soldering temperature		T_{sol}	260°C for 10s (at the leads)	

- **DC Characteristics**

(V_{DD} = 0V, T_a = –20 to 75°C)

Parameter		Symbol	Condition	Applicable Terminals	Min	Typ	Max	Unit
Operating voltage (1)*1	Recommended operation	V_{SS}		V_{SS}	–5.5	–5.0	–4.5	V
	Potential operation				–7.0	—	–2.4	
Operating voltage (2)	Recommended operation	V_5		V_5	–13.0	—	–3.5	V
	Potential operation				–13.0	—	—	
	Potential operation	V_1, V_2		V_1, V_2	0.6×V_5	—	V_{DD}	
	Potential operation	V_3, V_4		V_3, V_4	V_5	—	0.4×V_5	
HIGH input voltage		V_{IHT}		A0, D0~D7, E, R/$\overline{W}$, $\overline{CS}$	V_{SS}+2.0	—	V_{DD}	V
		V_{IHC}		CL, FR, M/S, $\overline{RES}$	0.2×V_{SS}	—	V_{DD}	
		V_{IHT}	V_{SS}= –3V	A0, D0~D7, E, R/$\overline{W}$, $\overline{CS}$	0.2×V_{SS}	—	V_{DD}	V
		V_{IHC}	V_{SS}= –3V	CL, FR, M/S, $\overline{RES}$	0.2×V_{SS}	—	V_{DD}	
LOW input voltage		V_{ILT}		A0, D0~D7, E, R/$\overline{W}$, $\overline{CS}$	V_{SS}	—	V_{SS}+0.8	V
		V_{ILC}		CL, FR, M/S, $\overline{RES}$	V_{SS}	—	0.8×V_{SS}	
		V_{ILT}	V_{SS}= –3V	A0, D0~D7, E, R/$\overline{W}$, $\overline{CS}$	V_{SS}	—	0.85×V_{SS}	V
		V_{ILC}	V_{SS}= –3V	CL, FR, M/S, $\overline{RES}$	V_{SS}	—	0.8×V_{SS}	
HIGH output voltage		V_{OHT}	I_{OH}= –3mA	D0~D7	V_{SS}+2.4	—	—	V
		V_{OHC1}	I_{OH}= –2mA	FR	V_{SS}+2.4	—	—	
		V_{OHC2}	I_{OH}= –120µA	OSC2	0.2×V_{SS}	—	—	
		V_{OHT}	V_{SS}= –3V I_{OH}= –2mA	D0~D7	0.2×V_{SS}	—	—	V
		V_{OHC1}	V_{SS}= –3V I_{OH}= –2mA	FR	0.2×V_{SS}	—	—	
		V_{OHC2}	V_{SS}= –3V I_{OH}= –50µA	OSC2	0.2×V_{SS}	—	—	
LOW output voltage		V_{OLT}	I_{OL}=3mA	D0~D7	—	—	V_{SS}+0.4	V
		V_{OLC1}	I_{OL}=2mA	FR	—	—	V_{SS}+0.4	
		V_{OLC2}	I_{OL}=120µA	OSC2	—	—	0.8×V_{SS}	
		V_{OLT}	V_{SS}= –3V I_{OL}=2mA	D0~D7	—	—	0.8×V_{SS}	V
		V_{OLC1}	V_{SS}= –3V I_{OL}=2mA	FR	—	—	0.8×V_{SS}	
		V_{OLC2}	V_{SS}= –3V I_{OL}=50µA	OSC2	—	—	0.8×V_{SS}	
Input leak current		I_{LI}		A0,E,R/$\overline{W}$,$\overline{CS}$,CL,$\overline{RES}$,MS pins	–1.0	—	1.0	µA
Output leak current		I_{LO}	Applicable when FR is in a high-impedance state	D0~D7, FR pins	–3.0	—	3.0	
LCD driver ON resistance		R_{ON}	T_a=25°C V_5= –5.0V	SEG0~68	—	5.0	7.5	kΩ
			T_a=25°C V_5= –3.5V	COM0~7	—	10.0	50.0	
Static current consumption		I_{DDQ}	$\overline{CS}$=CL=V_{DD}	V_{DD}	—	0.05	1.0	
Active current consumption	External CLK	$I_{DD(1)}$	During display V_5= –5V f_{CL}=2kHz	V_{DD}	—	2.0	5.0	µA
	Oscillator		During display V_5= –5V R_f=1MΩ		—	9.5	15.0	
	External CLK		During display V_5= –5V,V_{SS}= –3V f_{CL}=2kHz	V_{DD}	—	1.5	4.5	µA
	Oscillator		During display V_5= –5V,V_{SS}= –3V R_f=1MΩ		—	6.0	12.0	
		$I_{DD(2)}$	During access t_{cyc}=200kHz		—	300	500	µA
			V_{SS}= –3V, During access t_{cyc}=200kHz		—	150	300	
Input terminal capacity		C_{IN}	T_a=25°C, f=1MHz	All input terminals	—	5.0	8.0	pF
Oscillating frequency		f_{OSC}	R_f=1.0MΩ±2%, V_{SS}= –5.0V		15	18	21	kHz
			R_f=1.0MΩ±2%, V_{SS}= –3.0V		11	16	21	
Reset time		t_R		$\overline{RES}$	1.0	—	1000	µs

*1. A wide range of operating voltages is guaranteed, except in case of abrupt voltage fluctuations during MPU access.

AC Characteristics

Read/Write timing for the 80-port MPU

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

Parameter	Signal	Symbol	Condition	Min	Typ	Max	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}		10	—	—	ns
Address set-up time		t_{AW8}		20	—	—	ns
System cycle time	$\overline{WR}$, $\overline{RD}$	t_{CYC8}		1000	—	—	ns
Control pulse width		t_{CC}		200	—	—	ns
Data set-up time	D0~D7	t_{DS8}		80	—	—	ns
Data hold time		t_{DH8}		10	—	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	—	90	ns
Output disable time		t_{OH8}		10	—	60	ns

*2. The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

*3. The rise or fall time of input signals should be less than 15ns.

Read/Write timing for the 68-port MPU

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

Parameter		Signal	Symbol	Condition	Min	Typ	Max	Unit
System cycle time		A0, $\overline{CS}$ R/$\overline{W}$	t_{CYC6} *4		1000	—	—	ns
Address set-up time			t_{AW6}		20	—	—	ns
Address hold time			t_{AH6}		10	—	—	ns
Data set-up time		D0~D7	t_{DS6}		80	—	—	ns
Data hold time			t_{DH6}		10	—	—	ns
Output disable time			t_{OH6}	C_L=100pF	10	—	60	ns
Access time			t_{ACC6}		—	—	90	ns
Enable pulse width	READ	E	t_{EW}		100	—	—	ns
	WRITE				80	—	—	ns

*4 t_{CYC6} indicates the cycle during which $\overline{CS}$/E are HIGH; it does not indicate the cycle of the E signal.

*5 The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

*6 The rise or fall time of input signals should be less than 15ns.

Control timing for 80-port/68-port display

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

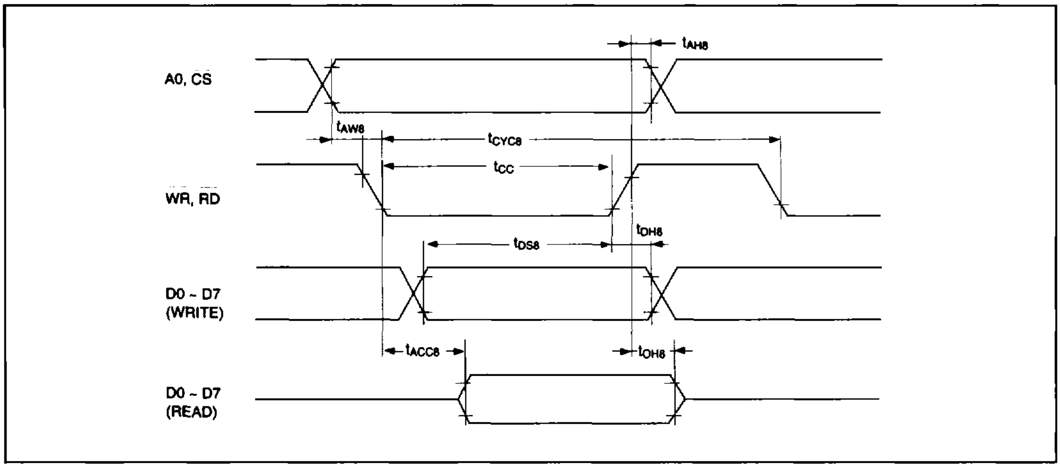
Parameter	Signal	Symbol	Condition	Min	Typ	Max	Unit
LOW pulse width	C_L	t_{WLCL}	(Input timing)	35	—	—	µs
HIGH pulse width		t_{WHCL}		35	—	—	µs
Rising time		t_r		—	30	150	ns
Falling time		t_f		—	30	150	ns
FR delay time	FR	t_{DFR}	(Input timing)	–2.0	0.2	2.0	µs
			(Output timing), C_L=100pF	—	0.2	0.4	µs

*7. The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

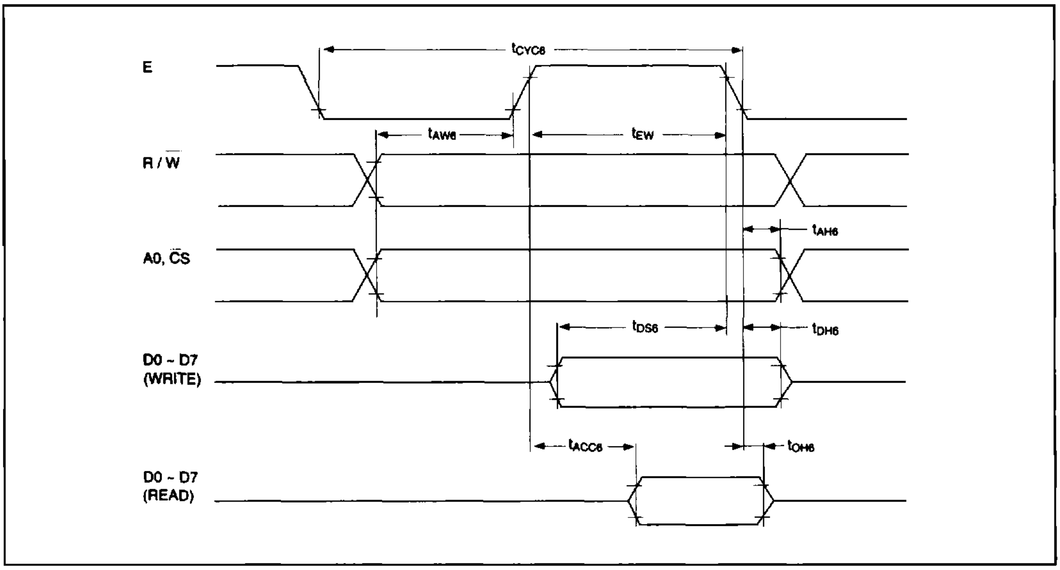
*8. The input timing of the FR delay time is determined by the SED1522 (Slave).
The output timing of the FR delay time is determined by the SED1522 (Master).

● Timing Chart

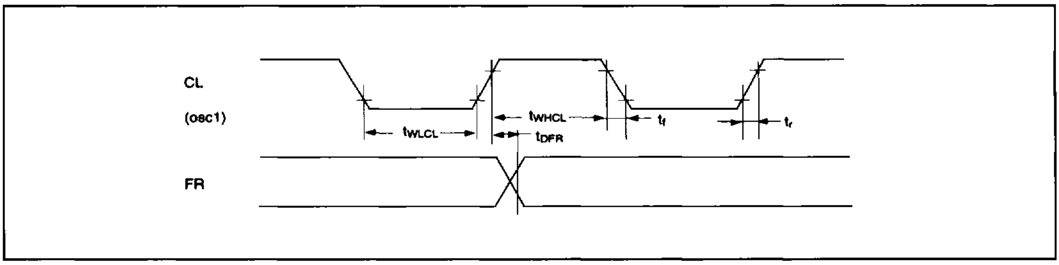
○ Read/Write timing for the 80-port MPU



○ Read/Write timing for the 68-port MPU



○ Control timing for 80-port/68-port display



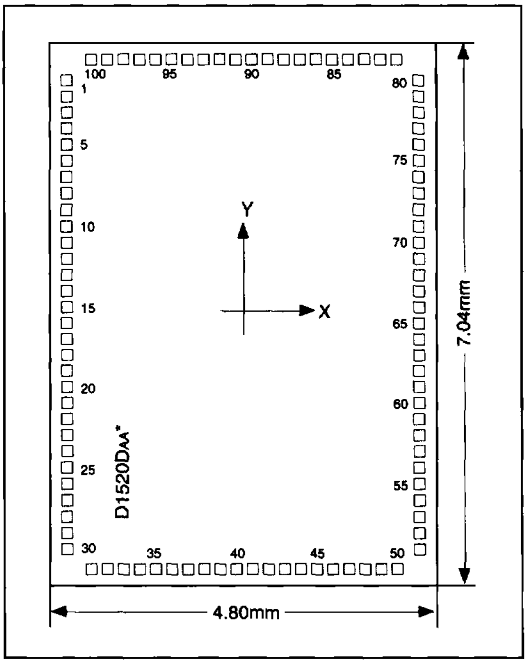
DISPLAY COMMANDS

(Based on the 80-port MPU; the $\overline{RD}$ and $\overline{WR}$ commands differ for the 68-port MPU)

Command		$\overline{RD}$	$\overline{WR}$	A0	D7	D6	D5	D4	D3	D2	D1	D0	Function	
1	Display ON/OFF	1	0	0	1	0	1	0	1	1	1	0/1	Switches the entire display ON or OFF, regardless of the Display RAM's data or the internal status.	
2	Display START Line	1	0	0	1	1	0	Display START address (0~31)					Determines the line of RAM data to be displayed at the display's top line (COM0).	
3	Page Address Set	1	0	0	1	0	1	1	1	0	Page (0~3)		Sets the page of the Display RAM in the page address register.	
4	Column (Segment) Address Set	1	0	0	0	Column address (0~79)							Sets the column address of the Display RAM in the column address register.	
5	Status Read	0	1	0	BUSY	ACC	ON/OFF	RESET	0	0	0	0	Reads the status. BUSY 1: Busy (internal processing) 0: READY status ADC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting 0: Normal	
6	Write Display Data	1	0	1	Write Data								Writes the data on the data bus to RAM	These commands access a previously-specified address of the Display RAM, after which the column address is incremented by one.
7	Read Display Data	0	1	1	Read Data								Reads data from the Display RAM onto the data bus.	
8	ADC Select	1	0	0	1	0	1	0	0	0	0	0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse) output	
9	Static Drive ON/OFF	1	0	0	1	0	1	0	0	1	0	0/1	Selects normal display operation or static all-lit drive display operation. 1: Static drive (Power Save) *9 0: Normal display operation	
10	Duty Select	1	0	0	1	0	1	0	1	0	0	0/1	Selects the duty factor for driving LCD cells. 1: 1/16 duty 0: 1/8 duty	
11	Read Modify Write	1	0	0	1	1	1	0	0	0	0	0	Increments the column address counter by one only when display data is written but not when it is read.	
12	End	1	0	0	1	1	1	0	1	1	1	0	Cancels the Ready Modify Write mode.	
13	Reset	1	0	0	1	1	1	0	0	0	1	0	Resets the Display START line to the 1st line in the register. Resets the column address counter to 0 and sets page address register to 3.	

*9. Power Save mode is entered by selecting static drive in Display OFF status.

■ PAD LAYOUT



○ **Aluminum pad chip specifications**

Chip dimensions:	4.80 × 7.04 × 0.40mm
Pad surface area:	100 × 100µm

○ **Gold bump chip specifications (reference only)**

Minimum bump pitch:	199µm
Bump height:	20^{+10}_{-5} µm
Bump size:	132 × 111 µm (±20 µm)
Chip dimensions:	4.80 × 7.04 × 0.525mm

* The die shown is the SED1522DAA. The final A in the suffix indicates that the device is an aluminum pad product. Bump chip products share the same die part number as aluminum products; however, the last letter of the suffix is B.

PAD COORDINATES

Pin names are for the SED1522DAA/SED1522DAB, and those in brackets for the SED1522DOA/SED1522DOB.

Pad No.	Pin Name	X	Y
1	COM5	159	6507
2	COM6	159	6308
3	COM7	159	6108
4	SEG68	159	5909
5	SEG67	159	5709
6	SEG66	159	5510
7	SEG65	159	5310
8	SEG64	159	5111
9	SEG63	159	4911
10	SEG62	159	4712
11	SEG61	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	$\overline{\text{CS}}$ (OSC1)	4641	5247
75	CL (OSC2)	4641	5447
76	E ($\overline{\text{RD}}$)	4641	5646
77	R/W ($\overline{\text{WR}}$)	4641	5846
78	V_{SS}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{\text{RES}}$	2898	6884
89	FR	2699	6884
90	V5	2499	6884
91	V3	2300	6884
92	V2	2100	6884
93	M/S	1901	6884
94	V4	1701	6884
95	V1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	COM4	504	6884

Note: Values in the properties table are specified as Max or Min according to the comparison on the numerical coordinates.

All specifications of this device are subject to change without notice.