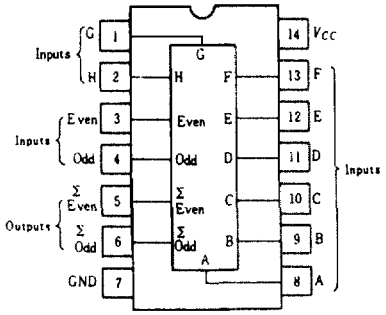
HD74HC180 ● 8-bit Odd/Even Parity Generator/Checker

This universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generator/checker features odd/even outputs and control inputs to facilitate operation in either odd or even parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

■FEATURES

- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

■PIN ARRANGEMENT



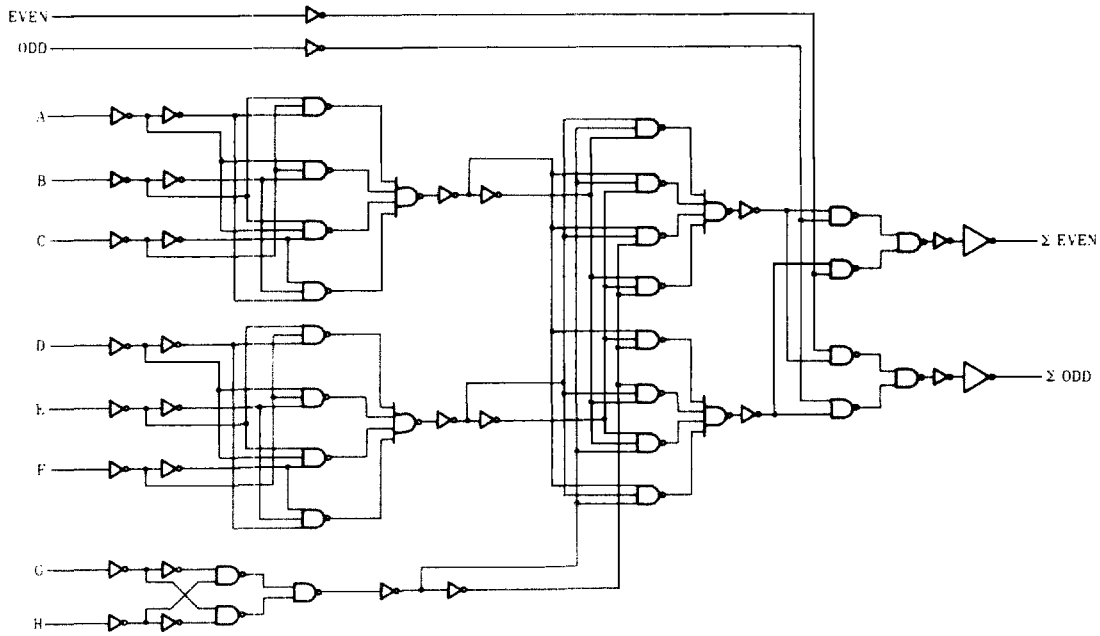
(Top View)

■ FUNCTION TABLE

Inputs			Outputs	
Σ Of H's at A Thru H	Even	Odd	Σ Even	Σ Odd
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = high level, L = low level, X = irrelevant

■ LOGIC DIAGRAM



■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		T_a=25°C min	T_a=25°C typ	T_a=25°C max	T_a=−40~+85°C min	T_a=−40~+85°C max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH}=−4mA	4.18	—	—	4.13	—	
		6.0		I_{OH}=−5.2mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL}=4mA	—	—	0.26	—	0.33	
		6.0		I_{OL}=5.2mA	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	T_a=25°C min.	T_a=25°C typ.	T_a=25°C max.	T_a=−40~+85°C min.	T_a=−40~+85°C max.	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	Data (Odd=0) to Σ Even	—	—	260	—	325	ns
		4.5		—	28	52	—	65	
		6.0		—	—	44	—	55	
	t_{PLH} t_{PHL}	2.0	Data (Odd=0) to Σ Odd	—	—	245	—	305	ns
		4.5		—	28	49	—	61	
		6.0		—	—	42	—	52	
	t_{PLH} t_{PHL}	2.0	Data (Even=0) to Σ Even	—	—	260	—	325	ns
		4.5		—	28	52	—	65	
		6.0		—	—	44	—	55	
	t_{PLH} t_{PHL}	2.0	Data (Even=0) to Σ Odd	—	—	245	—	305	ns
		4.5		—	28	49	—	61	
		6.0		—	—	42	—	52	
	t_{PLH} t_{PHL}	2.0	Even or Odd to Σ Even or Σ Odd	—	—	110	—	140	ns
		4.5		—	13	22	—	28	
		6.0		—	—	19	—	24	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	7	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF