# MILITARY DRAM

# 64K x 4 DRAM

## AVAILABLE AS MILITARY SPECIFICATION

- SMD 5962-87676
- MIL-STD-883, Class B

## FEATURES

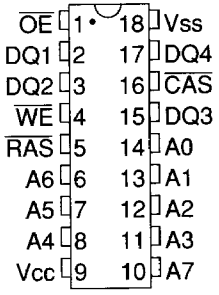
- Industry standard pinout and timing
- All inputs, outputs and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby; 150mW active, typical
- Optional PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, and HIDDEN
- 256-cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +110°C)

## OPTIONS

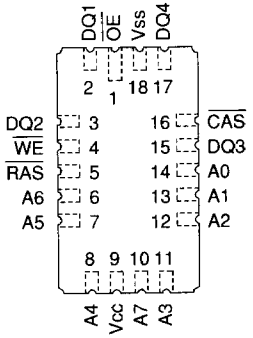
| OPTIONS | MARKING |
|---|---|
| • Timing | |
| 100ns access | -10 |
| 120ns access | -12 |
| 150ns access | -15 |
| • Packages | |
| Ceramic DIP | C |
| Ceramic LCC | EC |

## PIN ASSIGNMENT (Top View)

### 18L/300 DIP
(D-6)




### 18L/LCC

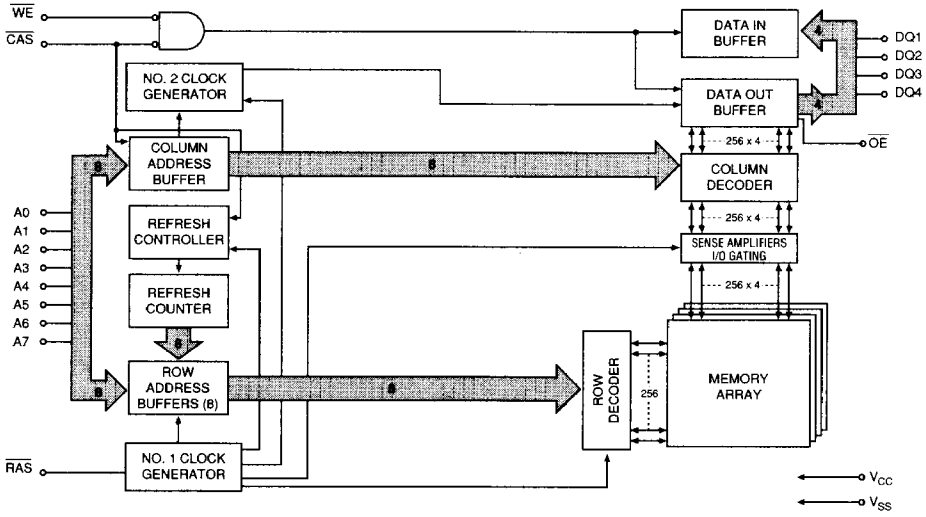



## GENERAL DESCRIPTION

The MT4067 883C is a randomly accessed solid-state memory containing 262,144 bits organized in a 65,536 x4 configuration. The 16 address bits are entered 8 bits at a time using $\overline{RAS}$ to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits. If $\overline{WE}$ goes LOW after data reaches the output pins, the output pins are activated and retain the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-MODIFY-WRITE cycle. Data in is latched when $\overline{WE}$ strobes LOW.

By holding $\overline{RAS}$ LOW, $\overline{CAS}$ may be toggled to execute several faster READ, WRITE or READ-MODIFY-WRITE cycles within the $\overline{RAS}$ address defined page boundary. Returning $\overline{RAS}$ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing a $\overline{RAS}$ (READ, WRITE, $\overline{RAS}$-ONLY or HIDDEN REFRESH) cycle so that all 256 combinations of $\overline{RAS}$ addresses are executed at least every 4ms (regardless of sequence).

## FUNCTIONAL BLOCK DIAGRAM
PAGE MODE




## TRUTH TABLE

| Function | RAS | CAS | WE | OE | Addresses tR | Addresses tC | |
|---|---|---|---|---|---|---|---|
| Standby | H | H | H | H | X | X | High-Z |
| READ | L | L | H | L | ROW | COL | Data Out |
| WRITE (EARLY-WRITE) | L | L | L | X | ROW | COL | Data In |
| READ-WRITE | L | L | H→L→H | L→H | ROW | COL | Data Out, Data In |
| PAGE-MODE READ | L | H→L→H | H | L | ROW | COL | Data Out, Data Out |
| PAGE-MODE WRITE | L | H→L→H | L | X | ROW | COL | Data In, Data In |
| PAGE-MODE READ-WRITE | L | H→L→H | H→L→H | L→H | ROW | COL | Data Out, Data In |
| RAS-ONLY REFRESH | L | H | X | H | ROW | n/a | High-Z |
| HIDDEN REFRESH | L→H→L | L | H | L | ROW | COL | Data Out |
| CAS-BEFORE-RAS REFRESH | H→L | L | X | X | X | X | High-Z |

## ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1.5V to +7.0V
Storage Temperature Range ..... -65°C to +150°C
Power Dissipation ..... 1W
Lead Temperature (soldering 5 seconds) ..... 300°C
Junction Temperature (Tj) ..... +150°C
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL PERFORMANCE CHARACTERISTICS

(Notes: 4, 6, 7) (-55°C ≤ $T_C$ ≤ +110°C; Vcc = 5.0V ±10%)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Supply Current from Vcc (Active); $\overline{RAS}$ and $\overline{CAS}$ Cycling; $^tRC$ = $^tRC$ (MIN) | Icc1 | | 55 | mA | 2 |
| Supply Current from Vcc (Active, PAGE MODE); $\overline{RAS}$ = VIL, $\overline{CAS}$ Cycling; $^tPC$ = $^tPC$ (MIN) | Icc2 | | 55 | mA | 2 |
| Supply Current from Vcc (Standby); $\overline{RAS}$ and $\overline{CAS}$ = VIH | Icc3 | | 8 | mA | |
| Supply Current from Vcc (REFRESH, $\overline{RAS}$-ONLY); $\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH | Icc4 | | 45 | mA | 2 |
| Supply Current from Vcc (REFRESH, $\overline{CAS}$-BEFORE-$\overline{RAS}$); $\overline{RAS}$ and $\overline{CAS}$ Cycling | Icc5 | | 55 | mA | 2 |
| Output High Voltage (IOH = -5mA) | VOH | 2.4 | | V | 1 |
| Output Low Voltage (IOL = 5mA) | VOL | | 0.4 | V | 1 |
| Input Leakage | IIH | -10 | 10 | µA | |
| Any Input (0V ≤ VIN ≤ Vcc); All Other Pins = 0V | IIL | -10 | 10 | µA | |
| Output Leakage (0 ≤ VOUT ≤ Vcc) | IOZ | -10 | 10 | µA | |

## DC OPERATING CONDITIONS

(Notes: 4, 6, 7) (-55°C ≤ $T_C$ ≤ +110°C; Vcc = 5.0V ±10%)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Vcc Supply Voltage | Vcc | 4.5 | 5.5 | V | |
| Vss Power Supply and Signal Reference | Vss | 0.0 | 0.0 | V | 1 |
| High-Level Input Voltage (All Inputs) | VIH | 2.4 | Vcc+1 | V | 1 |
| Low-Level Input Voltage (All Inputs) | VIL | -1.0 | 0.8 | V | 1 |

## CAPACITANCE

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance: (A0-A7) | CI1 | | 5 | pF | 3 |
| Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | CI2 | | 8 | pF | 3 |
| Input/Output Capacitance: (DQ1-DQ4) | CO | | 7 | pF | 3 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

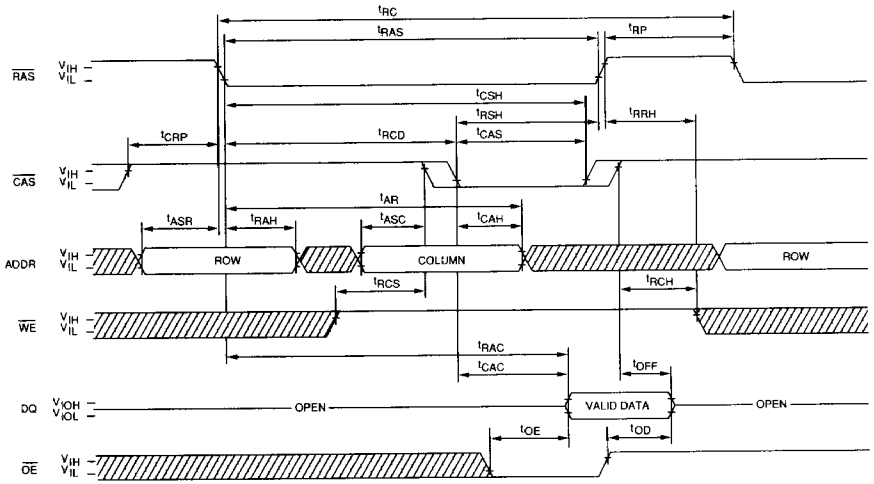
(Notes: 4, 5, 6, 7, 8) (-55°C ≤ $T_C$ ≤ +110°C; Vcc = 5.0V ±10%)

| AC CHARACTERISTICS | | -10 | | -12 | | -15 | | | |
|---|---|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Random READ or WRITE cycle time | tRC | 195 | | 220 | | 250 | | ns | |
| READ-MODIFY-WRITE cycle time | tRWC | 250 | | 290 | | 315 | | ns | 20 |
| PAGE-MODE cycle time | tPC | 90 | | 100 | | 120 | | ns | 20 |
| Access time from $\overline{RAS}$ | tRAC | | 100 | | 120 | | 150 | ns | 9 |
| Access time from $\overline{CAS}$ | tCAC | | 50 | | 60 | | 75 | ns | 10 |
| $\overline{RAS}$ pulse width | tRAS | 100 | 10,000 | 120 | 10,000 | 150 | 10,000 | ns | |
| $\overline{CAS}$ pulse width | tCAS | 50 | 10,000 | 60 | 10,000 | 75 | 10,000 | ns | |
| $\overline{RAS}$ precharge time | tRP | 80 | | 80 | | 90 | | ns | |
| $\overline{RAS}$ hold time | tRSH | 50 | | 60 | | 75 | | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | tRCD | 25 | 50 | 30 | 60 | 30 | 75 | ns | 16 |
| $\overline{CAS}$ precharge time | tCPN | 25 | | 25 | | 30 | | ns | 20 |
| $\overline{CAS}$ precharge time (PAGE MODE) | tCP | 30 | | 30 | | 35 | | ns | 11 |
| $\overline{CAS}$ to $\overline{RAS}$ setup time | tCRP | 5 | | 5 | | 5 | | ns | |
| $\overline{CAS}$ hold time | tCSH | 110 | | 120 | | 150 | | ns | |
| Row address setup time | tASR | 0 | | 0 | | 0 | | ns | 20 |
| Row address hold time | tRAH | 15 | | 20 | | 20 | | ns | |
| Column address setup time | tASC | 0 | | 0 | | 0 | | ns | 20 |
| Column address hold time | tCAH | 20 | | 30 | | 30 | | ns | |
| Column address hold time referenced to $\overline{RAS}$ | tAR | 70 | | 80 | | 100 | | ns | |
| Read command setup time | tRCS | 0 | | 0 | | 0 | | ns | 20 |
| Read command hold time referenced to $\overline{CAS}$ | tRCH | 0 | | 0 | | 0 | | ns | 20 |
| Read command hold time referenced to $\overline{RAS}$ | tRRH | 10 | | 10 | | 10 | | ns | |
| Output disable delay | tOFF | 0 | 40 | 0 | 40 | 0 | 40 | ns | 12 |
| Output disable | tOD | | 35 | | 40 | | 40 | ns | |
| Output enable | tOE | | 25 | | 25 | | 30 | ns | 13 |
| Write command setup time | tWCS | 0 | | 0 | | 0 | | ns | 14 |
| Write command hold time | tWCH | 35 | | 40 | | 45 | | ns | |
| Write command hold time referenced to $\overline{RAS}$ | tWCR | 85 | | 100 | | 120 | | ns | |
| Write command pulse width | tWP | 35 | | 40 | | 45 | | ns | |
| Write command to $\overline{RAS}$ lead time | tRWL | 35 | | 40 | | 45 | | ns | |
| Write command to $\overline{CAS}$ lead time | tCWL | 35 | | 40 | | 45 | | ns | |
| Data-in setup time | tDS | 0 | | 0 | | 0 | | ns | 15, 20 |
| Data-in hold time | tDH | 35 | | 35 | | 45 | | ns | 15 |
| Data-in hold time referenced to $\overline{RAS}$ | tDHR | 85 | | 100 | | 120 | | ns | |
| $\overline{CAS}$ to write delay | tCWD | 70 | | 90 | | 110 | | ns | 14 |
| $\overline{RAS}$ to write delay | tRWD | 120 | | 150 | | 185 | | ns | 14 |
| Transition time (rise or fall) | tT | 3 | 100 | 3 | 100 | 3 | 100 | ns | 20 |
| $\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH) | tCSR | 10 | | 10 | | 10 | | ns | 17 |
| $\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH) | tCHR | 20 | | 25 | | 30 | | ns | 17 |
| Refresh period (256 cycles distributed) | tREFD | | 4 | | 4 | | 4 | ms | 18 |
| Refresh period (256 cycles burst) | tREFB | | 4 | | 4 | | 4 | ms | 19 |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | tRPC | 0 | | 0 | | 0 | | ns | 20 |

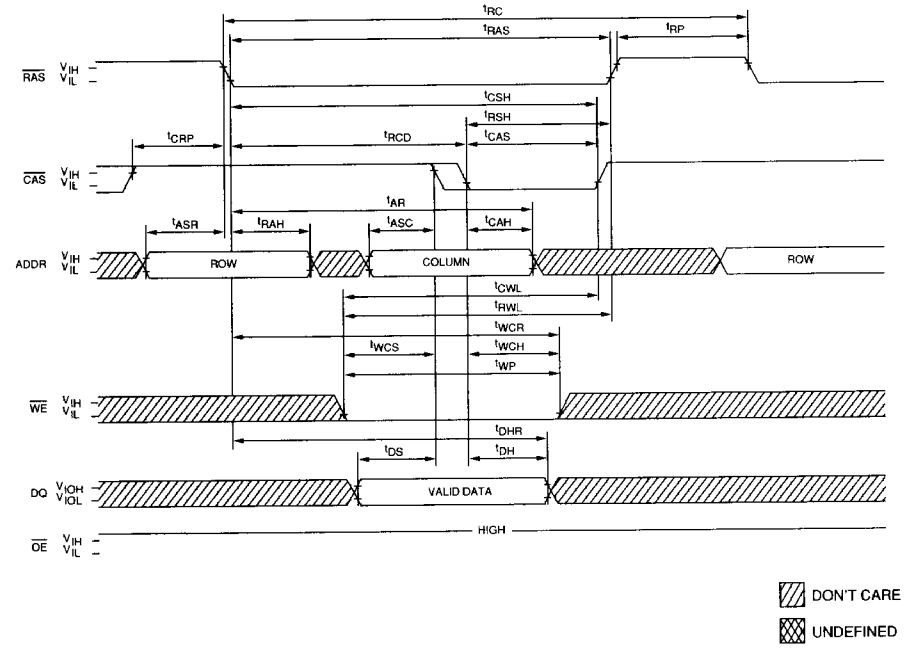
## NOTES

1. $V_{SS}$ is common for all voltages.
2. Specified values are obtained with the output load equal to 2TTL loads and 100pF to $V_{SS}$.
3. This parameter is sampled, not 100% tested. Capacitance is measured with Vcc = 5.0V, f = 1MHz at less than 50mVrms, $T_A$ = 25°C ± 3°C, Vbias = 2.4V applied to each input and output individually with remaining inputs and outputs open.
4. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles, (READ, WRITE, READ-MODIFY-WRITE, $\overline{RAS}$ REFRESH) before proper device operation is assured.
5. AC characteristics assume transition time ($^tT$) = 5ns. This parameter is not measured.
6. $V_{IL}$ (MAX) and $V_{IH}$ (MIN) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IL}$ and $V_{IH}$.
7. In addition to meeting the transition rate specification, all input signals must transit between $V_{IL}$ and $V_{IH}$ (or between $V_{IH}$ and $V_{IL}$) in a monotonic manner.
8. If $\overline{CAS}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$, DQs are High-Z. If $\overline{CAS}$ = $V_{IL}$, and $\overline{OE}$ = $V_{IL}$, DQs may contain data from the last valid READ cycle.
9. Assumes that $^tRCD < {}^tRCD$ (MAX).
10. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
11. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, DQs will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{CAS}$ must be pulsed HIGH for $^tCP$. Note 8 applies to determine valid data out.
12. $^tOFF$ (MAX) defines the time at which the outputs achieve the open circuit condition. $^tOFF$ (MAX) is not referenced to $V_{OH}$ or $V_{OL}$.
13. If $\overline{OE}$ is taken LOW then HIGH, DQs go open. If $\overline{OE}$ is tied permanently LOW a READ-WRITE or READ-MODIFY-WRITE operation requires a separate READ and WRITE cycle.
14. $^tWCS$, $^tCWD$ and $^tRWD$ are restrictive operating parameters in the READ-MODIFY-WRITE cycle only. If $^tWCS \geq {}^tWCS$ (MIN) the cycle is an EARLY-WRITE cycle and the DQs will remain open circuit throughout the entire cycle. If $^tCWD \geq {}^tCWD$ (MIN) and $^tRWD \geq {}^tRWD$ (MIN) the cycle is a READ-WRITE and the DQs will contain data read from the selected address. When performing LATE-WRITE cycle $^tWCS$, $^tCWD$ and $^tRWD$ do not apply.
15. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and to the $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
16. Operation within the $^tRCD$ (MAX) limit ensures that $^tRAC$ (MAX) can be met. $^tRCD$ (MAX) is specified as a reference point only; if $^tRCD$ is greater than the specified $^tRCD$ (MAX) limit, then access time is controlled exclusively by $^tCAC$.
17. Enables on-chip refresh and address counters.
18. A 256-cycle distributed refresh consists of an address location refresh cycle being performed within 15.625µS so that all 256 $\overline{RAS}$ address combinations are executed within 4ms (regardless of sequence). Micron recommends distributed refresh.
19. A 256-cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of $\overline{RAS}$ addresses (regardless of sequence). The refresh mode must be executed within 4ms.
20. This parameter is a "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, with several other parameters, in the performance verification of other attributes.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.

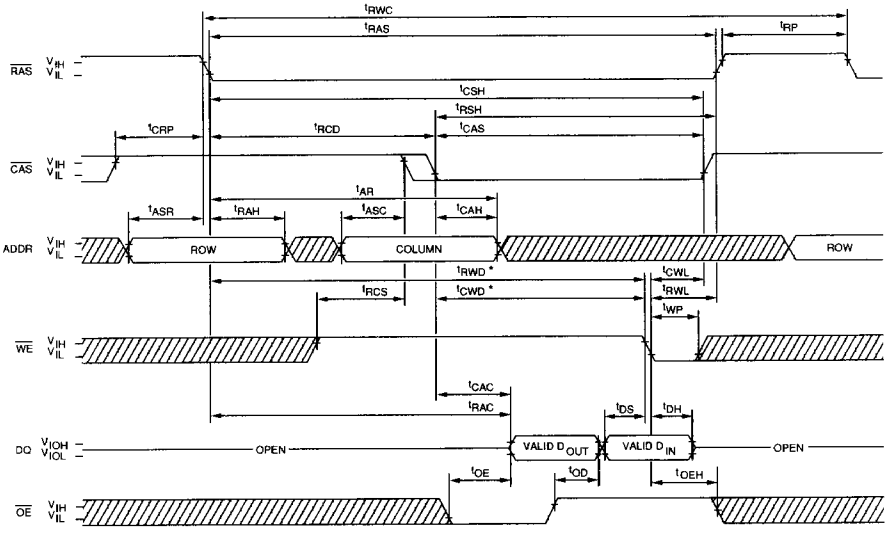
## READ CYCLE




## EARLY-WRITE CYCLE
($\overline{OE}$ = DON'T CARE)

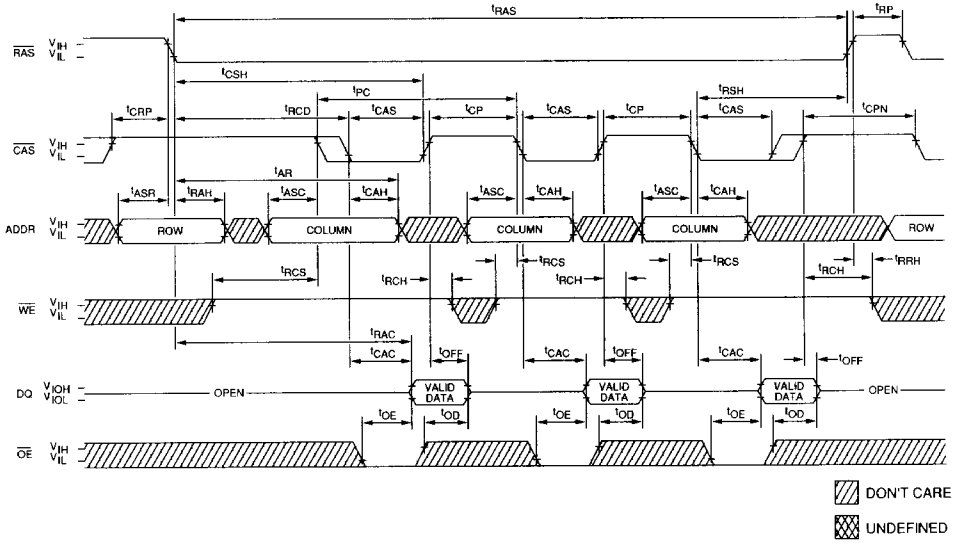


## READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

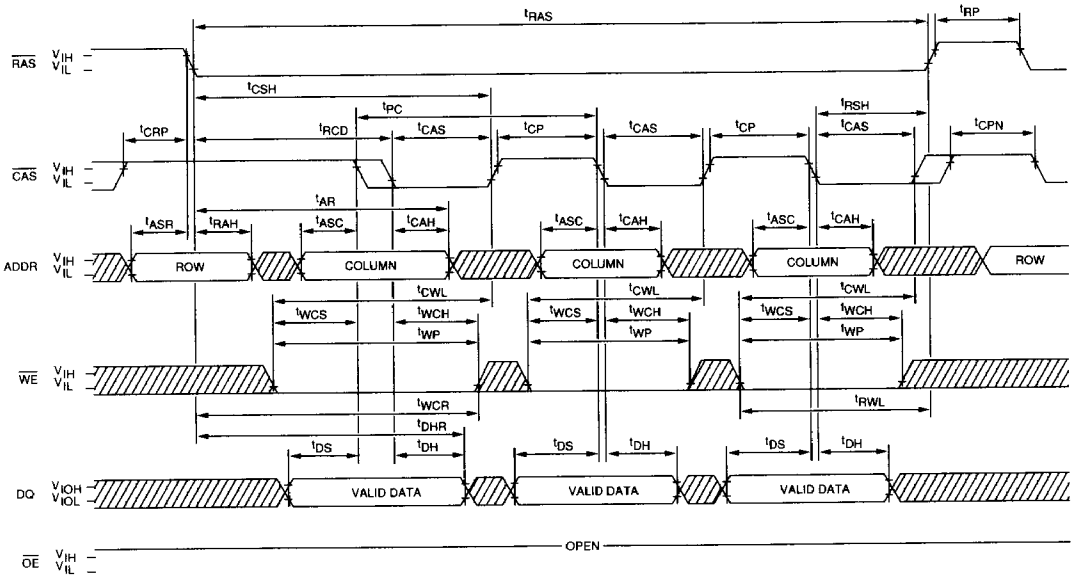



*Not required for LATE-WRITE cycle

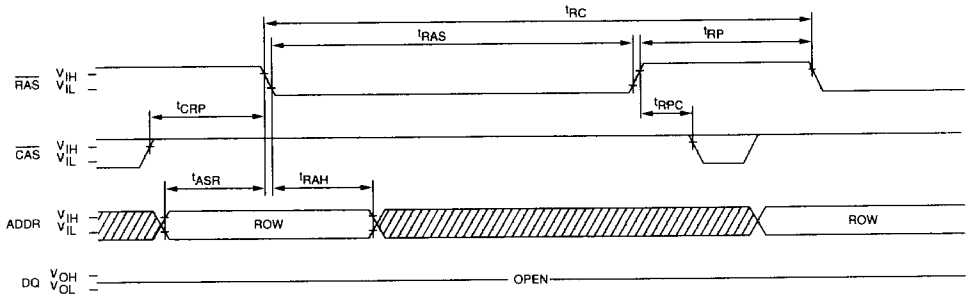
## PAGE-MODE READ CYCLE



## PAGE-MODE EARLY-WRITE CYCLE
($\overline{OE}$ = DON'T CARE)

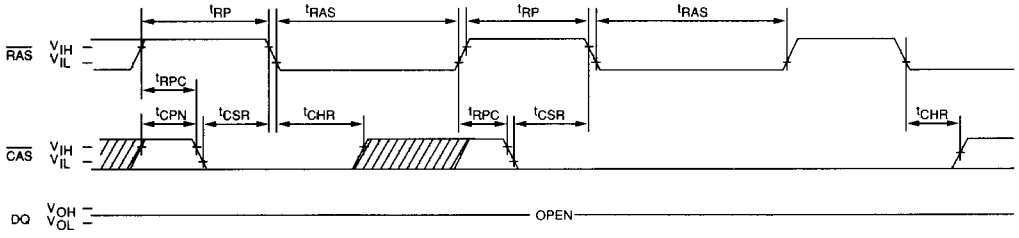



## $\overline{RAS}$-ONLY REFRESH CYCLE
(ADDR = A0-A7; $\overline{WE}$ = DON'T CARE)



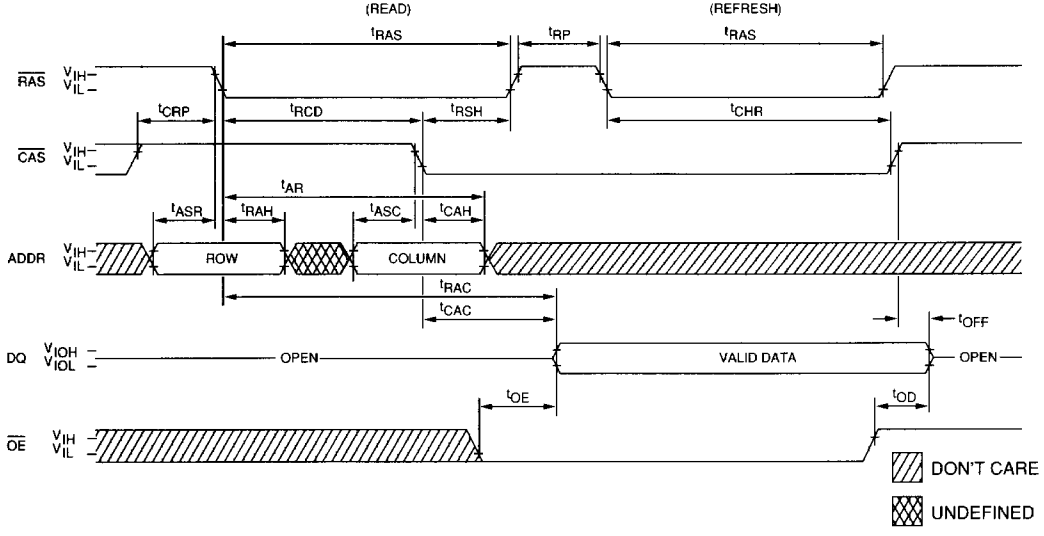
## CAS-BEFORE-RAS REFRESH CYCLE

(A0-A7; WE, OE = DON'T CARE)




## HIDDEN REFRESH CYCLE

(WE = HIGH) [21]



## ELECTRICAL TEST REQUIREMENTS

| MIL-STD-883 TEST REQUIREMENTS | SUBGROUPS (per Method 5005, Table I) |
|---|---|
| INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004) | 2, 8A, 10 |
| FINAL ELECTRICAL TEST PARAMETERS (Method 5004) | 1*, 2, 3, 7*, 8, 9, 10, 11 |
| GROUP A TEST REQUIREMENTS (Method 5005) | 1, 2, 3, 4**, 7, 8, 9, 10, 11 |
| GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005) | 1, 2, 3, 7, 8, 9, 10, 11 |

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes which may affect input or output capacitance.