Signetics

Document No.	853-0030
ECN No.	97679
Date of issue	September 20, 1989
Status	Product Specification
FAST Products	

FAST 74F605

Latch

Dual Octal Latch (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F605	10.0ns	85mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20µA in High and Low states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **Open Collector outputs**
- **Propagation delay 10ns typical**
- **Power supply current 85mA typical**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F605N
28-Pin Plastic SOL	N74F605D

DESCRIPTION

The 74F605 multiplexed latch is ideal for storing data from two input buses, A or B, and providing data from either the A or B latches to the ouput bus. Organized as 8-bit A and B latches, thelatch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT A/$\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight Open Collector outputs. Data entered from the B inputs are selected when SELECT A/$\overline{B}$ is Low; data from the A inputs are selected when SELECT A/$\overline{B}$ is High. Data enters the latches when the Latch Enable ($\overline{LE}$) input is Low and is latched on the $\overline{LE}$ rising edge. The outputs are enabled when $\overline{LE}$ is High and disabled when $\overline{LE}$ is Low.

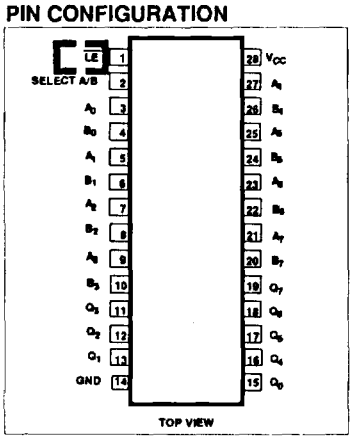
These functions are also well-suited for receiving 16-bit simultaneous data and transmitting it as two sequential 8-bit words.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

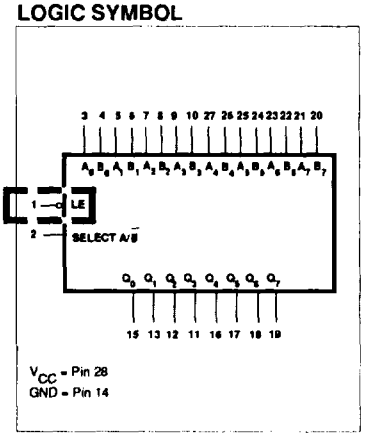
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	1.0/0.033	20µA/20µA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20µA/20µA
$\overline{LE}$	Latch Enable Input (active Low)	1.0/0.033	20µA/20µA
O_0-O_7	Data outputs	OC/40	OC/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC = Open Collector

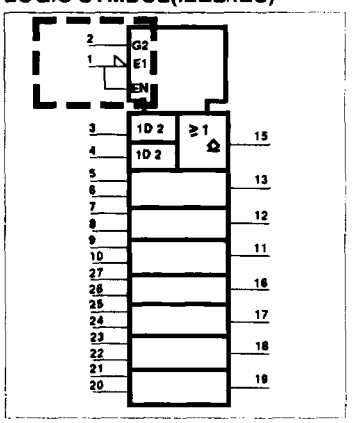
PIN CONFIGURATION



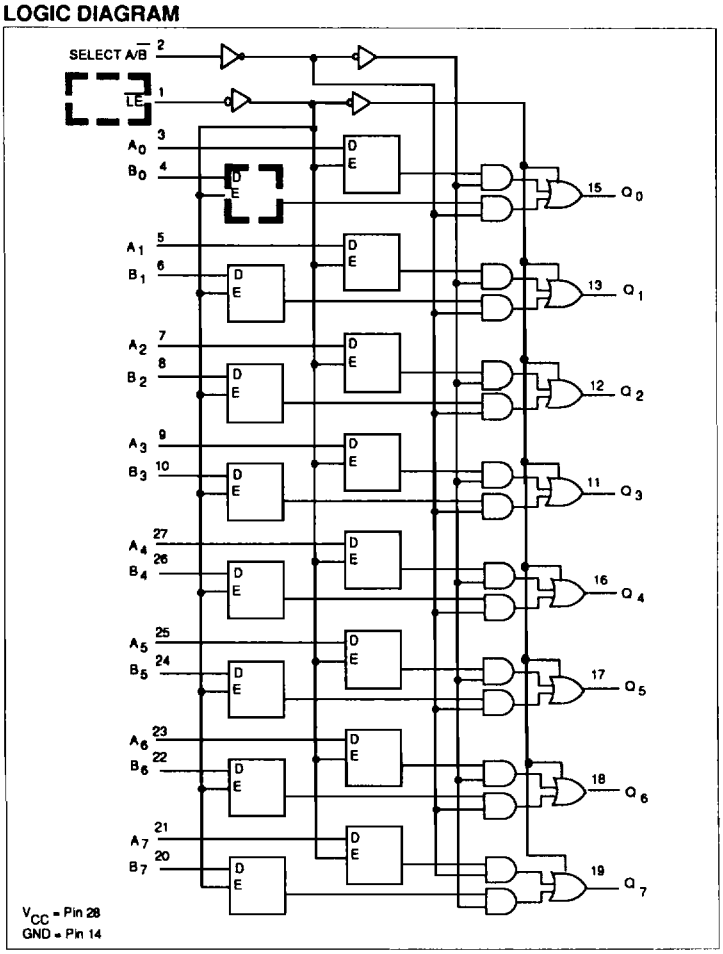
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
A_0-A_7	B_0-B_7	SELECT A/$\overline{B}$	$\overline{LE}$	Q_0-Q_7
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	OFF
X	X	L	H	B latched data
X	X	H	H	A latched data

H = High voltage level
L = Low voltage level
X = Don't care
OFF= Pulled up through resistor (open collector)
↑ =Low-to-High transition

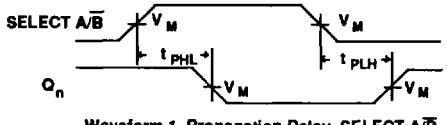
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (B latch)	Waveform 2	7.5 7.5	9.5 10.0	11.5 12.0	7.0 7.0	12.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (A latch)	Waveform 1	8.5 6.5	11.0 8.5	13.0 11.0	8.0 6.0	14.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to Q_n	Waveform 3	8.5 6.5	11.0 9.0	13.0 11.0	8.0 6.0	14.5 12.0	ns

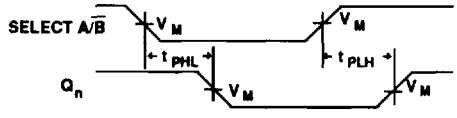
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n, B_n to $\overline{LE}$	Waveform 4	1.0 3.0			2.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n, B_n to $\overline{LE}$	Waveform 4	1.0 2.0			2.0 3.0		ns
t_w(L)	$\overline{LE}$ Pulse width, Low	Waveform 4	5.0			6.0		ns

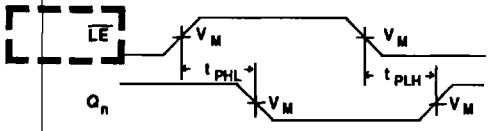
AC WAVEFORMS



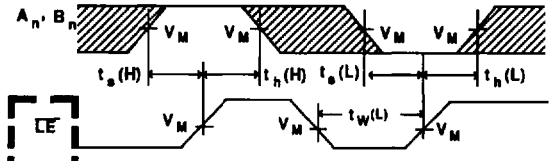
Waveform 1. Propagation Delay, SELECT A/$\overline{B}$ To Output (A latched data=Low. $\overline{LE}$=H)



Waveform 2. Propagation Delay, SELECT A/$\overline{B}$ To Output (B latched data=Low. $\overline{LE}$=H)



Waveform 3. Propagation Delay, Clock To Output (A latched data=Low. SELECT A/$\overline{B}$=H)



Waveform 4. Data Setup And Hold Times, Latch Enable pulse width

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.