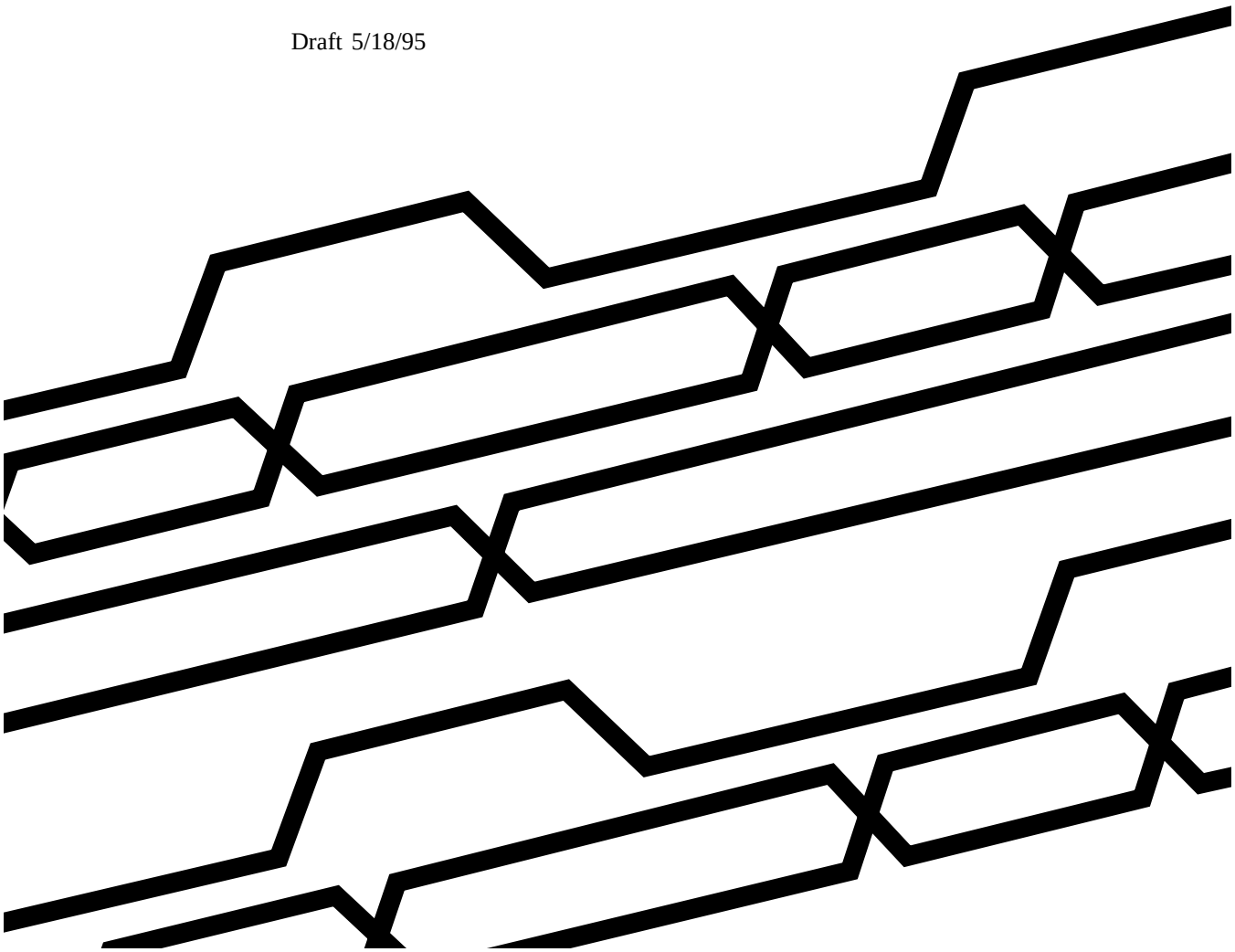
LSI LOGIC

L64705
FEC Concatenated Decoder
Preliminary
Specifications

L64705.TAR.0

Draft 5/18/95



This document is preliminary. As such, it contains data derived from functional simulations and performance estimates. LSI Logic has not verified either the functional descriptions, or the electrical and mechanical specifications using production parts.

First Edition
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This document applies to revision X of the L64705 and to all subsequent versions unless otherwise indicated in a subsequent edition or an update to this edition of the document.

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Preface

This book is the primary reference and user's manual for the L64705 FEC Concatenated Decoder. It contains a complete functional description for the L64705 and includes complete physical and electrical specifications for the L64705.

Audience

This book assumes that you have some familiarity with error control coding , digital signal processing, microprocessors and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the L64705 FEC COncatenated Decoder for use in a high speed channel decoding system.
- Engineers who are designing the L64705 into a system.

Organization

This book has the following chapters:

- Chapter 1, **Introduction**, defines the general characteristics and capabilities of the L64705.
- Chapter 2, **Interface Signal Description**, describes the characteristics of the L64705 signals that are used to interface with an external channel and CPU.
- Chapter 3, **Internal Registers and Data Tables**, describes how data is represented inside the L64705. This chapter also provides a summary of the L64705 registers and tables.
- Chapter 4, **Channel Interface**, describes the channel data transfer operations supported by the L64705.
- Chapter 5, **Synchronization Unit**, discusses the mechanism for synchronizing the internal decoder modules to the incoming data stream.
- Chapter 6, **Viterbi Decoder Module**, describes the structure and operation of the Viterbi decoder module.
- Chapter 7, **Deinterleaver Module**, describes how the data stream is reordered within the Deinterleaver module.

- Chapter 8, **Reed-Solomon Decoder Module**, presents the funtionality and operation of the Reed-Solomon Decoder module
- Chapter 9, **Descrambler Module**, describes how the data stream is reordered within the Descrambler module.
- Chapter 10, **Specifications**, describes the electrical and mechanical characteristics of the L64705.

Related Publications

L6471X, Reed-Solomon Series of FEC Devices, Technical Manual.

Conventions Used in this Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The following signal naming conventions are used throughout this manual:

- A level-significant signal that is true or valid when the signal is LOW always has an overbar ($\overline{}$) over its name.
- An edge-significant signal that initiates actions on a HIGH-to-LOW transition always has an overbar ($\overline{}$) over its name.

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” before the number—for example, 0x32CF. Binary numbers are indicated by a subscripted “2” following the number—for example, $0011.0010.1100.1111_2$.

Chapter 1
L64705 Concatenated DBS FEC Decoder

The L64705 is a complete concatenated FEC decoder that is compliant with specifications of the “Baseline Modulation/Channel Coding System” by the Digital Video Broadcast (DVB) Assosication.

It utilizes a Viterbi inner code and a Reed-Solomon outer code. The device also contains all the necessary synchronization,deinterleaving and scrambling for a complete decoding solution.

This chapter has four sections:

- Section 1.1,”Overview”
- Section 1.2 “Component Functions”
- Sections 1.3 “Features Summary”
- Section 1.4, “L64705 New Features”
- Section 1.5, “Code Performance Curves”

1.1 Overview

The advent of Digital Video Compression technology has increased the demands on Forward Error Correction (FEC) techniques. Specifically, video systems operating on compressed data streams require low bit-error rates (BER) in the order of 1e-12. Conventional FEC techniques require high transmitter power and large data overhead to achieve this low BER. The concatenation of two well known FEC techniques (Reed-Solomon and Viterbi decoding) reduces the power and bandwidth that would be required when using either FEC code individually.

FIGURE 1. Concatenated Code Structure

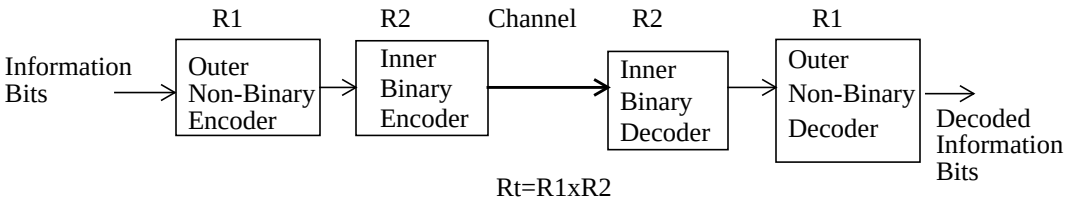


Figure 1.0 illustrates the basic Concatenated FEC technique. The first code or outer code is typically a Reed-Solomon (non-binary code) and the inner code (binary codes) can be a convolutional or binary block code. The Rate of the code is defined as the reciprocal of the bandwidth expansion. For instance a rate=1/2 code would double the bandwidth or data rate in the transmission channel. If two individual codes are used, the overall rate is just the product of the two codes.

The other performance criteria for measuring the effectiveness of an error correction technique is the Signal to Noise Ratio or SNR that is required in the channel to obtain the necessary BER at the output of the outer decoder. A low SNR corresponds to a low power requirement for the transmitter (hence lower cost). The best codes have a high-rate, and a low SNR requirement defined at a given error rate.

Table 1.0 illustrates the theoretical performance of three different rate 3/4 codes. The values are dependant on the BER operating range. For this error-rate, the composite code has almost a 3 db advantage of the best known single FEC code.

TABLE 1. Comparison Codes for BER 1e-12 and total Rate 3/4 codes

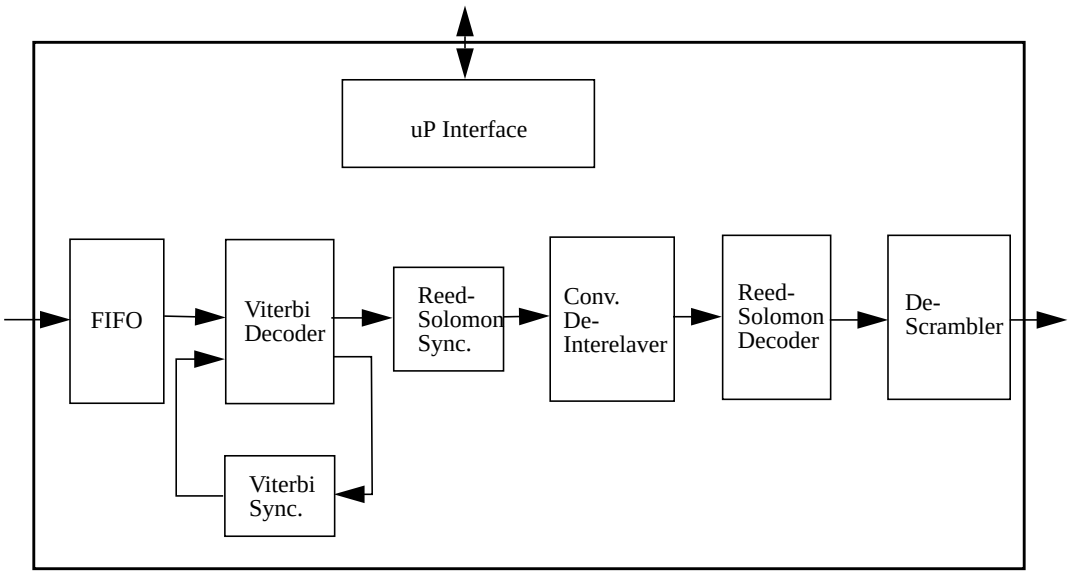
Code	**Eb/No db**
Viterbi	10.8
Reed-Solomon	8.5
Viterbi and Reed-Solomon	5.6

The lower power required by the concatenated code can result in a significantly smaller cost for DBS (Direct Broadcast Satellite) systems. The reduction in required power can be manifested in cheaper transmitters and receivers.

1.2 System Requirements

Figure 2.0 is a functional block diagram of the standard method of decoding a Viterbi-Reed-Solomon concatenated code. The process of transmission and reception introduced timing and polarity uncertainties in the data stream. These uncertainties must be removed from the data for proper FEC decoding to occur.

Figure 2.0 FEC Decoder Block Diagram



In this system methodology the Viterbi output BER is monitored to determine if the phase and symbol timing of the Viterbi are correct. By trial and error, the Viterbi timing and phase inputs (QPSK and BPSK modulation) are varied until proper alignment is detected by the synchronization circuit.

Once the Viterbi is synchronized the Reed-Solomon synchronization circuit searches for synchronization pattern in the output of the Viterbi data.When the synchronization word is found, the synchronization circuit aligns the Deinterleaver, the Reed-Solomon Decoder and the Descrambler properly and removes a possible 180 degrees phase shift not detected by the K=7 Viterbi decoder module. Use is made of the MPEG transport layer synchronization word.

The Descrambler is used to increase the transition density of the data.

The L64705 is also capable of operating with non-continuous input data streams.

1.3 Features Summary

- 60Mbits/sec maximum information rate
- Compliant with V4/MOD-B channel coding specifications
- Programmable Viterbi decoder module for rates 1/2, 2/3, 3/4, 5/6, 7/8
- (204/188) Reed-Solomon decoder
- Auto synchronization for Viterbi decoder with programmable threshold
- Programmable Synchronization for Deinterleaver, Reed-Solomon Decoder and Descrambler
- MPEGII synchronization word supported
- Single Clock with Clock Enable Pin control for “burst mode operation” or conventional 2 clock inputs for continuous data operating
- Bit Error monitoring for channel
- Uncorrectable block output indicator
- Depth 12 Deinterleaver
- Asynchronous Microprocessor interface
- 100 pin PQFP package

1.4 L64705 New Features

The following list summarizes the features that differentiate the L64705 FEC Concatenated Decoder from the L64709 FEC Concatenated Decoder:

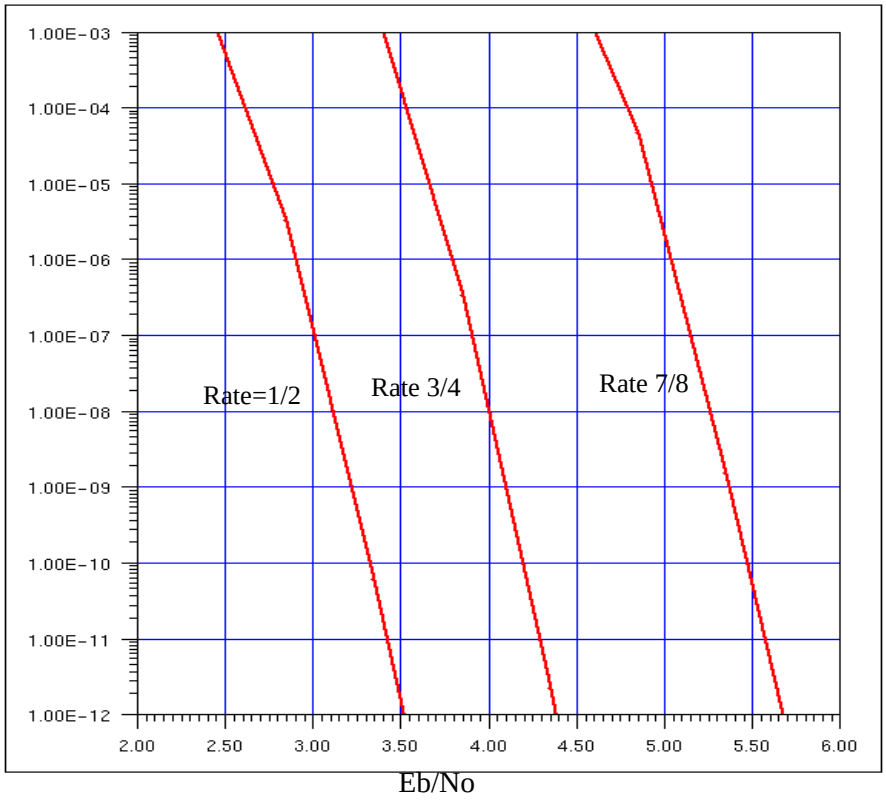
- BPSK mode of operation.
- MPEG Transport Error Indication by setting the 9th bit of the protected Transport Frame.
- Improved synchronization Algorithm: added programmability to the-synchronization state machines.
- Viterbi Bypass mode for cable systems.

- Added a SYNC pin which indicates whether a certain synchronization stage is locked or not.
- On-chip PLL allows the user to generate the required internal clock based on the puncture rate.
- DTACK pin was changed to a 3-State output.
- The De-Interleaver depth is set to 12--no programmability
- RS code is set to (204,188)--no programmability.
- Pins 72-76 changed from reserved to the PLL pins: pin 72: PCLK, 73: PLLVDD, 74: PLLAGND, 75: LP2, 76: PLLVSS.
- Pin 89 changed from reserved to SYNC

1.5 Code Performance Curves

Figure 3. is a plot of the performance of the Code selected by the European Broadcasting Union. It illustrates some typical performance characteristics for concatenated codes.

Figure 3. BER vs Eb/No RS(204,188) and K=7 Viterbi

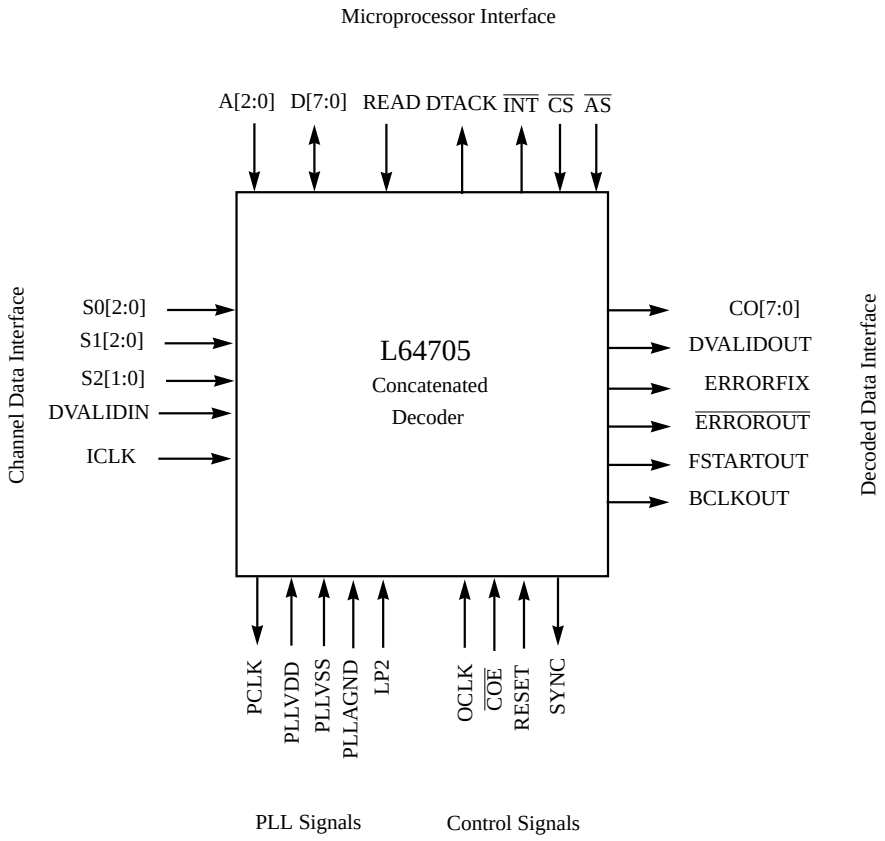


Chapter 2
L64705 Concatenated Decoder Signals

This section describes the decoder interface, which consists of 23 inputs, 17 outputs, and 8 bidirectional signals, excluding Vdd and Vss pins.

Figure 2.1 shows the logic symbol for the L64705 concatenated decoder.

Figure 2.1 Concatenated Decoder Signals



A[2:0] **Address for Internal Registers** **Input**

The decoder contains a 3-bit address bus (A[2:0]) that is used with an eight-bit data bus D[7:0], a read/write strobe (READ), and a chip select strobe ($\overline{CS}$) and an address strobe ($\overline{AS}$)to read and write internal registers. The address lines are used to select among internal registers as shown in the register map in Chapter 3.

$\overline{AS}$ **Address Strobe** **Input**

Active-LOW address strobe input. Latches the address on the A[2:0] bus on the falling edge.

BCLKOUT **Byte Clock Out** **Output**

The BCLKOUT output signal is provided as a strobe that accompanies data bytes on the CO bus when parallel data output mode is chosen. BCLKOUT cycles once per every valid output data byte and can be used by the following device to latch output data from the L64705 at the BCLKOUT rate rather than at the OCLK rate. BCLKOUT is to be disregarded in serial output mode.

CO[7:0] **Channel Data Out** **Output**

These signals form the eight-bit, decoded, output data port. Parallel or serial data is presented at the CO[7:0] pins or at CO0 respectively, and it is latched every byte or bit clock cycle. The chronological ordering in parallel output mode is MSB oldest, LSB newest.

$\overline{COE}$ **Channel Output Enable** **Input**

When asserted, $\overline{COE}$ enables the CO[7:0], ERROROUT, and ERRORFIX pins. DVALIDOUT is unaffected by the $\overline{COE}$ pin, and operation of the decoder continues regardless of the state of this pin.

$\overline{CS}$ **Chip Select** **Input**

Active-LOW chip select strobe input. During a read cycle, $\overline{CS}$ must be LOW to access the on-chip data registers. The controller may latch the data from the L64705 with the rising edge of $\overline{CS}$. During a write cycle, $\overline{CS}$ must go active LOW prior to data being valid from the controller to the L64705. After the data has met the minimum setup time, $\overline{CS}$ is taken HIGH to strobe the There is a minimum write time to allow for internal synchronization. Set up and hold times are measured with respect to the falling edge of $\overline{CS}$.(Figures 10.4, 10.5)

D[7:0] **Data Bus 7:0** **Bidirectional**
The bidirectional data bus is used for input when data are written to the chip, and as output when the chip is read. When not being read or written, the data lines are tri-stated.

DVALIDIN **Clock Enable Input** **Input**
When DVALIDIN is active (HIGH), L64705 decoder accepts data from S0[2:0] and S1[2:0] on a continuous basis. When DVALIDIN is LOW, data input to the internal FIFO and internal data processing is halted, and no new input from the S0[2:0] and S1[2:0] pins is accepted. The functionality of DVALIDIN is independent of decoding operation, so decoding can be stopped at any point on a cycle-by-cycle basis without corrupting internal data or output data streams.

DVALIDOUT **Valid Data Out** **Output**
Channel output is byte parallel or bit serial and contains the corrected channel data. New data is valid on the output in cycles in which DVALIDOUT is HIGH. DVALIDOUT is not asserted during the propagated check and GAP bytes.

$\overline{\text{DTACK}}$ **Data Acknowledge** **Output**
Active-LOW output indicating that the transaction on the D bus has completed.

ERRORFIX **Error Correction Flag** **Output**
The ERRORFIX pin is asserted to flag corrected errors. It is HIGH if any bit in a message or check byte has been corrected. ERRORFIX is only valid in cycles which DVALIDOUT is HIGH. The ERRORFIX and ERROROUT pins are never asserted in the same cycle.

$\overline{\text{ERROROUT}}$ **Error Detection Flag** **Output**
The ERROROUT pin is asserted to flag uncorrectable errors. ERROROUT is asserted at the beginning of a frame which contains an uncorrectable error, and it is deasserted at the end of the frame, if the error condition is removed. ERROROUT is exactly aligned with the output data stream.

FSTARTOUT **Frame Start Output** **Output**
FSTARTOUT is asserted during the first bit in every frame in serial output mode and during the first byte in parallel output mode with valid data when DVALIDOUT is HIGH.

ICLK **Decoder Input Clock** **Input**
ICLK is a positive, edge-triggered clock. The L64705 clocks in inputs S0, S1, DVALIDIN on the rising edge of ICLK. ICLK is independent of OCLK.

$\overline{\text{INT}}$ **Interrupt Request** **Output**
The L64705 asserts INT LOW when an internal, unmasked interrupt flag is set. INT remains asserted as long as the interrupt condition persists and the interrupt flag is not masked.

LP2 **Input to VCO** **Input**
The pin is the output from the external RC timing circuit. It serves as an input to the internal voltage controlled oscillator.

OCLK **Decoder Output Clock** **Input**
OCLK is a positive, edge-triggered clock. The L64705 internally processes data (Viterbi decoder, Synchronization, Descrambler, Deinterleaver, Reed-Solomon Decoder) based on OCLK. All data outputs (DVALIDOUT, ERROROUT, ERRORFIX, FSTARTOUT, CO[7:0]) are referenced to OCLK. OCLK is independent of ICLK.

PCLK **PLL Clock Output** **Output**
PCLK is the clock signal generated by the internal PLL clock synthesis module. The PLL is driven by the ICLK signal. PCLK can be configured to generate the clock appropriate signals for all Viterbi code rates specified under the DVB standard.

PLLAGND **PLL Analog Ground** **Input**
Analog ground pin for the PLL module.

PLLVDD **PLL Vdd** **Input**
Power supply pin for the PLL module.

PLLVSS **PLL Vss** **Input**
Power supply pin for the PLL module.

READ **Read/Write Strobe** **Input**
Active-LOW write strobe input. A LOW writes to the decoder, A HIGH reads from the decoder.

RESET **Reset** **Input**
This pin resets all internal data paths. Reset timing is asynchronous to the device clocks. Reset does not affect the configuration registers. It performs the same operation as the reset bit specified in chapter 3.

S0[2:0] **Symbol 0** **Input**
Three-bit soft decision symbol data input. One new symbol is input for every cycle of IClk.

S1[2:0] **Symbol 1** **Input**
Three-bit soft decision symbol data input. One new symbol is input for every cycle of IClk.

S2[1:0] **Symbol 2** **Input**
Extra bits for 7-bit or 8-bit symbols. Only used in Viterbi bypass mode (IS = 1).

SYNC **Synchronization Status Flag** **Output**
The SYNC pin displays the synchronization status for one of three synchronization modules incorporated in the desgin (Viterbi decoder sync, DI/RS sync, Descrambler sync). When HIGH the SYNC output inidcates the synchronization has been achieved for the chosen sync module. When LOW an out-of-synchronization condition is detected. (See chapter 3 for configuration bits)

Chapter 3
L64705 Concatenated Decoder Registers

This chapter discusses the L64705 internal registers and data tables. It also provides a description of the internal memory mapping and the access to these registers and tables from the system interface. This chapter is intended primarily for system programmers who are developing software drivers.

This chapter contains five sections:

- Section 3.1, L64705 Register Overview
- Section 3.2, Group 0, 1 Address Pointer Register (APR)
- Section 3.3, Group 2 Registers (SMR, STS)
- Section 3.4, Group 3 Diagnostics Registers
- Section 3.5, Group 4 Configuration Registers
- Section 3.6, Group 5 Tables

3.1 L64705 Register Overview

The L64705 registers and memory resources are divided into six groups: Group 0 - 5. Group 0 and 1 contain the APR Register, which addresses the registers and tables in Group 3, 4 and 5. Group 2 contains the status and mode register. Group 3 contains the status counters, Group 4 the set of configuration registers. Group 5 provides access to all the internal RAMs for testability purposes.

Group	*Function*
0	Address Pointer Register, LSB
1	Address Pointer Register, MSB
2	Mode/Status Registers
3	Status Counters
4	Configuration Register
5	RAM Access for Testability

Most registers and table entries are 8 bits wide—some registers are up to 24 bits wide. All accesses are done in 8-bit widths. Initialize the APR Register in group 0 and 1 before accessing the registers or tables in Groups 3, 4 and 5.

Internally, the L64705 has a 8-bit architecture. All registers and tables are memory-mapped to the system with 8-bit resolution. The L64705 contains some registers that are longer than 8 bits. These registers are divided into two or three 8-bit sections: the least-significant word (LSW) the middle-significant word (MW) and the most-significant word (MSW). Each 8-bit section is assigned a specific address, and therefore requires an individual memory cycle during programming.

The L64705 uses an auto-increment address pointer to simplify the initialization procedure and to reduce the number of memory locations occupied by the L64705 in CPU memory. The address pointer is active when accessing Groups 3, 4 and 5. The auto-increment feature is active for Groups 4 and 5. After each complete access to this group, the L64705 automatically increments the address pointer by one on the rising edge of $\overline{CS}$. After the address pointer increments, it points to the next table or register entry.

3.2 Group 0, 1 Address Pointer Register (APR)

The Address Pointer Register (APR), shown in Figure 3.1, is an 13-bit register, which points to the internal registers and tables in Groups 3, 4 and 5. It is accessed when A[2:0] =000_2 or 001_2 . Before accessing a register or table location from Group 3, 4 or 5, you must pre-initialize the APR with the address of the first desired register or table entry according to the internal memory mapping. The APR automatically increments by one on the LOW-to-HIGH transition of $\overline{CS}$ when accessing the Group 4 or 5 registers and tables (A[1:0] = 100_2 or 101_2). Two consecutive accesses are required to load the complete APR, the first to Group 0 to load the 8 LSB's, the second to Group1 to load the 4 MSB's.

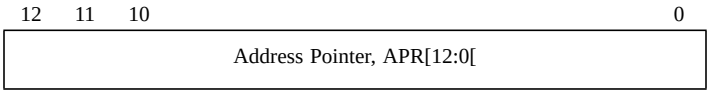
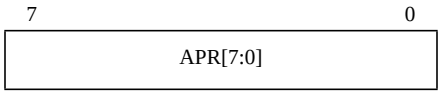


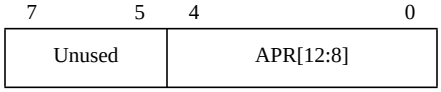
Figure 3.1 Address Pointer Register

Unused bits in these registers are reserved for future expansion and should be set to zero.

Group 0, Data Bus D[7:0]



Group 1, Data Bus D[7:0]



3.3 Group 2 Registers

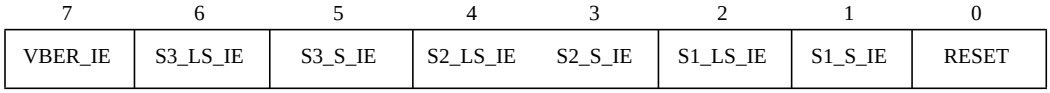
Group 2 contains two registers: the System Mode Register (SMR) and the System Status Register (STS). A CPU may access these registers by setting A[2:0] =010_2. An external system can access these registers without restrictions during operation without interrupting the internal processing unit. The following figure describes the two registers.

System Mode Register (SMR)

The SMR Register is a write-only register that allows external system control of the L64705. The SMR Register contains bits that reset the device and enable interrupts.

Figure 3.2 shows the bit organization of the SMR Register. Descriptions of the fields follow the figure. The L64705 clears all bits in the SMR Register to zero after a software or hardware reset.

Figure 3.2 System Mode Register



VBER_IE Viterbi Bit Error Rate Monitor Interrupt Enable 7
The CPU may set VBER_IE to enable an interrupt when the Viterbi decoder reaches the period specified by VMDC2 (period over which

the Viterbi bit errors are counted). If this condition occurs, the L64705 then sets the VBER bit in the STS.

VBER_IE	*Definition*
0	Disable Viterbi BER Count Interrupt
1	Enable Interrupt for Viterbi BER count

S3_LS_IE **Stage 3, Loss of Synchronization, Interrupt Enable** **6**

The CPU may set S3_LS_IE to enable an interrupt when Descrambler synchronization is lost.

S3_LS_IE	*Definition*
0	Disable Stage3, Loss of Sync. Interrupt
1	Enable Stage3 Loss of Sync. Interrupt

S3_S_IE **Stage 3, Synchronization, Interrupt Enable** **5**

The CPU may set S3_S_IE to enable an interrupt when Descrambler synchronization is established.

S3_S_IE	*Definition*
0	Disable Stage3, Sync. Interrupt
1	Enable Stage3 Sync. Interrupt

S2_LS_IE **Stage 2, Loss of Synchronization, Interrupt Enable** **4**

The CPU may set S2_LS_IE to enable an interrupt when Deinterleaver/Reed-Solomon Decoder synchronization is lost.

S2_LS_IE	*Definition*
0	Disable Stage2, Loss of Sync. Interrupt
1	Enable Stage2 Loss of Sync. Interrupt

S2_S_IE **Stage 2, Synchronization, Interrupt Enable** **3**

The CPU may set S2_S_IE to enable an interrupt when Deinterleaver/Reed-Solomon Decoder synchronization is established.

S2_S_IE	*Definition*
0	Disable Stage2, Sync. Interrupt
1	Enable Stage2 Sync. Interrupt

S1_LS_IE **Stage 1, Loss of Synchronization, Interrupt Enable** **2**

The CPU may set S1_LS_IE to enable an interrupt when Viterbi Decoder synchronization is lost.

S1_LS_IE	*Definition*
0	Disable Stage1, Loss of Sync. Interrupt
1	Enable Stage1 Loss of Sync. Interrupt

S1_S_IE **Stage 1, Synchronization, Interrupt Enable** **1**

The CPU may set S1_S_IE to enable an interrupt when Viterbi Decoder synchronization is established.

S1_S_IE	*Definition*
0	Disable Stage1, Sync. Interrupt
1	Enable Stage1 Sync. Interrupt

RESET **Software Reset** **0**

FRESET	*Definition*
0	No Reset
1	The L64705 Issues a Reset

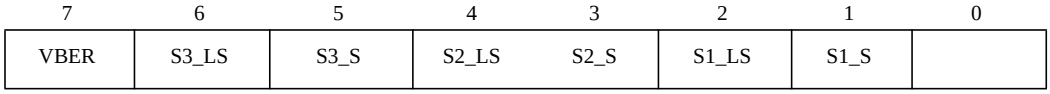
When the CPU sets the RESET bit to one, the L64705 resets the internal datapath and control modules. The CPU does not need to set the bit back to a zero to complete the reset. The L64705 issues a single RESET pulse each time the CPU writes a one to this bit. When the RESET bit is set, the L64705 resets the processing unit and state machines to their initial states. The following operations occur when RESET is asserted (note that the RESET pin has the same effect as the RESET bit):

- Internal datapath and control modules reset
- Group 4 and 5 tables and registers unaffected by RESET
- Group 3 UEC and CEC counters reset
- DVALIDOUT pin set LOW
- FSTARTOUT pin set LOW
- ERROROUT pin set HIGH
- ERRORFIX pin set LOW
- System Status Register (STS) flags cleared

System Status Register (STS)

The STS Register, shown below, provides the external system with status information on the L64705. This 8-bit register is read-only. It provides information that may cause generation of an internal interrupt condition. The interrupt status bits are set regardless of the enable interrupt bits in the SMR Register. The internal status is updated every L64705 OCLK, and when the CPU reads the status, the current information is buffered in a special purpose STS buffer, which locks the STS value until the end of the CPU read operation. Note that the status bits are reset after a read access to the STS, or after a hardware reset.

Figure 3.3 System Mode Register



S3_LS **Stage 3, Loss of Synchronization Flag** **6**

The L64705 sets S3_LS if the the Descrambler synchronization module has determined that synchornization is lost. Under this condition it also generates an interrupt if the S3_LS_IE bit is set in the SMR. After a reset or a Group 2 (STS) read, the L64705 clears S3_LS to zero.

S3_LS	***Definition***
0	Sync Status unchanged
1	Loss of Sync. detected

S3_S **Stage 3, Synchronization Flag** **5**

The L64705 sets S3_S if the Descrambler synchronization module has acquired synchronization. Under this condition it also generates an interrupt if the S3_S_IE bit is set in the SMR. After a reset or a Group 2 (STS) read, the L64705 clears S3_S to zero.

S3_S	***Definition***
0	Sync Status unchanged
1	Synchronization. acquired

S2_LS **Stage 2, Loss of Synchronization Flag** **4**

The L64705 sets S3_LS if the Deinterleaver/Reed-Solomon Decoder synchronization module has determined that synchornization was lost. Under this condition it also generates an interrupt if the S2_LS_IE bit is set in the SMR. After reset or a Group 2 (STS) read, the L64705 clears S2_LS to zero.

S2_LS	***Definition***
0	Sync Status unchanged
1	Loss of Sync. detected

S2_S **Stage 2, Synchronization Flag** **3**

The L64705 sets S2_S if the Deinterleaver/Reed-Solomon Decoder synchronization module has acquired synchronization. Under this condition it also generates an interrupt if the S2_S_IE bit is set in the SMR. After reset or a Group 2 (STS) read, the L64705 clears S2_S to zero.

S2_S	***Definition***
0	Sync Status unchanged
1	Synchronization. acquired

S1_LS **Stage 1, Loss of Synchronization Flag** **2**

The L64705 sets S1_LS if the Viterbi Decoder synchronization module has determined that synchornization was lost. Under this condition it also generates an interrupt if the S1_LS_IE bit is set in the SMR. After reset or a Group 2 (STS) read, the L64705 clears S1_LS to zero.

S1_LS	***Definition***
0	Sync Status unchanged
1	Loss of Sync. detected

S1_S **Stage 1, Synchronization Flag** **1**

The L64705 sets S1_S if the Viterbi Decoder synchronization module has acquired synchronization. Under this condition it also generates an interrupt if the S1_S_IE bit is set in the SMR. After reset or a Group 2 (STS) read, the L64705 clears S1_S to zero.

S1_S	***Definition***
0	Sync Status unchanged
1	Synchronization. acquired

VBER **Viterbi Bit Error Rate Flag** **7**

The L64705 sets VBER if the period specified by VMDC2 is reached. It also generates an interrupt if the VBER_IE bit is set in the SMR when the VMDC2 is reached. After reset or a Group 2 (STS) read, the L64705 clears VBER to zero.

VBER	*Definition*
0	VMDC2 period not reached
1	VMDC2 period reached

3.4 Group 3 Registers

Group 3 consists of a number of internal parameters that are made available to the user for diagnostics and performance evaluation purposes. The internal status of the registers is updated every OCLK cycle. When the CPU reads the status, the current information is buffered in a special purpose buffer which locks the value of the respective parameter until the end of the read operation.

The following figure shows the addresses and fields of the Group 3 registers.

Figure 3.4 Group 3 Register Map

APR	D7	D6	D5	D4	D3	D2	D1	DO
0	Reed-Solomon Corrected Error Count low byte, CEC[7:0]							
1	Reed-Solomon Corrected Error Count high byte, CEC[15:8]							
2	Reed-Solomon Uncorrected Error Count low byte, UEC[7:0]							
3	Reed-Solomon Uncorrected Error Count high byte, UEC[15:0]							
4	Viterbi Bit Error Rate Count low byte, VBERC[7:0]							
5	Viterbi Bit Error Rate Count high byte, VBERC[15:8]							

APR 0, 1 Registers

CEC **Corrected Error Count**

When read, this register presents a count of corrected errors since it was last reset. When written, the register is reset to zero. CEC is presented in 16 bits. The LSB is found on APR 0, bit 0, the MSB on APR 1, bit 7. The CEC count will saturate at 65535.

APR 2, 3 Registers

UEC **Uncorrected Error Count**

When read, this register presents a count of the uncorrected code words since it was last reset. When written, the register is set to zero. UEC is presented in 16 bits. The LSB is found on APR 2, bit 0, the MSB on APR 3, bit 7. The UEC count will saturate at 65535.

APR 4, 5 Registers

VBERC **Viterbi Bit Error Count**

When read, this register presents a count of the number of Viterbi decoder bit errors found during the time period specified by VMDC2. VBERC is presented in 16 bits. The LSB is found on APR 4, bit 0, the MSB on APR 5, bit 7. The actual number of errors is obtained as follows: Number of errors = VBERC * 4.

3.5 Group 4 Registers

Most registers and table entries are 8 bits wide—some registers are wider (up to 24 bits). All accesses are done in 8-bit widths.

The following figure shows the addresses and fields of the decoder registers.

Figure 3.5 Group 4 Register Map

APR	D7	D6	D5	D4	D3	D2	D1	DO
0	en	tstn	Pll_N(6)					
1	iddtn	cnt_out	Pll_S(6)					
2	IMQ	MF	QB	Pll_T(5)				
3	Viterbi Code Rate(3)			TEI	TM		Pll_M(2)	
4	Viterbi Max Data Bit Count 1(8)							
5	Viterbi Max Data Bit Count 2, VMDC2[7:0], low byte							
6	Viterbi Max Data Bit Count 2 , VMDC2[15:8], middle byte							
7	Viterbi Max Data Bit Count 2 , VMDC2[23:16], high byte							
8	Viterbi Maximum Bit Error Count(8)							
9	Synchronization Word(8)							
10								L
11	BF		Sync Status(2)		Sync States Acqu.(2)		Sync States Track(2)	

APR	D7	D6	D5	D4	D3	D2	D1	DO
12	BPS(3)			IS	OF	Output Selector (3)		
13	PLL Reset							

APR 0 Registers

Pll_N **PLL Configuration Parameter N**
Pll_N[5:0] is one of 3 parameters set to configure the PLL module for clock synthesis. See Chapter 4.4 for a table of values.

en **PLL Test**
LSI Logic internal test bit. The user must set this bit to 0.

tstn **PLL Test**
LSI Logic internal test bit. The user must set this bit to 0.

APR 1 Registers

Pll_S **PLL Configuration Parameter S**
Pll_S[5:0] is one of 3 parameters set to configure the PLL module for clock synthesis. See Chapter 4.4 for a table of values.

iddtn **PLL Test**
LSI Logic internal test bit. The user must set this bit to 0.

cnt_out **PLL Test**
LSI Logic internal test bit. The user must set this bit to 0.

APR 2 Registers

Pll_T **PLL Configuration Parameter T**
Pll_T[3:0] is one of 3 parameters set to configure the PLL module for clock synthesis. See Chapter 4.4 for a table of values.

MF **Modem Format**
The bit MF (Modem Format) determines the data format for the S0 and S1 soft decision data inputs.

Input quantization offset binary format (MF HIGH):

S0[2:0]/S1[2:0]	Interpretation
111	Most Reliable One
110	
101	
100	Least Reliable One

S0[2:0]/S1[2:0]	Interpretation
011	Least Reliable Zero
010	
001	
000	Most Reliable Zero

Input quantization sign magnitude format (MF LOW):

S0[2:0]/S1[2:0]	Interpretation
111	Most Reliable One
110	
101	
100	Least Reliable One
000	Least Reliable Zero
001	
010	
011	Most Reliable Zero

IMQ (I, -Q) Symbol Format

The bit IMQ indicates the format of the incoming symbol stream. For systems that input (I, -Q) to L64705 the IMQ bit needs to be set HIGH. For (I, Q) inputs to L64705 the IMQ bit is set LOW.

QB QPSK/BPSK Format Select

The bit QB indicates the demodulation format of the incoming symbol stream. For systems that input a QPSK symbol pair (I, Q) once per ICLK cycle the QB bit needs to be set LOW. For BPSK input (I stream only) the QB bit is set HIGH. For BPSK mode the S1[2:0] inputs are not used (Also see chapter 6.2). (QB must be set LOW when IS is HIGH).

TEI Transport Error Indicator Select

When TEI is set HIGH the transport error indicator mechanism is active. In this mode the first bit following the sync byte in a Transport Packet is forced HIGH whenever the data block was found to be uncorrectable by the Reed-Solomon decoder otherwise it remains unchanged. When TEI is LOW the transport

error indicator will not be set at any time.(See H.222, paragraph 2.4.3.2 Transport Stream Packet Layer)

APR 3 Registers

VCR **Viterbi Code Rate**

The three MSBs set the code rate for the Viterbi decoder module on the device. The three bits are assigned as follows:

	Data Bits		
Interpretation	***D7***	***D6***	***D5***
Rate 1/2	0	0	0
Rate 2/3	0	0	1
Rate 3/4	0	1	0
Rate 5/6	0	1	1
Rate 7/8	1	0	0
Unused	1	0	1
Unused	1	1	0
Unused	1	1	1

PLL_M **VCO Frequency Range for PLL module**

PLL_M[1:0] indicates the frequency range of the VCO. The user needs to set the PLL_M value according to the table presented in chapter 4.4.

	Data Bits	
VCO Range	***D1***	***D0***
40 - 50 MHz	0	0
50 - 60 MHz	0	1
60 - 70 MHz	1	0
70 - 80 MHz	1	1

TM **Test Mode**

When set HIGH Test Mode inables a LSI Logic internal test mode. The TM bit must be set LOW by the user.

APR 4 Registers

VMDC1 Viterbi Maximum Data Bit Count 1

VMDC1 specifies the number of valid data bits divided by 256 over which the number of Viterbi decoded bit errors are counted for synchronization. For example, a value of VMDC1[7:0] =00000010_2 specifies 512 data bits.

APR 5, 6, 7 Registers

VMDC2 Viterbi Maximum Data Bit Count 2

VMDC2 specifies the number of valid data bits divided by 4 over which the number of bit errors in the Viterbi output data stream are counted. The value for VMDC2 occupies 24 bits and is arranged in three bytes with APR 4, bit 0 being the least significant and APR 6, bit 7 being the most significant bit. For example, a value of VMDC2[23:0] =$0000F0_H$ specifies 960 data bits.

APR 8 Registers

VMBEC Viterbi Maximum Bit Error Count

VMBEC specifies the maximum number of (Viterbi bit errors/128 + 32) that are allowed to occur within the time period set by VMDC1. Whenever the bit error count VBEC exceeds the value VMBEC the sync module concludes that the Viterbi decoder module is out of synchronization and proceeds to adjust the phase of the incoming symbol

stream until synchronization is reached. For example, a value of VMBEC[7:0] =00000011_2 specifies 416 errors.

APR 9 Registers

SW **Synchronization word**

This register contains the synchronization word used by the synchronization module in stages two and three. Within this byte chronologically the MSB is oldest, the LSB newest.

APR 10 Registers

L **Mismatching Bits, Tracking Mode, Sync 2**

Maximum number of mismatching bits allowed to declare a match when comparing 8 bits in the data stream to the reference sync word during tracking phase in the second synchronization stage. L can be configured from 0 to 2. A higher value of L will result in a smaller probability of loss of lock due to random noise, a lower value in a higher one.

	Data Bits	
Number mismatching bits:	***D1***	***D0***
0	0	0
1	0	1
2	1	0

APR 11 Registers

SST **Synchronization States, Tracking Mode**

The second synchronization module (after Viterbi Decoder, before Deinterleaver module) allows for three different state diagrams to be used in the tracking phase. The number of missed synchronization

words that will cause “out-of-synchronization” to be declared can be configured from 2 to 5.

	Data Bits	
Number of missed Sync words to loss of lock:	***D1***	***D0***
2	0	0
3	0	1
4	1	0
5	1	1

SSA **Synchronization States, Acquisition Mode**

The second synchronization module (after Viterbi Decoder, before Deinterleaver module) allows for three different state diagrams to be used in the acquisition phase. The number of proerly identified synchronization words that will cause “in-synchronization” to be declared can be configured from 3 to 6.

	Data Bits	
Number of Sync words found to acquire:	***D3***	***D2***
3	0	0
4	0	1
5	1	0
6	1	1

SSS **Synchronization Status Select**

Through the SYNC pin the user is able to observe the synchronization status of the three synchronization modules contained in the device: Viterbi decoder synchronization, Deinterleaver/Reed-Solomon decoder synchronization and Descrambler Synchronization. SSS select which one of theses three sync status bit is being propagated to the SYNC output pin.

	Data Bits	
SYNC pin connected to:	***D5***	***D4***
Viterbi decoder sync	0	0
DI/RS decoder sync	0	1
Descrambler sync	1	0

BF **BCLKOUT Format**

When LOW BCLKOUT produces contiuous clock waveform with 50% duty cycle at 1/8 the OCLK frequency. It can be used by a downstream device that runs on a byte clock rather than on a bit clock. In order to identify valid data bytes for this case the DVALIDOUT pin

needs to be observed. When HIGH the BCLKOUT produces a rising edge for every valid data byte on the CO output bus. A downstream device is able to use BCLKOUT as a data latching strobe without the need to inspect DVALIDOUT.

BCLKOUT function:	*Data Bits D7*
Cont. clock	1
Data Strobe	0

APR 12 Registers

OS **Output Selector**

The output of several major functional blocks can be observed at the chip output. For a detailed description of the signals observed for the cases below, see chapter 4 for detailed waveforms

	Data Bits		
Interpretation	*D2*	*D1*	*D0*
Descrambler Output	0	0	0
Sync 3 Output	0	0	1
RS decoder Output	0	1	0
Deinterleaver Output	0	1	1
Sync 2 Output	1	0	0
Viterbi Decoder Output	1	0	1
Sync 1 Output	1	1	0
Unused	1	1	1

OF **Descrambler Output Format**

This register controls the selection of the output format for the descrambler:

Interpretation of CO[7:0]	*Data Bits D3*
Bit Serial Data Output	0
Byte Parallel Data Output2	1

For Bit Serial Output one bit of decoded data is presented on CO.0 every OCLK cycle. In Byte parallel mode one byte of decoded data is presented on CO[7:0] every eight OCLK cycles.

IS **Input Selector**
This register controls the selection of the input data path:

Interpretation	*Data Bits D4*
Viterbi Decoder stage active	0
Viterbi decoder Stage bypassed	1

When the Viterbi decoder stage is bypassed (IS=1) the BPSK/QPSK mode selector must be set to QPSK mode (QB=0). See chapter 4.4 for functional explanation.

BPS[2:0] **Symbol size for Viterbi Bypass Mode**
PBS is only used when IS =1, it is unused for IS =0. BPS indicates how many bits of input are to be treated as a symbol. The three bits are assigned as shown in the table below:

	Data Bits		
Number of Bits/Symbol	*D7*	*D6*	*D5*
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

APR 13 Registers

PLL Reset **Reset for PLL Module**

A write operation to APR13 will generate an internal reset pulse to the PLL module. Data on the D[7:0] bus is ignored during write. It is recommended that the PLL module be reset before opertion.
The PLL Reset location (APR13) cannot be read.

3.6 Group 5 Tables

Group 5 contains all the RAM elements that are incorporated in the L64705 architecture. From a users perspective, the Group 5 resources can be written and read randomly for testing purposes.

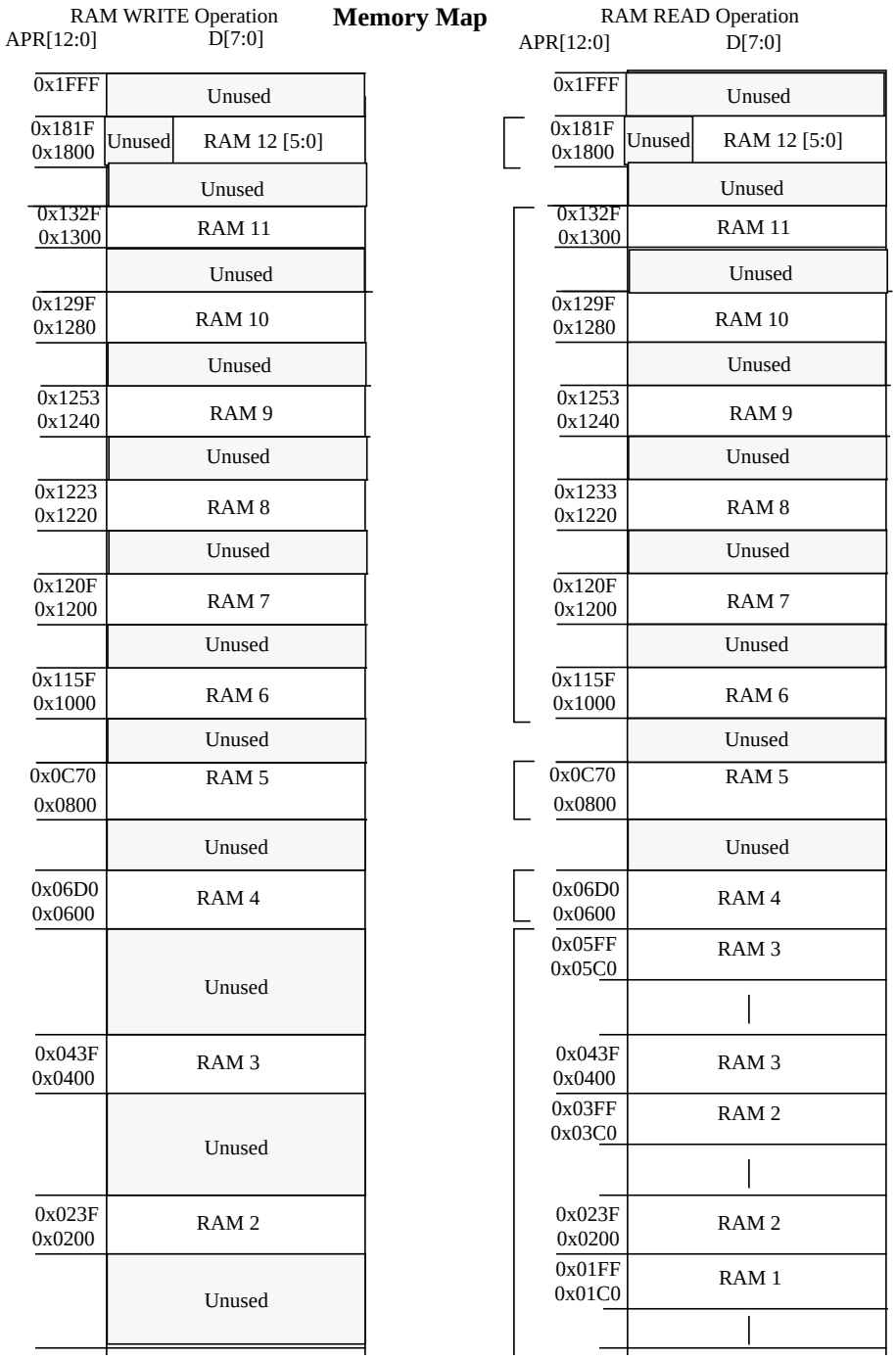
Because Group 5 contains larger tables, you must use the APR Register to address specific locations in the group. You must initialize the APR Register to the starting address of the destination memory in Group 5 prior to accessing Group 5. The APR Register is automatically incremented by one at the end of each memory read or write cycle to Group 5.

A CPU can access Group 5 by setting the ADR[2:0] pins to 101_2.

The following figure shows the overall memory mapping of Group 5 tables within the L64705. Writing into areas marked *unused* within the memory map will have no effect.

Note that RAM 1, RAM 2 and RAM 3 appear in different configuration depending as a function of read or write access. During write access each of these three memories occupies 64 consecutive addresses in the map. However, during a read they occupy eight consecutive blocks of 64 addresses. For example, RAM 1 is written from APR[12:0] =0000_H to APR[12:0] =$003F_H$. It is read in blocks starting at APR[12:0] =0000_H - $003F_H$ and ending at APR[12:0] =$01C0_H$ -$01FF_H$. The data presented on D[7:0] repeats every 64 address locations. RAM 2 and RAM 3 are organized in the same way starting from APR[12:0] =0200_H and APR[12:0] =0400_H respectively. All other storage elements have the same mapping for read and write cycles.

Memory Map


RAM WRITE Operation
APR[12:0]
D[7:0]
0x1FFF
Unused
0x181F
0x1800
Unused
RAM 12 [5:0]
Unused
0x132F
0x1300
RAM 11
Unused
0x129F
0x1280
RAM 10
Unused
0x1253
0x1240
RAM 9
Unused
0x1223
0x1220
RAM 8
Unused
0x120F
0x1200
RAM 7
Unused
0x115F
0x1000
RAM 6
Unused
0x0C70
0x0800
RAM 5
Unused
0x06D0
0x0600
RAM 4
Unused
0x043F
0x0400
RAM 3
Unused
0x023F
0x0200
RAM 2
Unused
RAM READ Operation
APR[12:0]
D[7:0]
0x1FFF
Unused
0x181F
0x1800
Unused
RAM 12 [5:0]
Unused
0x132F
0x1300
RAM 11
Unused
0x129F
0x1280
RAM 10
Unused
0x1253
0x1240
RAM 9
Unused
0x1233
0x1220
RAM 8
Unused
0x120F
0x1200
RAM 7
Unused
0x115F
0x1000
RAM 6
Unused
0x0C70
0x0800
RAM 5
Unused
0x06D0
0x0600
RAM 4
0x05FF
0x05C0
RAM 3
0x043F
0x0400
RAM 3
0x03FF
0x03C0
RAM 2
0x023F
0x0200
RAM 2
0x01FF
0x01C0
RAM 1

Chapter 4
Channel Interfaces and Data Control

The L64705 interface supports two independent interfaces for incoming channel data and for decoded output data. Both interfaces are used simultaneously to transfer data from a demodulator device to the L64705 and from the L64705 to the next processing device.

This chapter contains four sections:

Section 4.1, Data Control and Clocking Schemes

Section 4.2, Channel Data Input Interface

Section 4.3, Decoded Data Output Interface

Section 4.4, Data Path Configuration

4.1 Data Control and Clocking Schemes

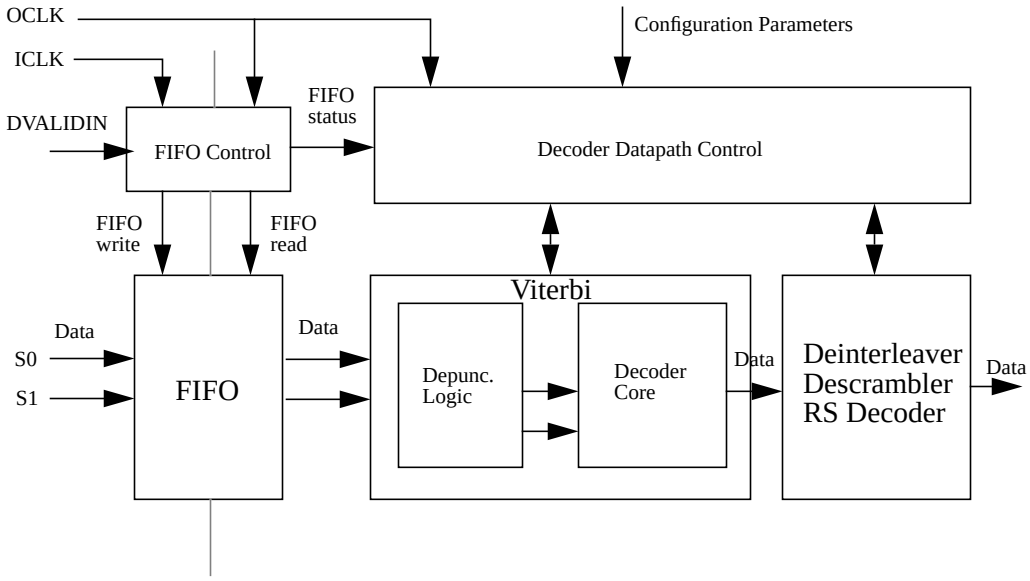
In order to accommodate a number of possible configurations in a channel decoding system the L64705 employs a scheme that uses two independent clock signals (ICLK, OCLK) to control incoming channel data, internal data processing and decoded output data.

The block diagrams below outlines the major elements involved: Input FIFO, Viterbi Depuncturing Module, Decoder modules.

The two FIFO ports are operated asynchronously. Data on the FIFO input is latched with respect to the rising edge of ICLK, data on the FIFO output is read with respect to the rising edge of OCLK. A FIFO control unit performs the necessary arbitration between the two asynchronous ports and issues the appropriate control signals (FIFO read, write, FIFO empty).

The clock rates at which the FIFO ports can be operated are a function of the code rate chosen for the Viterbi decoder. In particular, the fact that the depuncturing module is performing the insertion of erasures into the data stream determines the relation between ICLK and OCLK. In the case of a

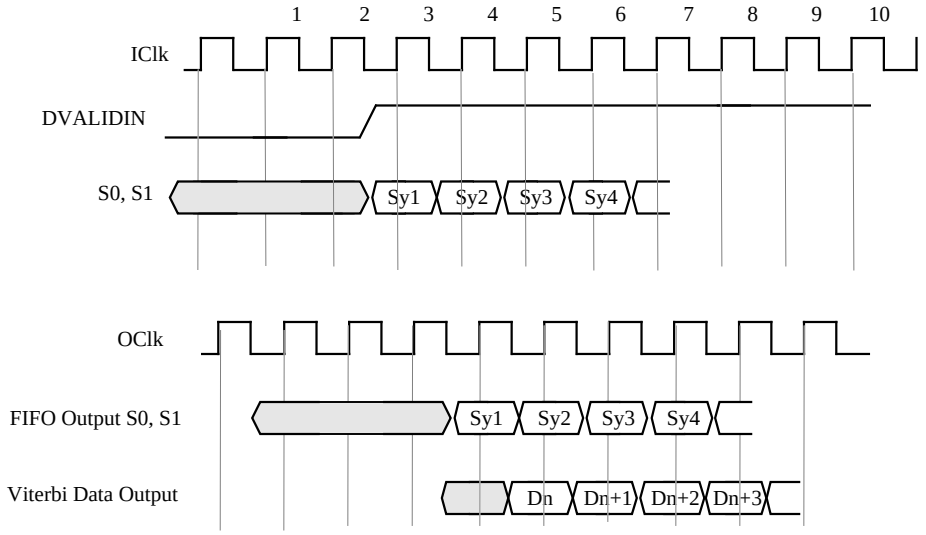
rate 1/2 decoder configuration both ports need to run at the same speed on average since no additional data is being generated after the FIFO. The maximum operation frequency is 60 MHz for FIFO input and output as well as the following decoding modules. For a rate 3/4 scenario the FIFO input data rate is limited to 40 Msymbols/sec (or 40 MHz for ICLK).



Under certain circumstances localized differences in data rates between FIFO input and output may occur. As long as the input data rate remains below the maximum average rate for the chosen configuration no internal corruption of the internal data stream will occur since the L64705 is capable of temporarily halting internal processing (FIFO empty condition) until sufficient data is available to continue. Should the input data rate be above the relevant rate there is a possibility of an FIFO overflow which will result in an incomplete data sequence being supplied to the decoding cores. Therefore, the user must not allow the FIFO to overflow for proper operation of the L64705.

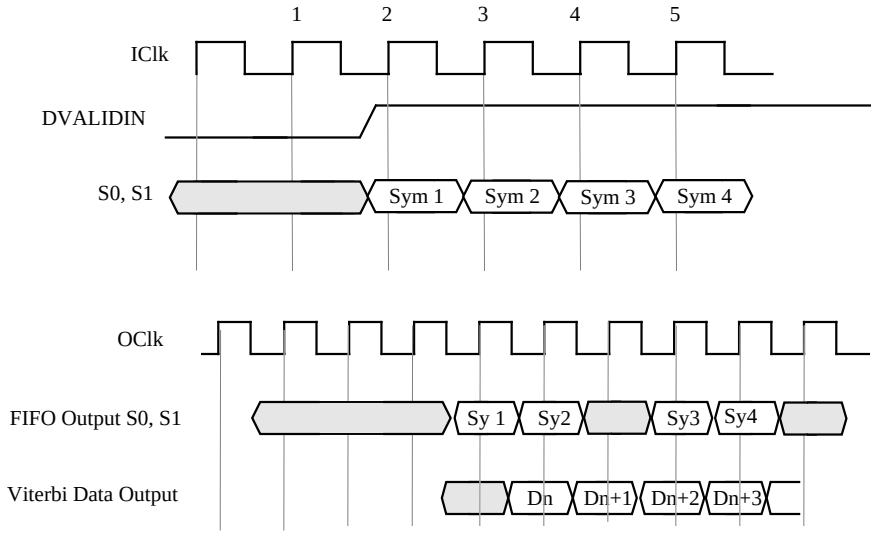
The sample waveforms below outline some cases that are likely to occur.

Example 1: Code Rate 1/2 system



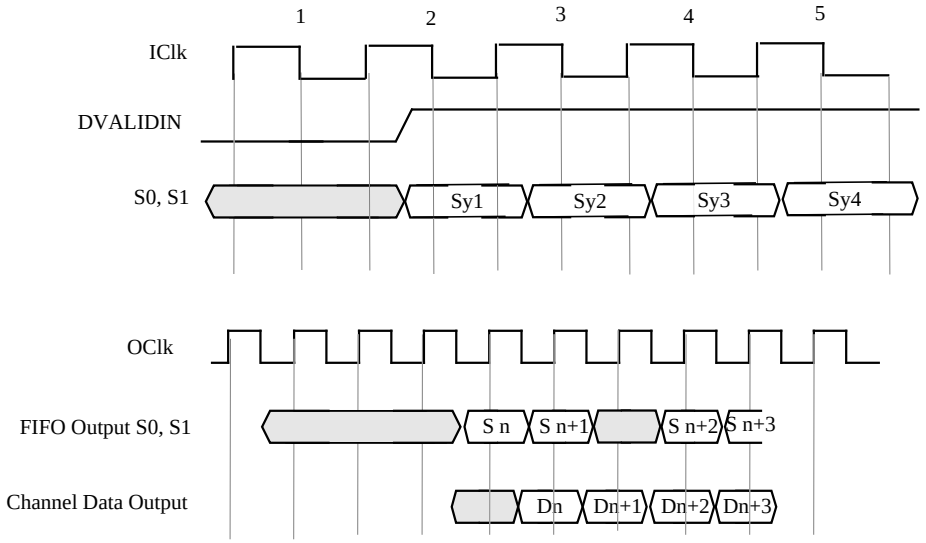
Example 1 shows a rate 1/2 case. Both FIFO input and FIFO output data streams run at the same rate since no extra information (erasures) needs to be added after the FIFO. ICLK and OCLK do not need to be aligned in phase.

Example 2: Code Rate 3/4 system, different ICLK and OCLK



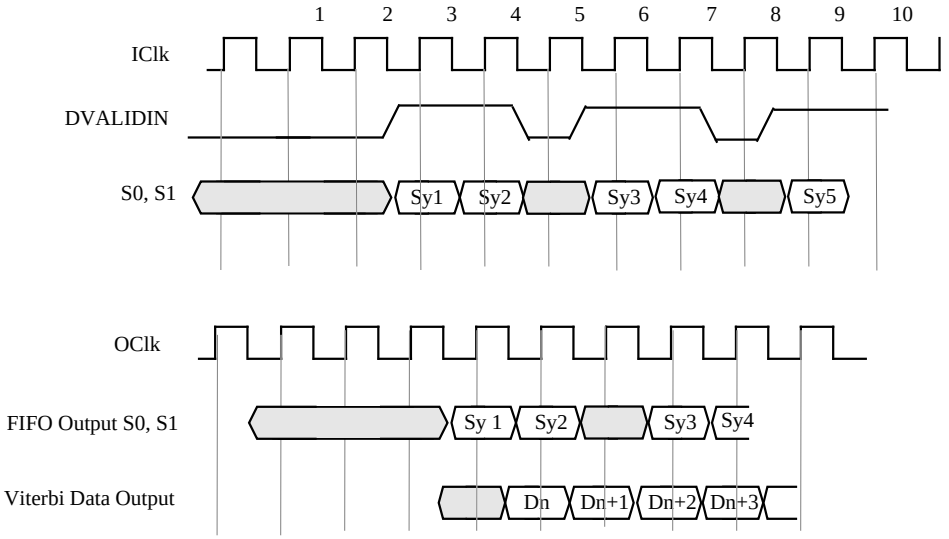
Example 2 outlines the case in which the input data rate is set at 3/4 of the data processing rate in the decoding pipeline. Since extra symbols (erasures) will be inserted by the depuncturing logic the symbols are removed from the FIFO in small bursts at the higher clock rate (OCLK). After the Viterbi decoder the data stream becomes a continuous one at the OCLK rate.

Example 3: Code Rate 3/4 system, 2 * ICLK = OCLK



Example 3: If the same data rate ratios shown in example 2 are to be maintained and the incoming data stream is continuous, a clocking scheme can be used in which the frequency of OCLK is fixed at twice that of ICLK. Since the FIFO is being read at the OCLK frequency, a rate greater than the one dictated the Viterbi code rate, it will empty out periodically. The data pipeline is designed to handle such internal interruptions in the data stream without corrupting data already being processed. As a consequence, the channel output data appears in bursts at the OCLK rate, but on average still maintains the data rate imposed by the Viterbi decoder. The DValidOut pin is used to indicate the position of valid output data.

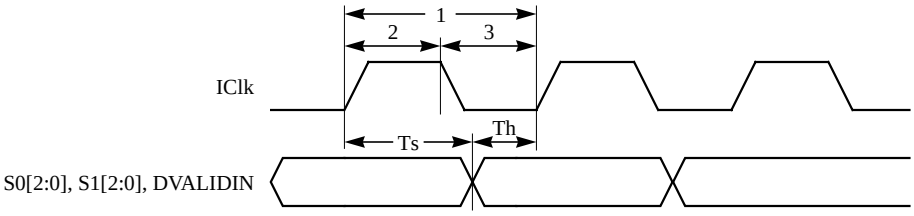
Example 4: Code Rate 3/4 system, ICLK = OCLK



Example 4: If the same data rate ratios shown in example 2 are to be maintained, but only a single clock (OClk) is available the DVALIDIN pin can be used to accommodate these requirements. On the FIFO input side two symbols are being accepted in two cycles with every third cycle skipped as indicated by DVALIDIN LOW. Internally the FIFO will be read according to a similar scheme dictated by the depuncturing logic.

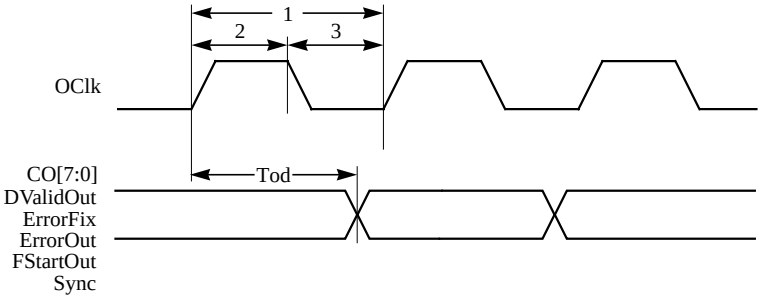
4.2 Channel Data Input Interface

The channel data input signals S0[2:0], S1[2:0], DVALIDIN are referenced to IClk in the manner outlined below.



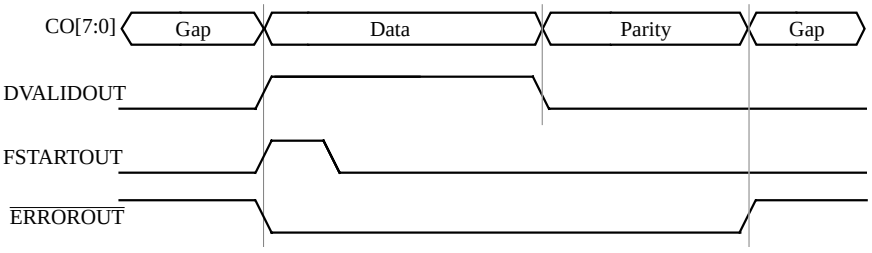
4.3 Channel Data Output Interface

The channel data output signals CO[7:0], DValidOut, ErrorFix, ErrorOut, FStartOut and Sync are all referenced to OClk.



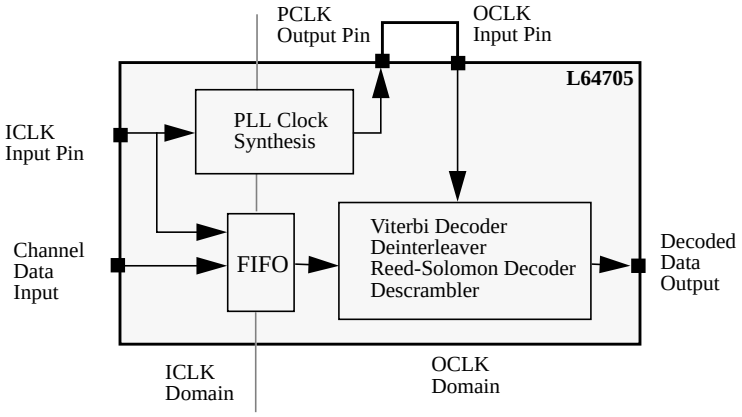
New data is valid on the output in cycles in which DVALIDOUT is HIGH, as shown in figure below. DVALIDOUT is not asserted during the propagated parity and gap bytes, but $\overline{\text{ERROROUT}}$ goes LOW for both data and parity bytes when an uncorrectable error is detected.

FSTARTOUT is asserted during the first bit of the first symbol of every frame. A gap is not required in the frame structure, and gap data is not affected by the decoding process.



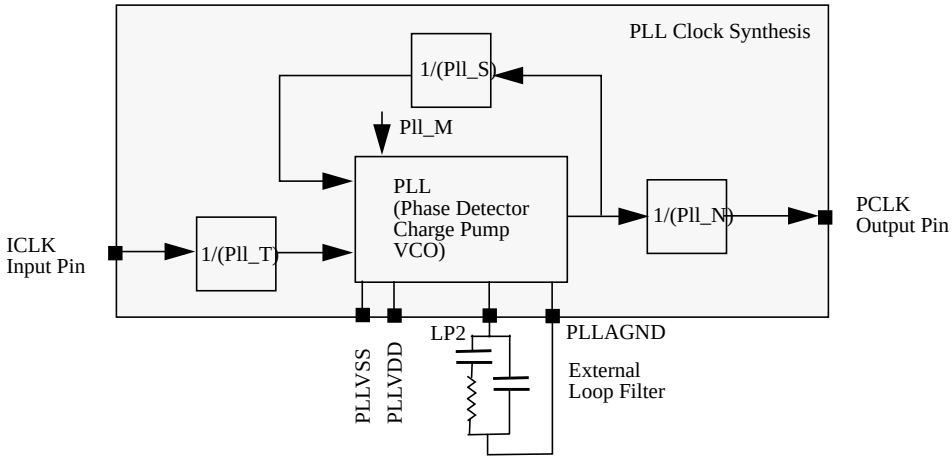
4.4 PLL Clock Generation

The data control and clocking schemes presented in chapter 4.1 outline the requirements for the generation of the two clock signals ICLK and OCLK that operate the device. The user has a choice to provide either an externally generated signal to the OCLK input or to make use of the internal PLL for clock synthesis by connecting the PLL output pin (PCLK) to the OCLK input pin as shown in the diagram below.



L64705 contains a clock synthesizer to derive OCLK from ICLK operating in the range of 2 MHz to 60 MHz. The synthesized clock is available on the PCLK output pin.

The PLL can be configured to handle clock ratios for the Viterbi code rates of 1/2, 2/3, 3/4, 5/6 and 7/8 (IS=0) as well as for the different data input formats when the Viterbi decoder is bypassed (IS=1). Four registers Pll_T[2:0], Pll_N[5:0], Pll_S[5:0] and Pll_M[1:0] must be set to derive the appropriate clock frequencies.



The recommended values for Pll_S, Pll_N, Pll_T and Pll_M to cover the frequency range from 2 - 60 MHz for PCLK are tabulated below:

IS = 0:

Code Rate	*Pll S[5:0]*	*Pll N[5:0]*	*Pll T[3:0]*	*Pll_M [1:0]*	*VCO min*	*VCO max*	*ICLK min*	*ICLK max*	*PCLK min*	*PCLK max*
1/2	2	1	2	3	70	80	70.00	80.00	*70.00	*80.00
1/2	2	1	2	2	60	70	60.00	70.00	60.00	*70.00
1/2	2	1	2	1	50	60	50.00	60.00	50.00	60.00
1/2	2	1	2	0	40	50	40.00	50.00	40.00	50.00
1/2	4	2	2	3	70	80	35.00	40.00	35.00	40.00
1/2	4	2	2	2	60	70	30.00	35.00	30.00	35.00
1/2	4	2	2	1	50	60	25.00	30.00	25.00	30.00
1/2	4	2	2	0	40	50	20.00	25.00	20.00	25.00
1/2	8	4	2	3	70	80	17.50	20.00	17.50	20.00
1/2	8	4	2	2	60	70	15.00	17.50	15.00	17.50
1/2	8	4	2	1	50	60	12.50	15.00	12.50	15.00
1/2	12	6	2	3	70	80	11.67	13.33	11.67	13.33
1/2	12	6	2	2	60	70	10.00	11.67	10.00	11.67
1/2	16	8	2	3	70	80	8.75	10.00	8.75	10.00
1/2	16	8	2	2	60	70	7.50	8.75	7.50	8.75

Code Rate	***Pll S[5:0]***	***Pll N[5:0]***	***Pll T[3:0]***	***Pll_M [1:0]***	***VCO min***	***VCO max***	***ICLK min***	***ICLK max***	***PCLK min***	***PCLK max***
1/2	16	8	2	1	50	60	6.25	7.50	6.25	7.50
1/2	16	8	2	0	40	50	5.00	6.25	5.00	6.25
1/2	20	10	2	0	40	50	4.00	5.00	4.00	5.00
1/2	24	12	2	0	40	50	3.33	4.17	3.33	4.17
1/2	28	14	2	0	40	50	2.86	3.57	2.86	3.57
1/2	32	16	2	0	40	50	2.50	3.12	2.50	3.12
1/2	36	18	2	0	40	50	2.22	2.78	2.22	2.78
1/2	40	20	2	0	40	50	2.00	2.50	2.00	2.50
2/3	8	1	6	3	70	80	52.50	60.00	*70.00	*80.00
2/3	8	1	6	2	60	70	45.00	52.50	60.00	*70.00
2/3	8	1	6	1	50	60	37.50	45.00	50.00	60.00
2/3	8	1	6	0	40	50	30.00	37.50	40.00	50.00
2/3	16	2	6	3	70	80	26.25	30.00	35.00	40.00
2/3	16	2	6	2	60	70	22.50	26.25	30.00	35.00
2/3	16	2	6	1	50	60	18.75	22.50	25.00	30.00
2/3	16	2	6	0	40	50	15.00	18.75	20.00	25.00
2/3	32	4	6	3	70	80	13.12	15.00	17.50	20.00
2/3	32	4	6	2	60	70	11.25	13.12	15.00	17.50
2/3	32	4	6	1	50	60	9.38	11.25	12.50	15.00
2/3	32	4	6	0	40	50	7.50	9.38	10.00	12.50
2/3	16	6	2	1	50	60	6.25	7.50	8.33	10.00
2/3	16	6	2	0	40	50	5.00	6.25	6.67	8.33
2/3	32	12	2	3	70	80	4.38	5.00	5.83	6.67
2/3	32	12	2	2	60	70	3.75	4.38	5.00	5.83
2/3	32	12	2	1	50	60	3.12	3.75	4.17	5.00
2/3	32	12	2	0	40	50	2.50	3.12	3.33	4.17
2/3	48	18	2	1	50	60	2.08	2.50	2.78	3.33
2/3	48	18	2	0	48	50	2.00	2.08	2.67	2.78
3/4	6	1	4	3	70	80	46.67	53.33	*70.00	*80.00
3/4	6	1	4	2	60	70	40.00	46.67	60.00	*70.00
3/4	6	1	4	1	50	60	33.33	40.00	50.00	60.00
3/4	6	1	4	0	40	50	26.67	33.33	40.00	50.00
3/4	6	2	2	3	70	80	23.33	26.67	35.00	40.00

Code Rate	***Pll S[5:0]***	***Pll N[5:0]***	***Pll T[3:0]***	***Pll_M [1:0]***	***VCO min***	***VCO max***	***ICLK min***	***ICLK max***	***PCLK min***	***PCLK max***
3/4	6	2	2	2	60	70	20.00	23.33	30.00	35.00
3/4	6	2	2	1	50	60	16.67	20.00	25.00	30.00
3/4	6	2	2	0	40	50	13.33	16.67	20.00	25.00
3/4	12	4	2	3	70	80	11.67	13.33	17.50	20.00
3/4	12	4	2	2	60	70	10.00	11.67	15.00	17.50
3/4	12	4	2	1	50	60	8.33	10.00	12.50	15.00
3/4	12	4	2	0	40	50	6.67	8.33	10.00	12.50
3/4	18	6	2	1	50	60	5.56	6.67	8.33	10.00
3/4	24	8	2	2	60	70	5.00	5.83	7.50	8.75
3/4	24	8	2	1	50	60	4.17	5.00	6.25	7.50
3/4	24	8	2	0	40	50	3.33	4.17	5.00	6.25
3/4	42	14	2	2	60	70	2.86	3.33	4.29	5.00
3/4	42	14	2	1	50	60	2.38	2.86	3.57	4.29
3/4	42	14	2	0	42	50	2.00	2.38	3.00	3.57
5/6	10	1	6	3	70	80	42.00	48.00	*70.00	*80.00
5/6	10	1	6	2	60	70	36.00	42.00	60.00	*70.00
5/6	10	1	6	1	50	60	30.00	36.00	50.00	60.00
5/6	10	1	6	0	40	50	24.00	30.00	40.00	50.00
5/6	20	2	6	3	70	80	21.00	24.00	35.00	40.00
5/6	20	2	6	2	60	70	18.00	21.00	30.00	35.00
5/6	20	2	6	1	50	60	15.00	18.00	25.00	30.00
5/6	20	2	6	0	40	50	12.00	15.00	20.00	25.00
5/6	40	4	6	3	70	80	10.50	12.00	17.50	20.00
5/6	40	4	6	2	60	70	9.00	10.50	15.00	17.50
5/6	40	4	6	1	50	60	7.50	9.00	12.50	15.00
5/6	40	4	6	0	40	50	6.00	7.50	10.00	12.50
5/6	20	6	2	1	50	60	5.00	6.00	8.33	10.00
5/6	20	6	2	0	40	50	4.00	5.00	6.67	8.33
5/6	40	12	2	3	70	80	3.50	4.00	5.83	6.67
5/6	40	12	2	2	60	70	3.00	3.50	5.00	5.83
5/6	40	12	2	1	50	60	2.50	3.00	4.17	5.00
5/6	40	12	2	0	40	50	2.00	2.50	3.33	4.17
7/8	14	1	8	3	70	80	40.00	45.71	*70.00	*80.00

Code Rate	*Pll S[5:0]*	*Pll N[5:0]*	*Pll T[3:0]*	*Pll_M [1:0]*	*VCO min*	*VCO max*	*ICLK min*	*ICLK max*	*PCLK min*	*PCLK max*
7/8	14	1	8	2	60	70	34.29	40.00	60.00	*70.00
7/8	14	1	8	1	50	60	28.57	34.29	50.00	60.00
7/8	14	1	8	0	40	50	22.86	28.57	40.00	50.00
7/8	14	2	4	3	70	80	20.00	22.86	35.00	40.00
7/8	14	2	4	2	60	70	17.14	20.00	30.00	35.00
7/8	14	2	4	1	50	60	14.29	17.14	25.00	30.00
7/8	14	2	4	0	40	50	11.43	14.29	20.00	25.00
7/8	14	4	2	3	70	80	10.00	11.43	17.50	20.00
7/8	14	4	2	2	60	70	8.57	10.00	15.00	17.50
7/8	14	4	2	1	50	60	7.14	8.57	12.50	15.00
7/8	42	6	4	3	70	80	6.67	7.62	11.67	13.33
7/8	42	6	4	2	60	70	5.71	6.67	10.00	11.67
7/8	28	8	2	3	70	80	5.00	5.71	8.75	10.00
7/8	28	8	2	2	60	70	4.29	5.00	7.50	8.75
7/8	28	8	2	1	50	60	3.57	4.29	6.25	7.50
7/8	42	12	2	3	70	80	3.33	3.81	5.83	6.67
7/8	42	12	2	2	60	70	2.86	3.33	5.00	5.83
7/8	42	12	2	1	50	60	2.38	2.86	4.17	5.00
7/8	42	12	2	0	42	50	2.00	2.38	3.50	4.17

IS = 1 (Viterbi Decoder bypassed)

Symbol Width	*Pll S[5:0]*	*Pll N[5:0]*	*Pll T[3:0]*	*Pll_M [1:0]*	*VCO min*	*VCO max*	*ICLK min*	*ICLK max*	*PCLK min*	*PCLK max*
1	2	1	2	2	60	70	60.00	*70.00	60.00	*70.00
1	2	1	2	1	50	60	50.00	60.00	50.00	60.00
1	2	1	2	0	40	50	40.00	50.00	40.00	50.00
1	4	2	2	3	70	80	35.00	40.00	35.00	40.00
1	4	2	2	2	60	70	30.00	35.00	30.00	35.00
1	4	2	2	1	50	60	25.00	30.00	25.00	30.00
1	4	2	2	0	40	50	20.00	25.00	20.00	25.00
1	8	4	2	3	70	80	17.50	20.00	17.50	20.00
1	8	4	2	2	60	70	15.00	17.50	15.00	17.50
1	8	4	2	1	50	60	12.50	15.00	12.50	15.00

Symbol Width	*Pll S[5:0]*	*Pll N[5:0]*	*Pll T[3:0]*	*Pll_M [1:0]*	*VCO min*	*VCO max*	*ICLK min*	*ICLK max*	*PCLK min*	*PCLK max*
1	8	4	2	0	40	50	10.00	12.50	10.00	12.50
1	16	8	2	3	70	80	8.75	10.00	8.75	10.00
1	16	8	2	2	60	70	7.50	8.75	7.50	8.75
1	16	8	2	1	50	60	6.25	7.50	6.25	7.50
1	16	8	2	0	40	50	5.00	6.25	5.00	6.25
1	24	12	2	2	60	70	5.00	5.83	5.00	5.83
1	24	12	2	1	50	60	4.17	5.00	4.17	5.00
1	24	12	2	0	40	50	3.33	4.17	3.33	4.17
1	48	24	2	3	70	80	2.92	3.33	2.92	3.33
1	48	24	2	2	60	70	2.50	2.92	2.50	2.92
2	4	1	2	3	70	80	35.00	40.00	*70.00	*80.00
2	4	1	2	2	60	70	30.00	35.00	60.00	*70.00
2	4	1	2	1	50	60	25.00	30.00	50.00	60.00
2	4	1	2	0	40	50	20.00	25.00	40.00	50.00
2	8	2	2	3	70	80	17.50	20.00	35.00	40.00
2	8	2	2	2	60	70	15.00	17.50	30.00	35.00
2	8	2	2	1	50	60	12.50	15.00	25.00	30.00
2	8	2	2	0	40	50	10.00	12.50	20.00	25.00
2	16	4	2	3	70	80	8.75	10.00	17.50	20.00
2	16	4	2	2	60	70	7.50	8.75	15.00	17.50
2	16	4	2	1	50	60	6.25	7.50	12.50	15.00
2	16	4	2	0	40	50	5.00	6.25	10.00	12.50
2	32	8	2	3	70	80	4.38	5.00	8.75	10.00
2	32	8	2	2	60	70	3.75	4.38	7.50	8.75
2	32	8	2	1	50	60	3.12	3.75	6.25	7.50
2	32	8	2	0	40	50	2.50	3.12	5.00	6.25
2	40	10	2	0	40	50	2.00	2.50	4.00	5.00
3	6	1	2	3	70	80	23.33	26.67	*70.00	*80.00
3	6	1	2	2	60	70	20.00	23.33	60.00	*70.00
3	6	1	2	1	50	60	16.67	20.00	50.00	60.00
3	6	1	2	0	40	50	13.33	16.67	40.00	50.00
3	12	2	2	3	70	80	11.67	13.33	35.00	40.00
3	12	2	2	2	60	70	10.00	11.67	30.00	35.00

Symbol Width	*Pll S[5:0]*	*Pll N[5:0]*	*Pll T[3:0]*	*Pll_M [1:0]*	*VCO min*	*VCO max*	*ICLK min*	*ICLK max*	*PCLK min*	*PCLK max*
3	12	2	2	1	50	60	8.33	10.00	25.00	30.00
3	12	2	2	0	40	50	6.67	8.33	20.00	25.00
3	24	4	2	3	70	80	5.83	6.67	17.50	20.00
3	24	4	2	2	60	70	5.00	5.83	15.00	17.50
3	24	4	2	1	50	60	4.17	5.00	12.50	15.00
3	24	4	2	0	40	50	3.33	4.17	10.00	12.50
3	48	8	2	3	70	80	2.92	3.33	8.75	10.00
3	48	8	2	2	60	70	2.50	2.92	7.50	8.75
3	48	8	2	1	50	60	2.08	2.50	6.25	7.50
3	48	8	2	0	48	50	2.00	2.08	6.00	6.25
4	8	1	2	3	70	80	17.50	20.00	*70.00	*80.00
4	8	1	2	2	60	70	15.00	17.50	60.00	*70.00
4	8	1	2	1	50	60	12.50	15.00	50.00	60.00
4	8	1	2	0	40	50	10.00	12.50	40.00	50.00
4	16	2	2	3	70	80	8.75	10.00	35.00	40.00
4	16	2	2	2	60	70	7.50	8.75	30.00	35.00
4	16	2	2	1	50	60	6.25	7.50	25.00	30.00
4	16	2	2	0	40	50	5.00	6.25	20.00	25.00
4	32	4	2	3	70	80	4.38	5.00	17.50	20.00
4	32	4	2	2	60	70	3.75	4.38	15.00	17.50
4	32	4	2	1	50	60	3.12	3.75	12.50	15.00
4	32	4	2	0	40	50	2.50	3.12	10.00	12.50
4	48	6	2	1	50	60	2.08	2.50	8.33	10.00
4	48	6	2	0	48	50	2.00	2.08	8.00	8.33
5	10	1	2	3	70	80	14.00	16.00	*70.00	*80.00
5	10	1	2	2	60	70	12.00	14.00	60.00	*70.00
5	10	1	2	1	50	60	10.00	12.00	50.00	60.00
5	10	1	2	0	40	50	8.00	10.00	40.00	50.00
5	20	2	2	3	70	80	7.00	8.00	35.00	40.00
5	20	2	2	2	60	70	6.00	7.00	30.00	35.00
5	20	2	2	1	50	60	5.00	6.00	25.00	30.00
5	20	2	2	0	40	50	4.00	5.00	20.00	25.00
5	40	4	2	3	70	80	3.50	4.00	17.50	20.00

Symbol Width	*Pll S[5:0]*	*Pll N[5:0]*	*Pll T[3:0]*	*Pll_M [1:0]*	*VCO min*	*VCO max*	*ICLK min*	*ICLK max*	*PCLK min*	*PCLK max*
5	40	4	2	2	60	70	3.00	3.50	15.00	17.50
5	40	4	2	1	50	60	2.50	3.00	12.50	15.00
5	40	4	2	0	40	50	2.00	2.50	10.00	12.50
6	12	1	2	3	70	80	11.67	13.33	*70.00	*80.00
6	12	1	2	2	60	70	10.00	11.67	60.00	70.00
6	12	1	2	1	50	60	8.33	10.00	50.00	60.00
6	12	1	2	0	40	50	6.67	8.33	40.00	50.00
6	24	2	2	3	70	80	5.83	6.67	35.00	40.00
6	24	2	2	2	60	70	5.00	5.83	30.00	35.00
6	24	2	2	1	50	60	4.17	5.00	25.00	30.00
6	24	2	2	0	40	50	3.33	4.17	20.00	25.00
6	48	4	2	3	70	80	2.92	3.33	17.50	20.00
6	48	4	2	2	60	70	2.50	2.92	15.00	17.50
6	48	4	2	1	50	60	2.08	2.50	12.50	15.00
6	48	4	2	0	48	50	2.00	2.08	12.00	12.50
7	14	1	2	3	70	80	10.00	11.43	*70.00	*80.00
7	14	1	2	2	60	70	8.57	10.00	60.00	*70.00
7	14	1	2	1	50	60	7.14	8.57	50.00	60.00
7	14	1	2	0	40	50	5.71	7.14	40.00	50.00
7	28	2	2	3	70	80	5.00	5.71	35.00	40.00
7	28	2	2	2	60	70	4.29	5.00	30.00	35.00
7	28	2	2	1	50	60	3.57	4.29	25.00	30.00
7	28	2	2	0	40	50	2.86	3.57	20.00	25.00
7	56	4	2	3	70	80	2.50	2.86	17.50	20.00
7	56	4	2	2	60	70	2.14	2.50	15.00	17.50
7	56	4	2	1	56	60	2.00	2.14	14.00	15.00
8	16	1	2	3	70	80	8.75	10.00	*70.00	*80.00
8	16	1	2	2	60	70	7.50	8.75	60.00	*70.00
8	16	1	2	1	50	60	6.25	7.50	50.00	60.00
8	16	1	2	0	40	50	5.00	6.25	40.00	50.00
8	32	2	2	3	70	80	4.38	5.00	35.00	40.00
8	32	2	2	2	60	70	3.75	4.38	30.00	35.00

Symbol Width	Pll S[5:0]	Pll N[5:0]	Pll T[3:0]	Pll_M [1:0]	VCO min	VCO max	ICLK min	ICLK max	PCLK min	PCLK max
8	32	2	2	1	50	60	3.12	3.75	25.00	30.00
8	32	2	2	0	40	50	2.50	3.12	20.00	25.00

Note:

(*) : Although the PLL module is capable of generating PCLK frequencies of up to 80 MHz, the maximum OCLK frequency is still limited to 60 MHz.

4.5 Data Path Input Configurations

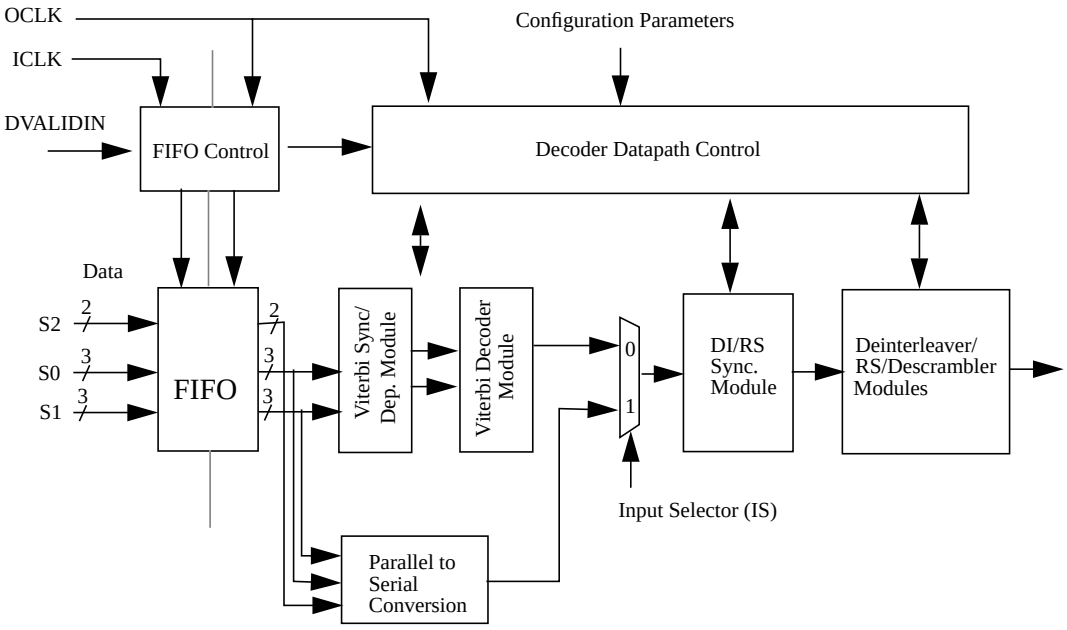
The L64705 data path input can be configured into two modes that include or bypass the Viterbi decoder module respectively.

In addition to operating the device as a full concatenated decoder (Input Selector IS =0) that includes the Viterbi decoder module the user has the choice to bypass the Viterbi section (Input Selector IS =1).

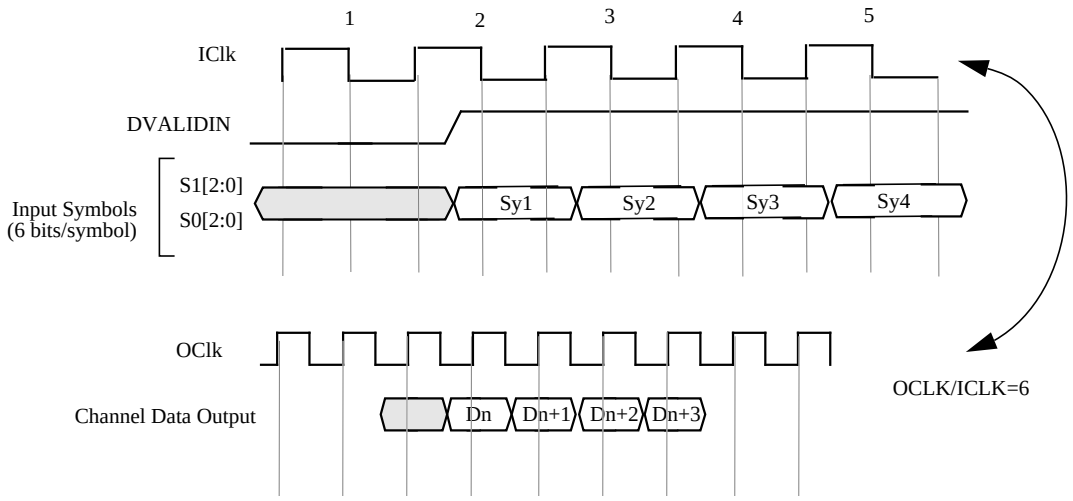
For Input Selector IS =0 data is input on S0[2:0] and S1[2:0] representing the two 3-bit soft decision symbols for QSPK/BPSK modes of operation. FIFO output data is delivered to the Viterbi synchronization and depuncturing module before being convolutionaly decoded in the Viterbi decoder core. The decoded Viterbi data is supplied as a serial stream to the Deinterleaver/Reed-Solomon Decoder Synchronization module.

When IS =1 is selected data is input on S0[2:0], S1[2:0] and S2[1:0] representing data symbols of 1 up to 8 bits per symbol for operating modes such a QAM. The incoming data is fed from the chip input through the FIFO directly to the Deinterleaver/Reed-Solomon Synchronization module.

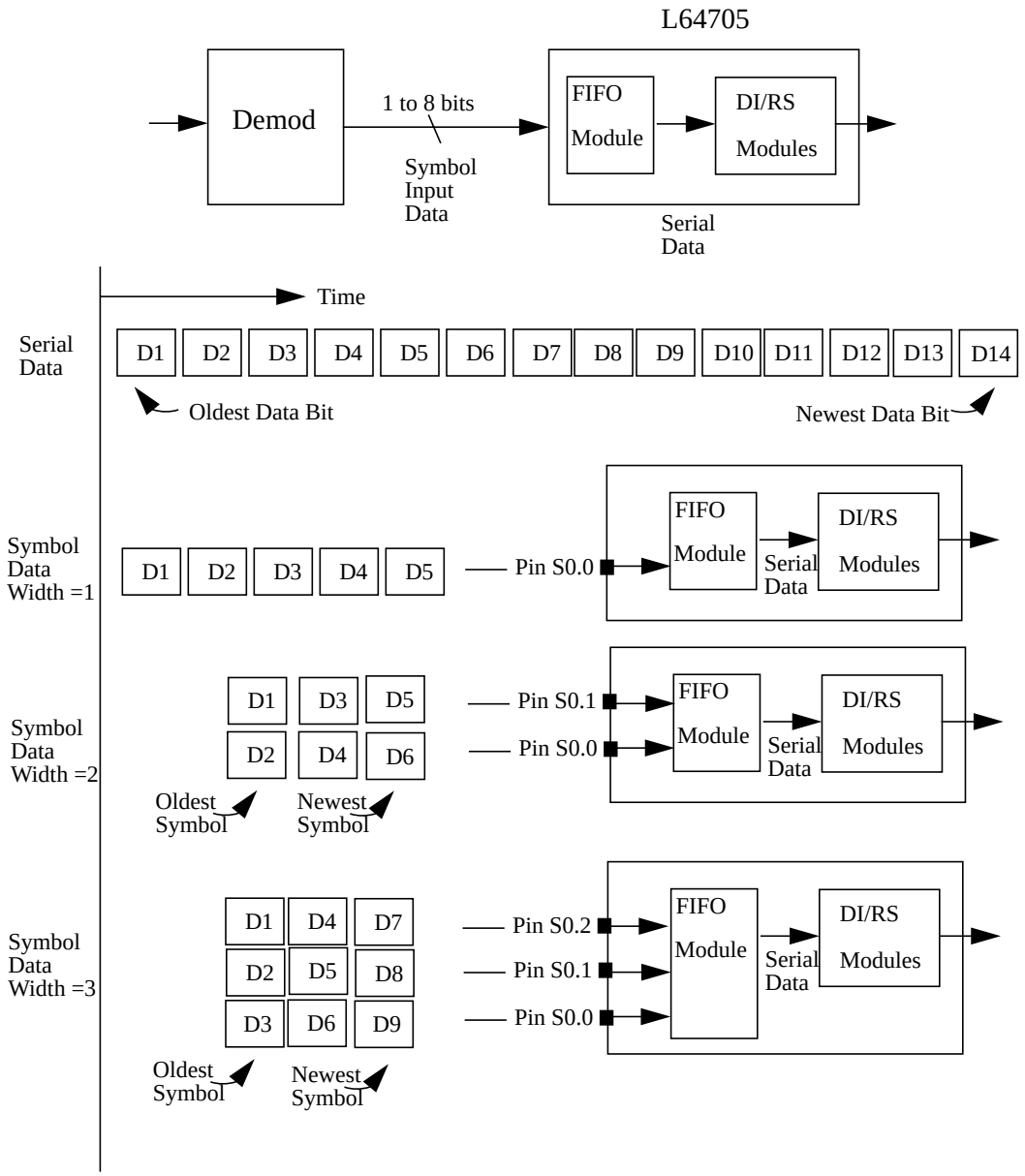
The specifc number of bits assigned to a symbol is set by the BPS[2:0] paramter in the configuration registers. For symbol widths of up to six bits the inputs S0[2:0] and S1[2:0] are utlilized. In the case of seven or eight bits per symbol the input pins S2[1:0] are being used in addition.

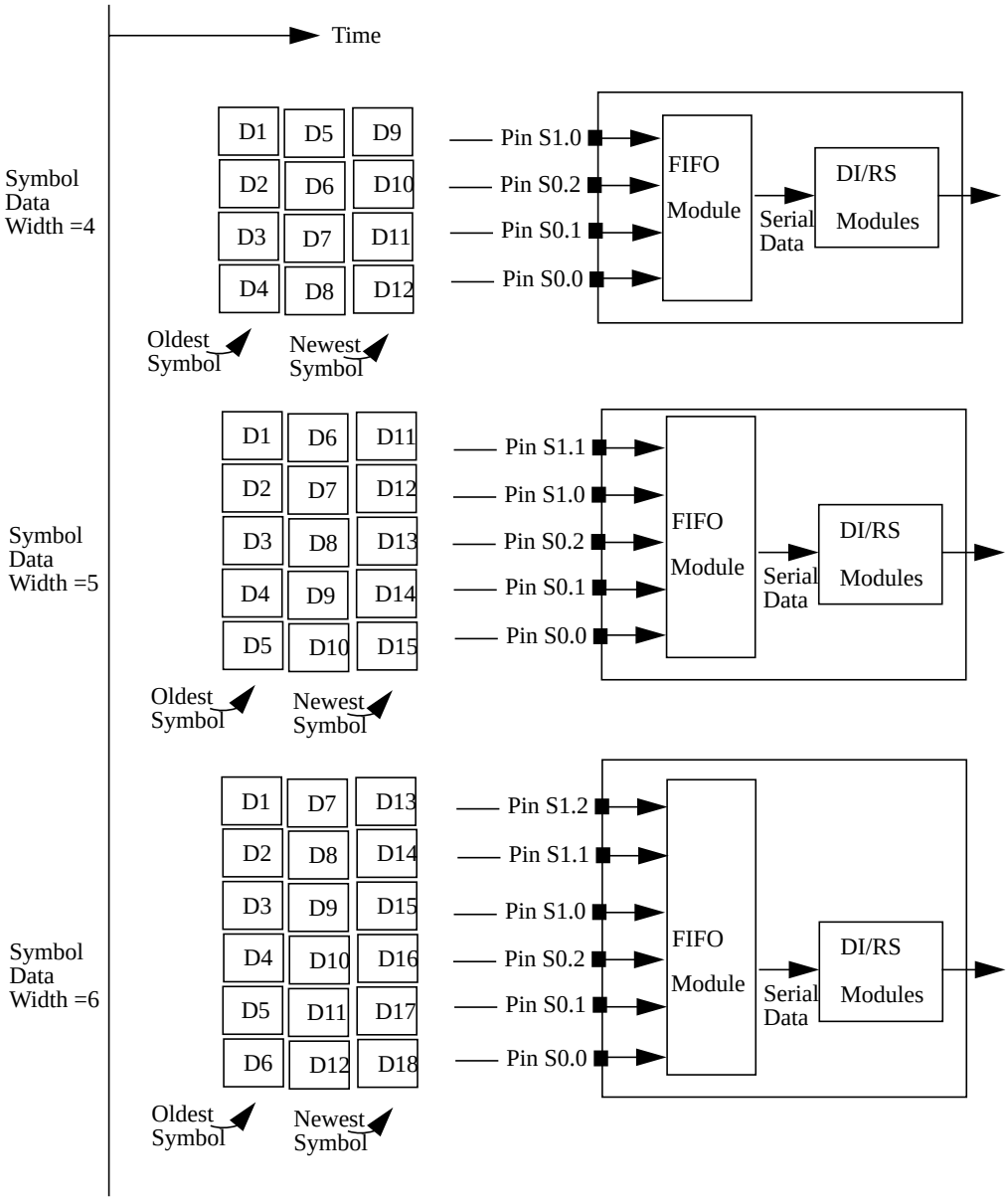


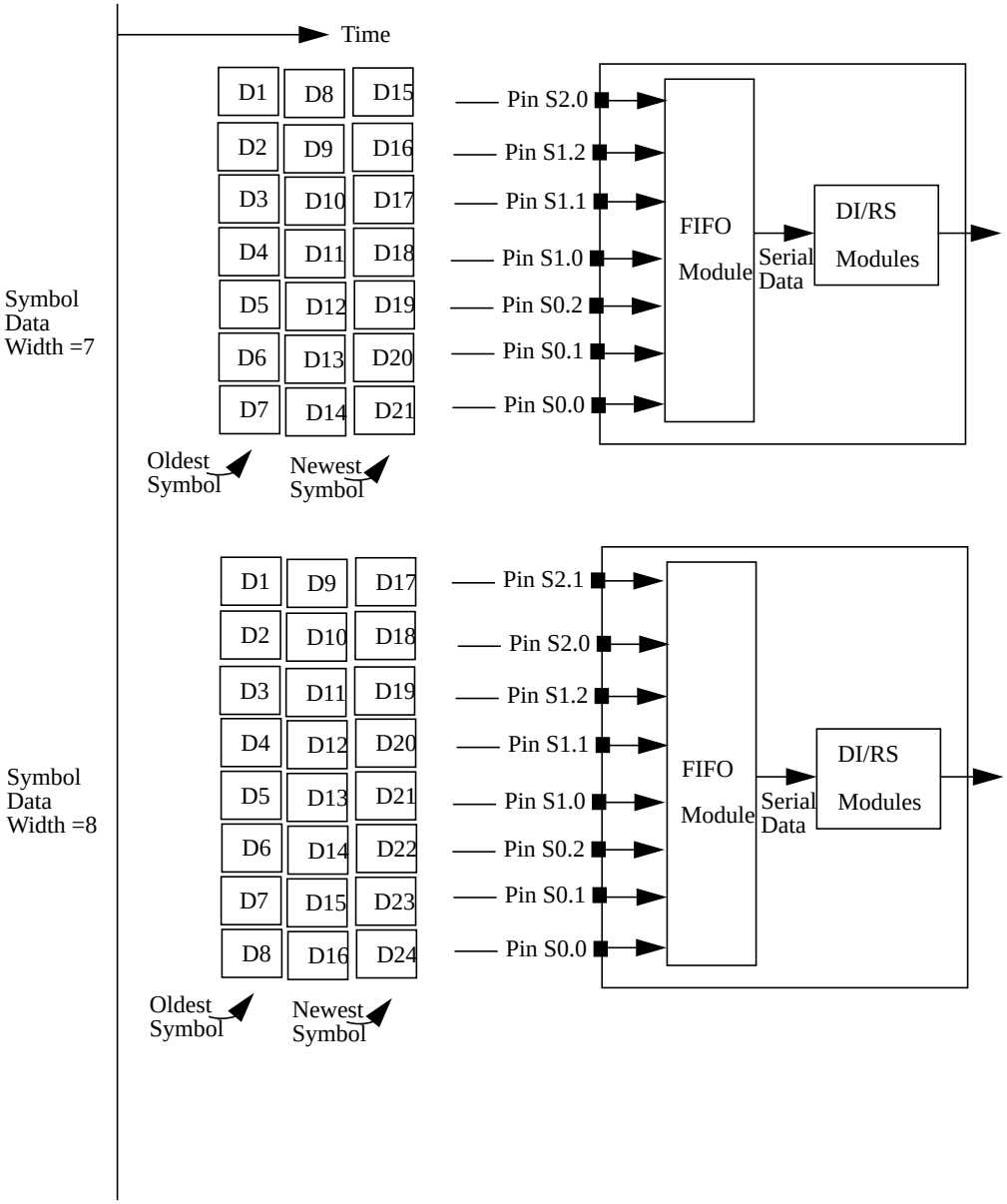
As sample set of input waveforms is shown for the case of 6 bits/symbol (IS=1, BPS[2:0]=010b). Observe that in this case the ratio of OCLK and ICLK is dictated by the number of bits/symbol: OCLK/ICLK=6.



The following signal assignments are used for the different symbol widths in the case of a bypassed Viterbi decoder:


L64705
Demod
1 to 8 bits
Symbol
Input
Data
FIFO
Module
DI/RS
Modules
Serial
Data
Time
Serial
Data
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
Oldest Data Bit
Newest Data Bit
Symbol
Data
Width =1
Pin S0.0
Symbol
Data
Width =2
Pin S0.1
Pin S0.0
Oldest
Symbol
Newest
Symbol
Symbol
Data
Width =3
Pin S0.2
Pin S0.1
Pin S0.0

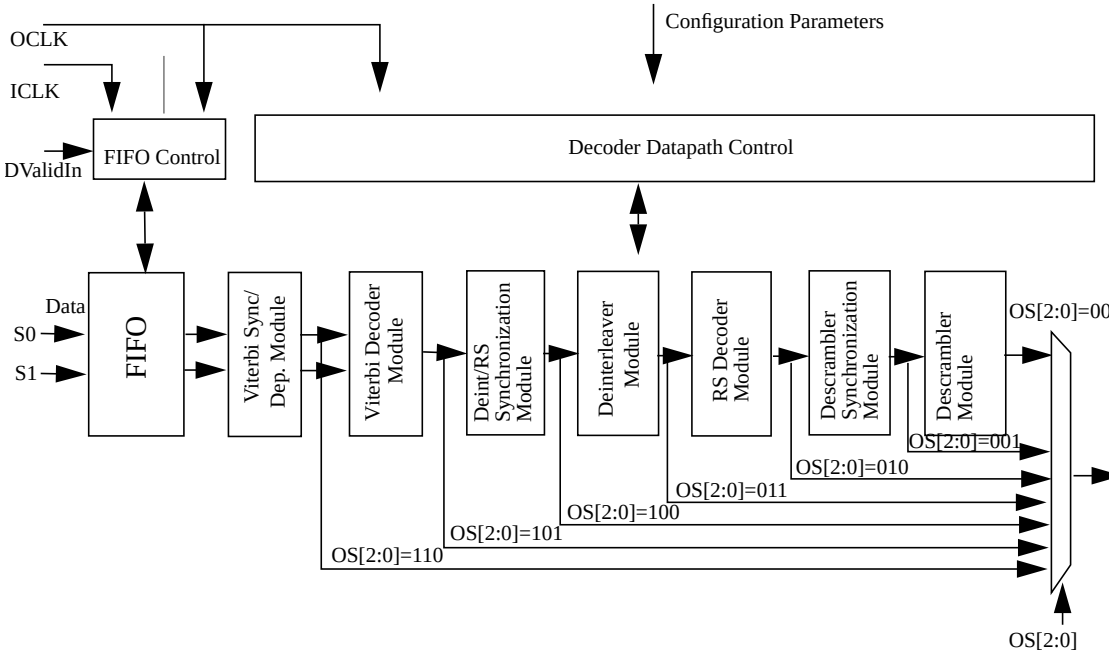

Time
Symbol Data Width =4
D1
D5
D9
D2
D6
D10
D3
D7
D11
D4
D8
D12
Pin S1.0
Pin S0.2
Pin S0.1
Pin S0.0
FIFO Module
Serial Data
DI/RS Modules
Oldest Symbol
Newest Symbol
Symbol Data Width =5
D1
D6
D11
D2
D7
D12
D3
D8
D13
D4
D9
D14
D5
D10
D15
Pin S1.1
Pin S1.0
Pin S0.2
Pin S0.1
Pin S0.0
FIFO Module
Serial Data
DI/RS Modules
Oldest Symbol
Newest Symbol
Symbol Data Width =6
D1
D7
D13
D2
D8
D14
D3
D9
D15
D4
D10
D16
D5
D11
D17
D6
D12
D18
Pin S1.2
Pin S1.1
Pin S1.0
Pin S0.2
Pin S0.1
Pin S0.0
FIFO Module
Serial Data
DI/RS Modules
Oldest Symbol
Newest Symbol


Time
Symbol Data Width =7
D1
D8
D15
D2
D9
D16
D3
D10
D17
D4
D11
D18
D5
D12
D19
D6
D13
D20
D7
D14
D21
Pin S2.0
Pin S1.2
Pin S1.1
Pin S1.0
Pin S0.2
Pin S0.1
Pin S0.0
FIFO Module
Serial Data
DI/RS Modules
Oldest Symbol
Newest Symbol
Symbol Data Width =8
D1
D9
D17
D2
D10
D18
D3
D11
D19
D4
D12
D20
D5
D13
D21
D6
D14
D22
D7
D15
D23
D8
D16
D24
Pin S2.1
Pin S2.0
Pin S1.2
Pin S1.1
Pin S1.0
Pin S0.2
Pin S0.1
Pin S0.0
FIFO Module
Serial Data
DI/RS Modules
Oldest Symbol
Newest Symbol

4.6 Data Path Output Configurations

The L64705 incorporates a number of configuration options that are targeted at providing the user with a mechanism to access parts of the decoding pipeline individually. In particular, performance characterization and system diagnostics tasks are simplified.

In addition to the Descrambler Output, the Reed-Solomon decoder, the Viterbi Decoder and Deinterleaver module outputs can be propagated to the existing device data output interface. The pins CO[7:0], DValidOut, ErrorFix, ErrorOut, FStartOut will carry the output data and strobes of the respective module chosen.

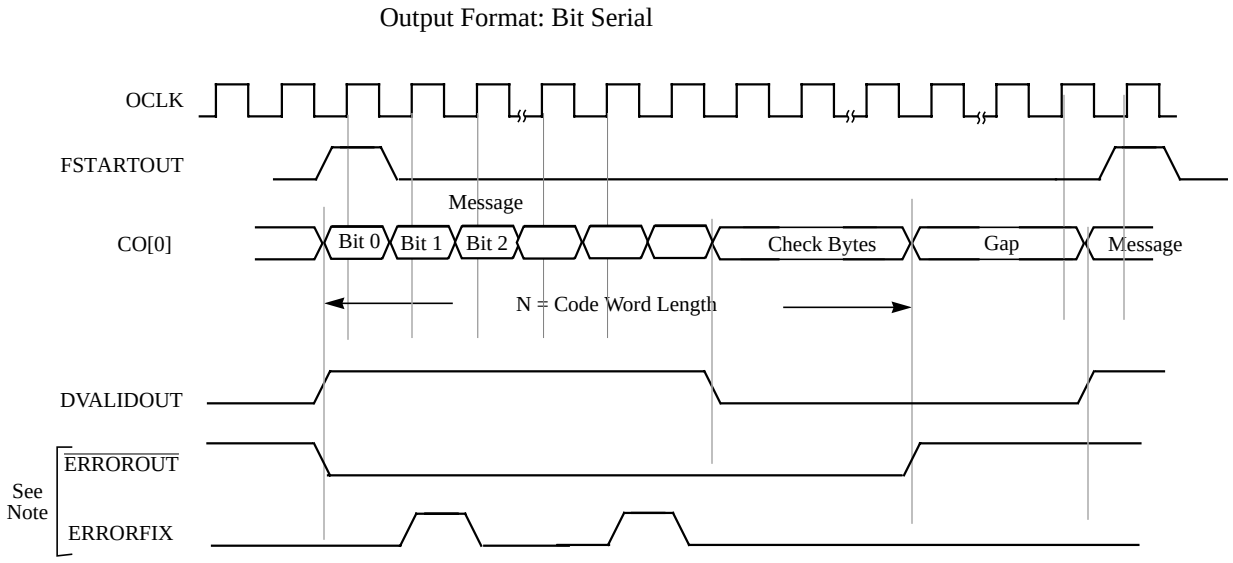


Descrambler Output

Output Selector OS[2:0] =000_2

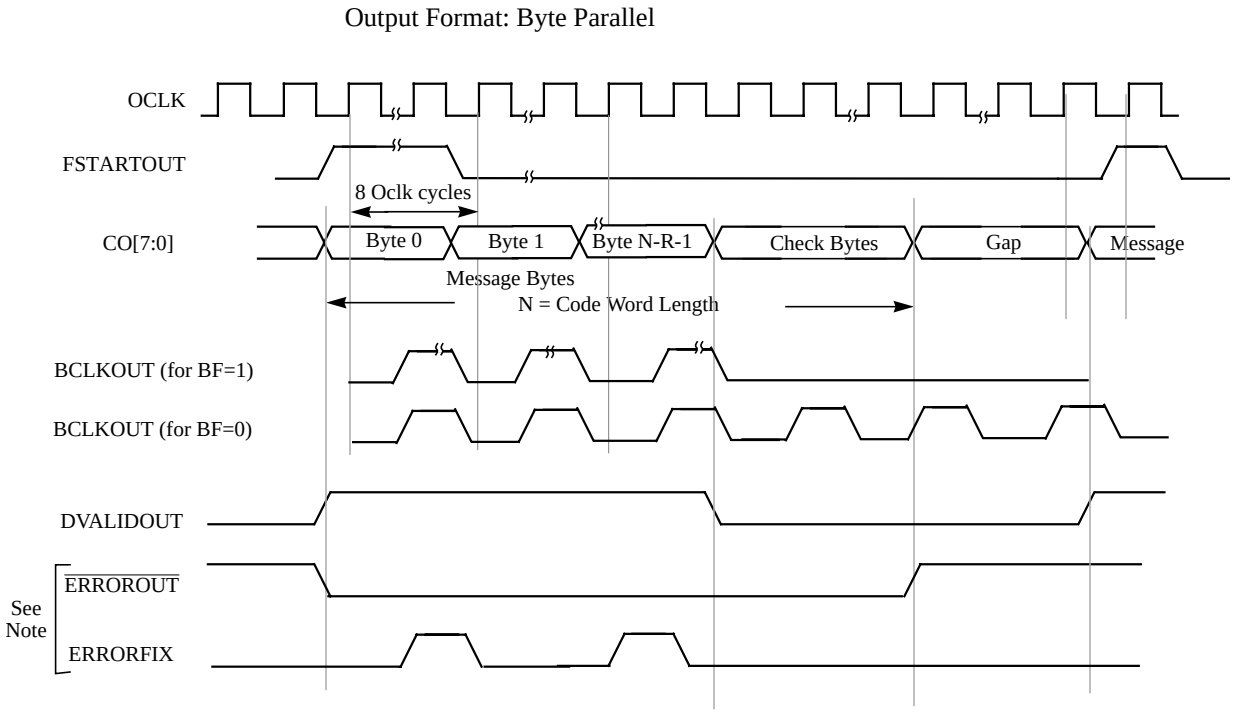
This configuration produces the output of the entire decoding pipeline. The output waveforms are shown below.

Figure 4.1
Descrambler Serial
Output waveforms



When the bit serial output mode is chosen (Output Format OF =0_2) only the LBS on the CO bus (CO[0]) is active. New data is output one bit per cycle of OCLK. FSTARTOUT is active for one cycle and overlaps the first message bit of a Reed-Solomon code word.

Figure 4.2
Descrambler
Parallel Output
waveforms



When the byte parallel mode is selected (Output Format OF =1_2) one new data byte is output on C0[7:0] every eight OCLK cycles. The chronological order in parallel output mode is MSB oldest, LSB newest. The FSTARTOUT strobe overlaps the first data byte. BCLKOUT is provided as an additional strobe and shows one rising and one falling edge per valid CO[7:0] data byte when the BF configuration bit is set HIGH . It is positioned in the middle of the decoded data bytes and can be used by devices following L64705 to latch data at the BLKOUT rate rather than at the OCLK rate. BCLKOUT is a continuous clock output at 1/8 the OCLK frequency when BF is set LOW regardless of whether valid data is present on

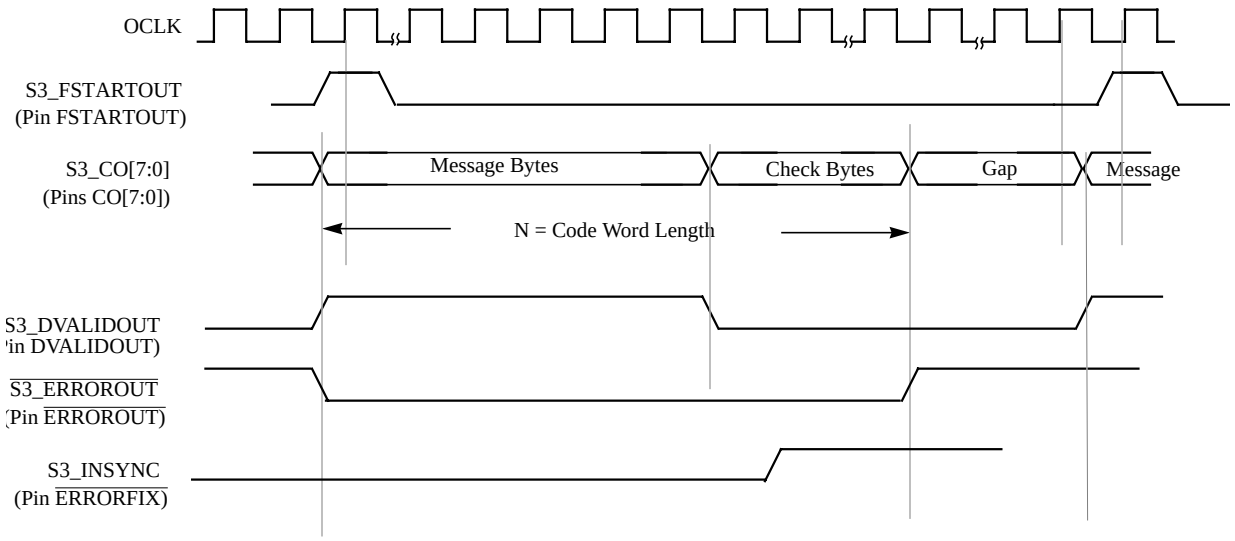
the CO bus or not. (*: Note that ERROROUT and ERRORFIX are never active at the same time).

Synchronization Stage 3 Output

Output Selector OS[2:0] =001_2

This configuration produces the outputs of the synchronization stage preceding the descrambler. The pin assignment from Sync3 outputs to L64705 chip output pins shown in the diagram.

Figure 4.3 Synchronization Stage 3 Output Waveforms



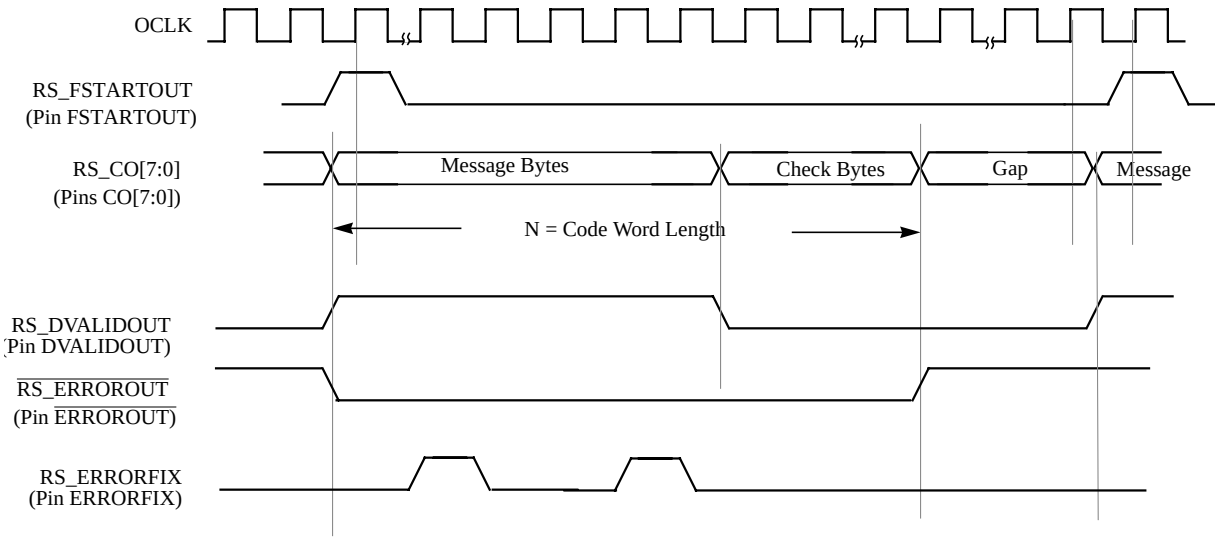
In difference to the descrambler output the CO bus carries the still scrambled data. Pin ERRORFIX (S3_INSYNC) is being used to monitor the state of the third synchronization stage. A HIGH S3_INSYNC indicates that the descrambler synchronization has been established, LOW indicates an out of sync condition.

Reed-Solomon Decoder Output

Output Selector OS[2:0] =010_2

This configuration produces the outputs of the Reed-Solomon decoder module. The mode is relevant for all users who wish to bypass the descrambler entirely.

Figure 4.4
Reed-Solomon
Decoder Output
Waveforms

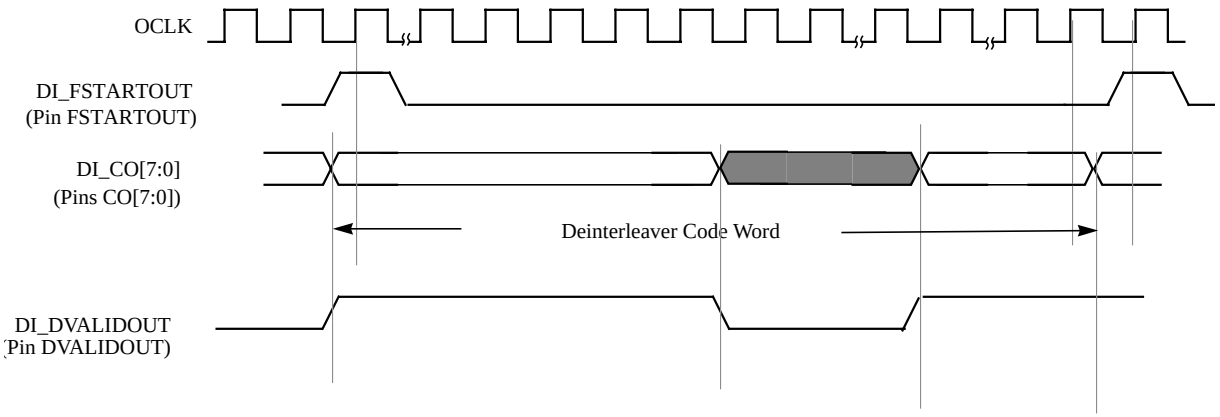


Deinterleaver Output

Output Selector OS[2:0] =011_2

This configuration produces the outputs of the Convolutional Deinterleaver.

Figure 4.5
Deinterleaver
Output Waveforms



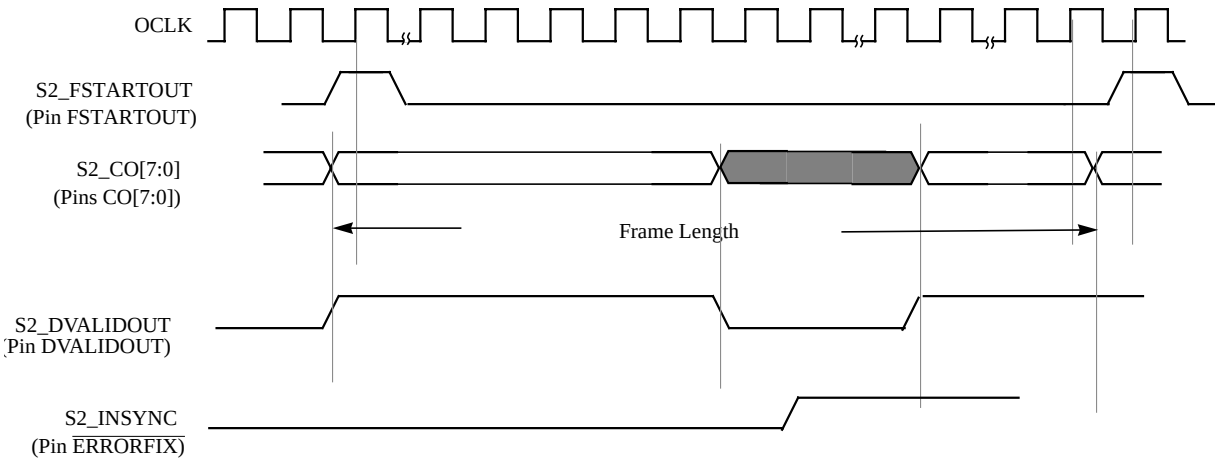
Pins FSTARTOUT, CO and DVALIDOUT are used for the corresponding Deinterleaver outputs. Pins ERROROUT and ERRORFIX are not used in this case and should be disregarded.

Synchronization Stage 2 Output

Output Selector OS[2:0] =100_2

This configuration produces the outputs of the synchronization stage preceding the deinterleaver. It detects the predefined synchronization word to properly align the data stream.

Figure 4.6
Synchronization
Stage 2 Output
Waveforms



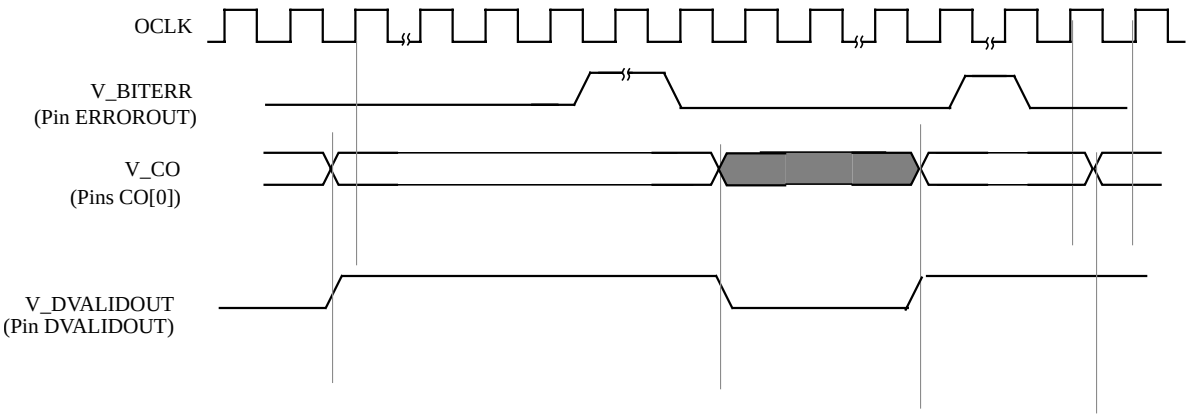
Pin ERRORFIX (S2_INSYNC) is being used to monitor the state of the second synchronization stage. A HIGH S2_INSYNC indicates that frame synchronization has been established, LOW indicates an out of sync condition. Pin ERROROUT is not used in this case and should be disregarded.

Viterbi Decoder Output

Output Selector OS[2:0] =101_2

This configuration produces the outputs of the Viterbi decoder module. Users who wish to observe the decoded data after the inner layer of decoding only should use this mode.

Figure 4.7
Viterbi Decoder
Output Waveforms



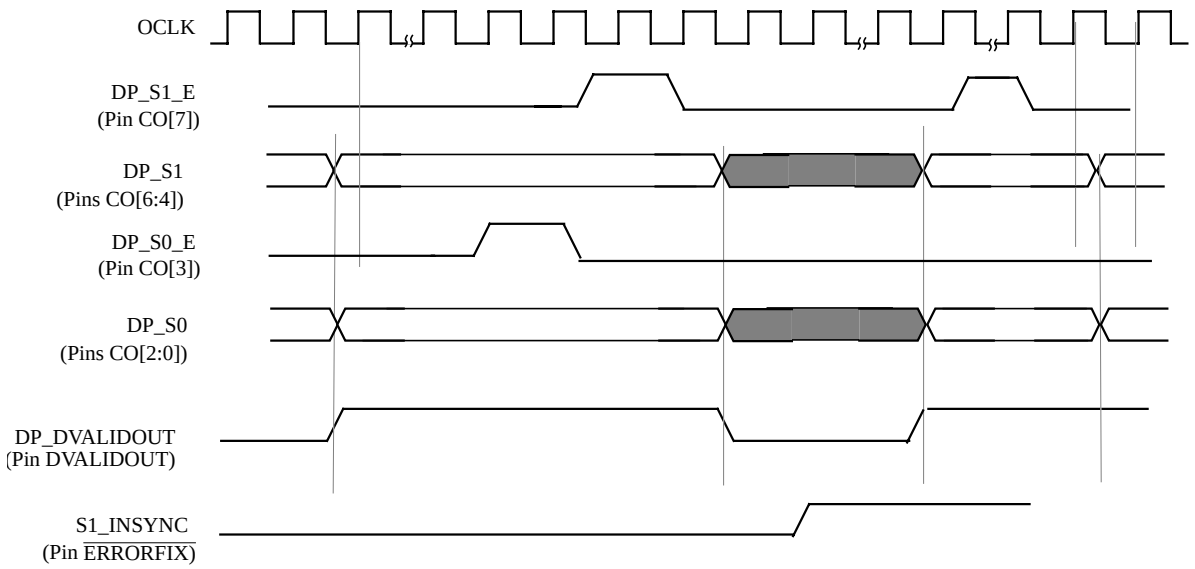
The decoded Viterbi data stream (V_CO) is output serially on pin CO[0] one bit per OCLK cycle. Pin DVALIDOUT indicates whether data on CO[0] is valid on a cycle-by-cycle basis. ERROROUT (V_BITERR) carries information on errors found in the Viterbi output bit stream. A HIGH on ERROROUT indicates that the current on V_CO is not decoded correctly. ERRORFIX is not used and should be disregarded.

Viterbi Depuncture/ Synchronization Output

Output Selector OS[2:0] = 110_2

The outputs of the Viterbi synchronization stage and the associated depuncturing module are propagated to the chip level outputs.

Figure 4.8
Viterbi
Synchronization/
Depuncture Output
Waveforms



The depunctured Viterbi input data stream, consisting of symbol streams (DP_S0, DP_S1) and two corresponding erasures flags (DP_SO_E, DP_S1_E) are presented on the CO bus as noted above. Pin ERRORFIX (S1_INSYNC) is being used to monitor the state of the Viterbi synchronization stage. A HIGH S1_INSYNC indicates that the Viterbi module synchronization has been established, LOW indicates an out-of-sync condition. Pin ERROROUT is not used and should be disregarded.

Chapter 5
Synchronization

5.1 Overview

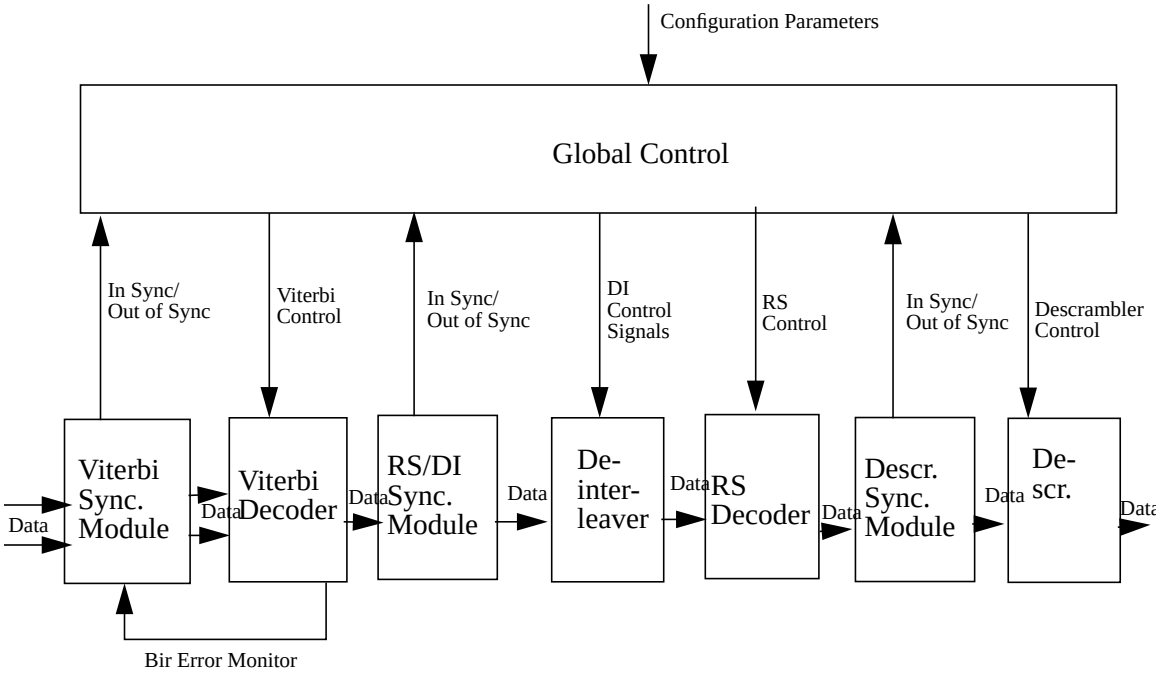
The L64705 decoder contains a configurable synchronization circuit for aligning the Viterbi, Deinterleaver, RS decoder and Descrambler to the overall frame structure. The input to the device will be a two 3-bit symbols. The maximum information rate is 60 Mbits/sec at rate 1/2 operation.

A global control module generates the control signals for Viterbi, Descrambler, Deinterleaver and Reed-Solomon decoder cores. In particular, the appropriate sequencing of the sync signals under in/out of synchronization is handled.

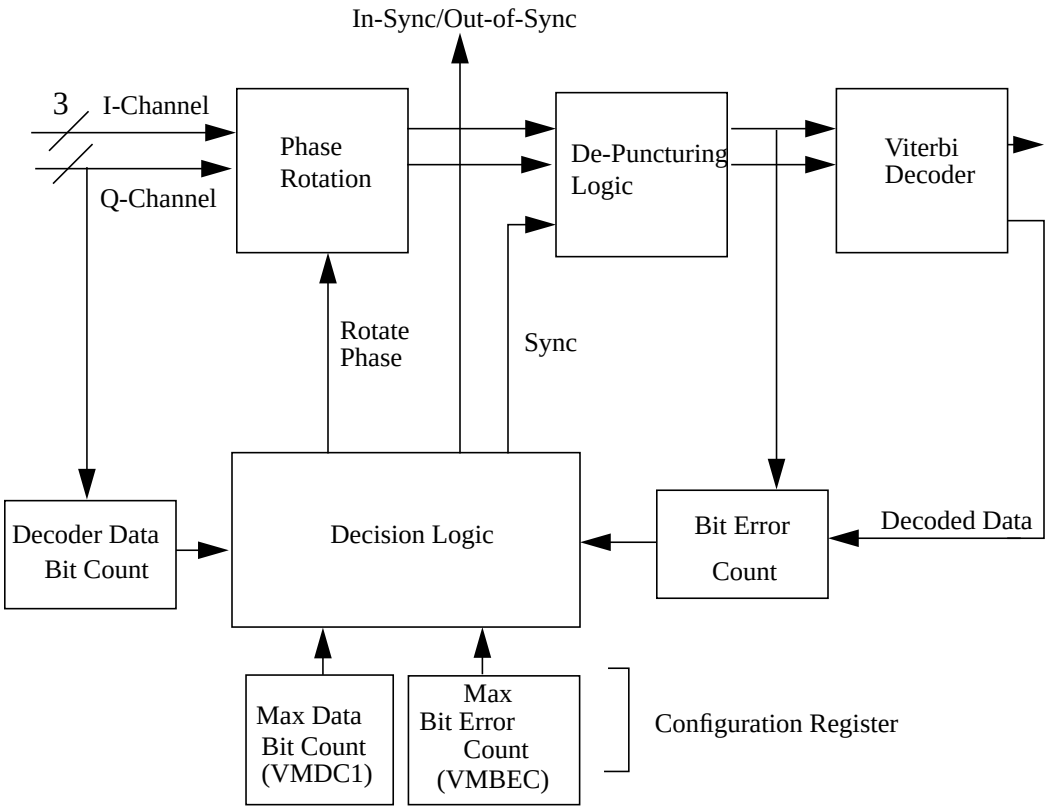
The block diagram below shows the position of, and major connections to the synchronization module.

5.2 Synchronization Scheme

The device level synchronization scheme chosen breaks down into a three stage synchronization process: Synchronization using output statistics of the Viterbi decoder module for the first stage, identification of a synchronization word for the second stage and identification of an inverted synchronization word for the third stage.


Configuration Parameters
Global Control
In Sync/
Out of Sync
Viterbi
Control
In Sync/
Out of Sync
DI
Control
Signals
RS
Control
In Sync/
Out of Sync
Descrambler
Control
Viterbi
Sync.
Module
Viterbi
Decoder
RS/DI
Sync.
Module
De-
inter-
leaver
RS
Decoder
Descr.
Sync.
Module
De-
scr.
Data
Bir Error Monitor

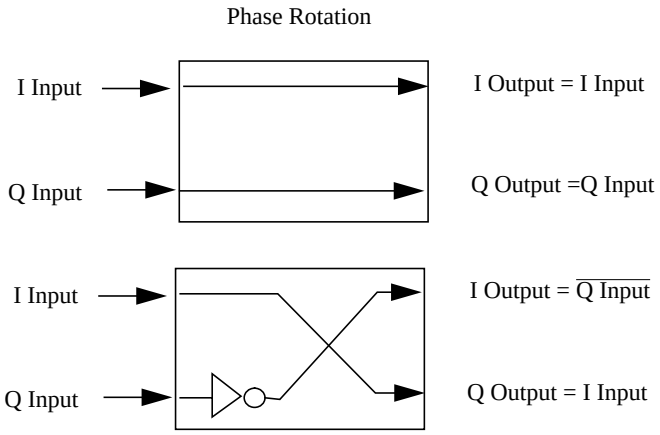
Viterbi Decoder Synchronization



The first stage (Viterbi decoder synchronization) determines the in/out of sync condition by observing the valid data symbols and the bit errors in the decoded data stream. The Max Data Bit Count configuration register sets the number of valid data bits at the output of the Viterbi decoder over which the number of channel symbol errors are to be counted. Whenever during that interval the bit error count is above the value specified in the Max Bit Error Count register the decision logic flags an out-of-sync condition and proceeds to adjust the phase in the phase rotation module or the data stream alignment in the depuncturing logic by successively stepping through as many as needed and possibly all combinations until synchronization is achieved. Since both I and Q channel have a chance of appearing

inverted and swapped there are four possible phases for the phase rotation block. Depending on the Viterbi code rate chosen the depuncturing mechanism includes up to four states.

The following diagram outlines the operations performed during phase rotation:

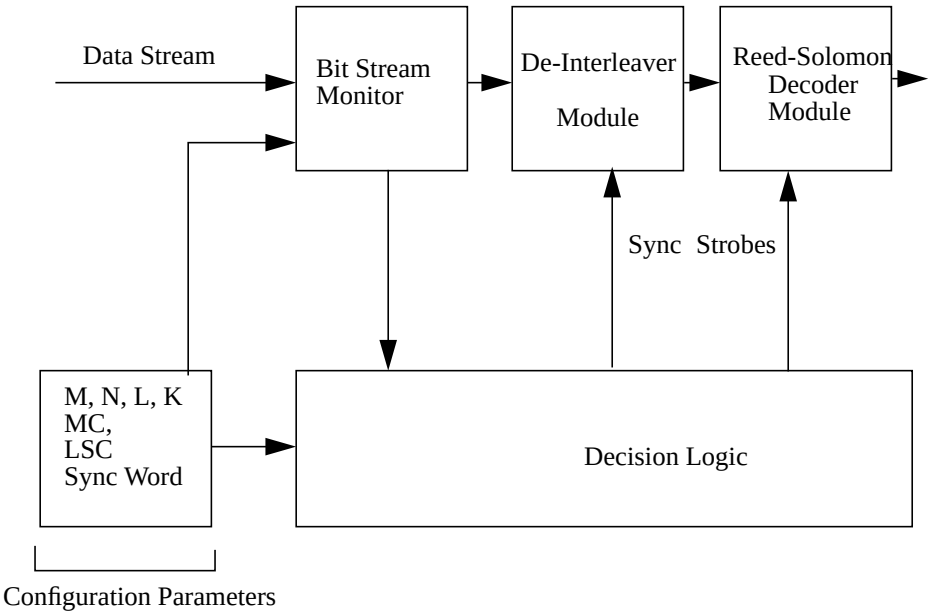


In case of a misaligned data stream the resulting bit error rate at the Viterbi decoder output compared to the original message is about 0.5. The mechanism implemented provides strong correlation between an out-of-sync condition and the observed bit error rate.

This first synchronization stage does not inspect the data stream for specific synchronization patterns nor does it remove any portions of the data stream.

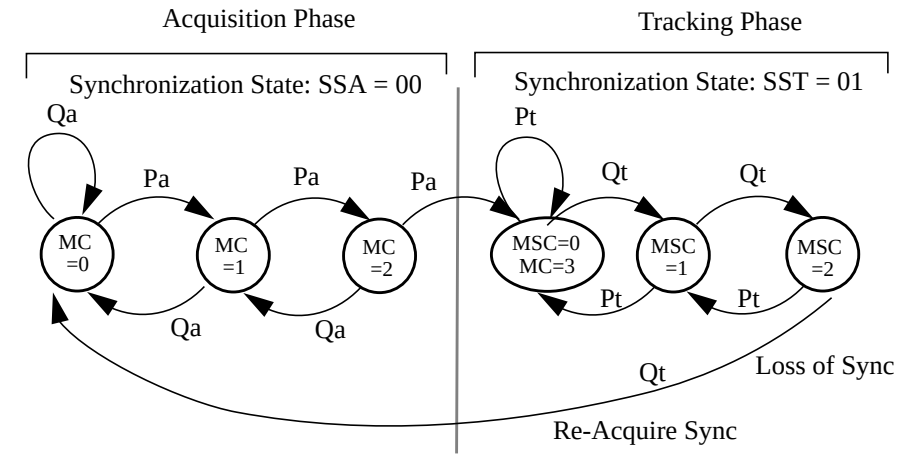
Once the Viterbi decoder module has reached synchronization the following blocks (De-Interleaver and Reed-Solomon decoder) require a synchronization procedure of their own.

Reed-Solomon,
Deinterleaver
Synchronization



The second synchronization stage relies on searching the data stream for a pre-defined sync word as the basis for the in-sync/out-of-sync decision.

The example state diagram below outlines the mechanism to determine synchronization, tracking and loss of synchronization.



Pa: State Transition, Sync word detected (N, M, K)
Qa: State Transition, Sync word misdetected

Pt: State Transition, Sync word detected (N, M, L)
Qt: State Transition, Sync word not detected

The parameters are defined as follows:

N: Length of the RS codeword in Bytes

M: Length of synchronization word in bits (M=8, fixed)

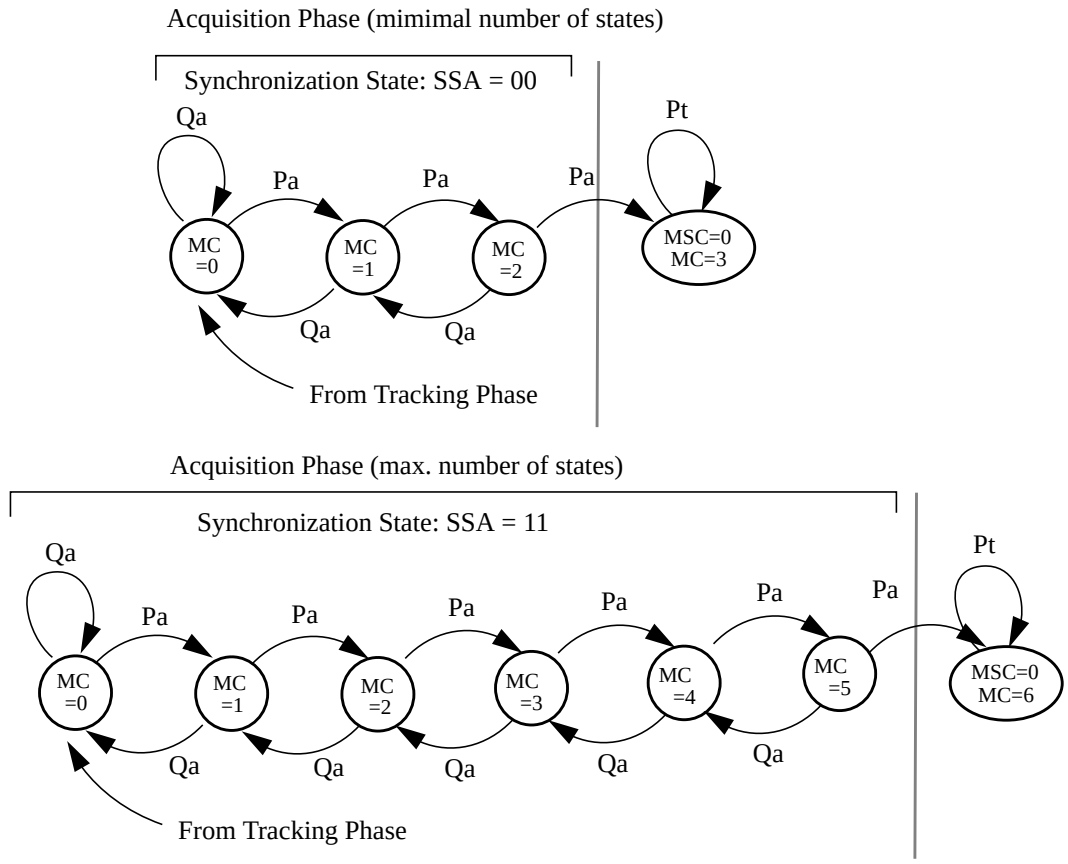
K: Max. Number of mismatching bits allowed to declare a match when comparing M bits in the data stream to the reference sync word during acquisition phase. (K=0, fixed)

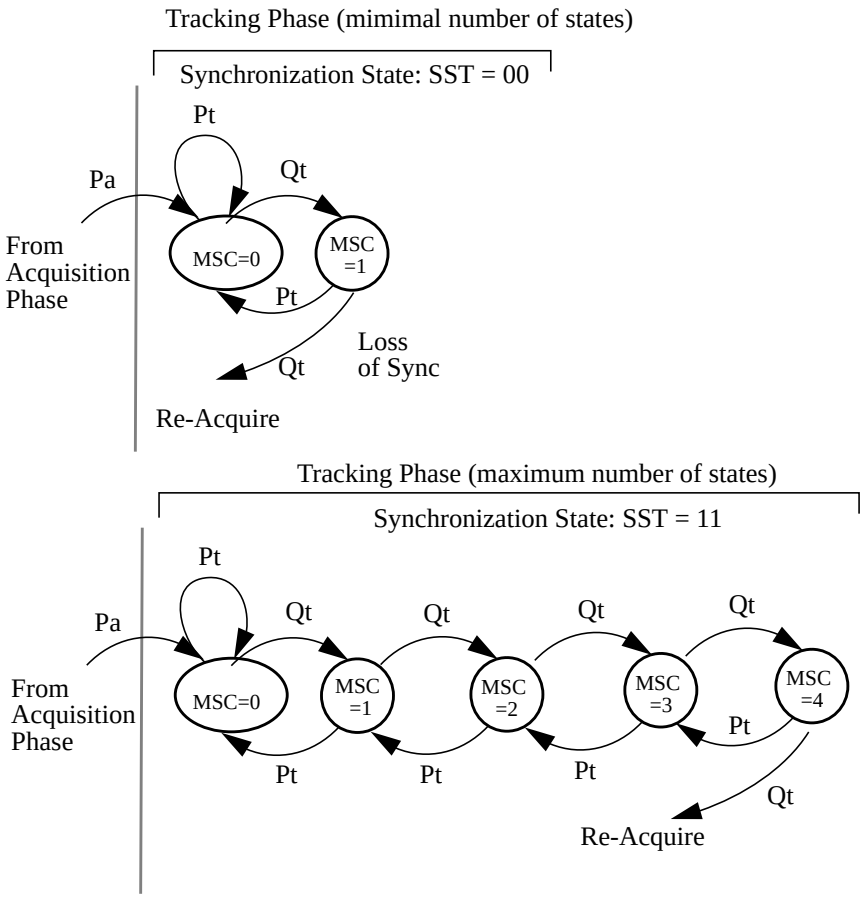
MC: Match counter, number of sync word matches found so far during acquisition phase.

L: Max. Number of mismatching bits allowed to declare a match when comparing M bits in the data stream to the reference sync word during tracking phase. (L= 0, 1 or 2)

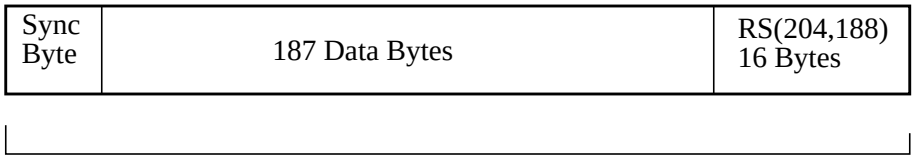
MSC: Mismatch counter, number of sync word mismatches found so far during tracking phase.

In addition, the state diagram for the acquisition and tracking phase is user configurable to some degree. The SSA and SST parameters (Synchronization State) allows for three to six and two to five detected and misdetected sync words before a acquisition or loss of synchronization respectively is declared. Shown below are the minimum and maximum nuber of states that the user can select for aquisition and tracking modes.





Of particular interest is the data format specified in the MPEG2 system layer document . It calls for a MPEG-2 RS(204,188) protected transport packet to consist of 204 bytes, including 1 sync byte, 187 data bytes and 16 redundancy bytes.

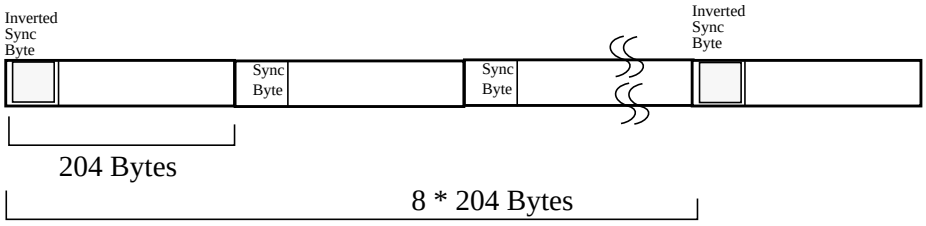


The table below shows the computed values for mean acquisition time (T ac), mean time to loss of lock (T ll) and probability of false lock (P fl) for the synchronization stage 2 as a function of the incoming bit error rate (code word length = 204 bytes, sync word length = 8 bits, K=0, L=2, 60 Mbits/sec):

Bit Error Rate	***T ac***		***T ll***		***P fl***
	# frames	sec	# frames	sec	
5.0e-04	3.88	1.05e-04	9.00e+15	2.44e+11	5.98e-08
1.0e-03	**3.91**	**1.06e-04**	**9.00e+15**	**2.44e+11**	**5.98e-08**
2.0e-03	3.98	1.07e-04	9.00e+15	2.44e+11	5.98e-08
5.0e-03	4.16	1.12e-04	4.50e+15	1.22e+11	5.98e-08
1.0e-02	4.48	1.21e-04	6.37e+12	1.72e+08	5.98e-08
2.0e-02	5.15	1.39e-04	1.39e+10	3.78e+05	5.98e-08
5.0e-02	7.23	1.98e-04	5.21e+06	1.41e+02	5.98e-08

For an expected BER of 1.0e-03 about 4 frame times will be required to establish synchronization and loss of sync will occur after 9.0e+15 frames.

With one modification this basic format has been adopted by the V4/MOD-B task force for a multiprogram TV via satellite standard. One out of every eight synchronization words in the data stream is mod 2 complemented. The resulting structure looks as follows:



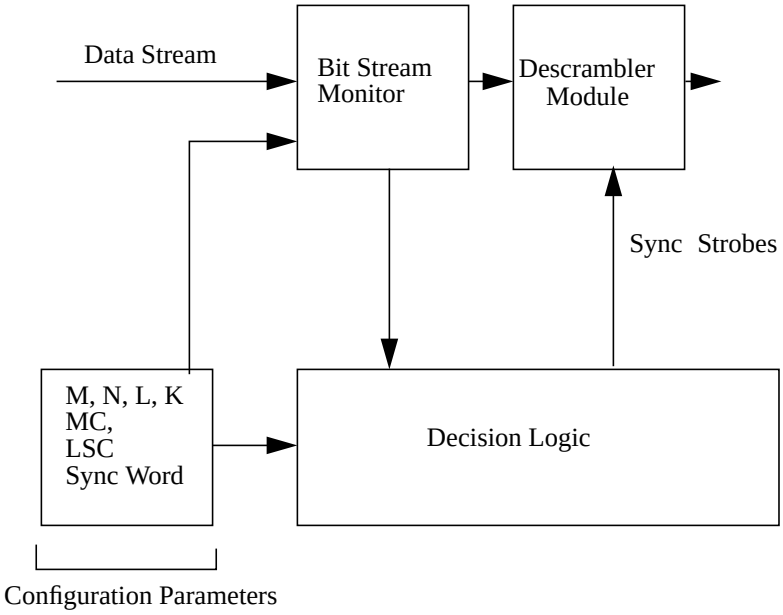
Given a bit stream consisting of a sequence of these packets the second sync stage searches for the predefined sync byte and, upon having met the sync acquisition criteria, issues the control strobes for the down stream modules.

In addition to providing the proper data alignment for the following Deinterleaver and Reed-Solomon decoder modules the second synchronization stage is able to resolve the 180 degrees phase uncertainty that may have been introduced by the demodulator and that the first (Viterbi) synchronization stage is not able to detect. This is achieved during the acquisition phase by simultaneously monitoring not only the synchronization word itself, but also its complemented version.

The sync byte does not need to be removed from the data stream since it is part of the MPEG system layer syntax and therefore needs to be left undisturbed by the channel decoding operation.

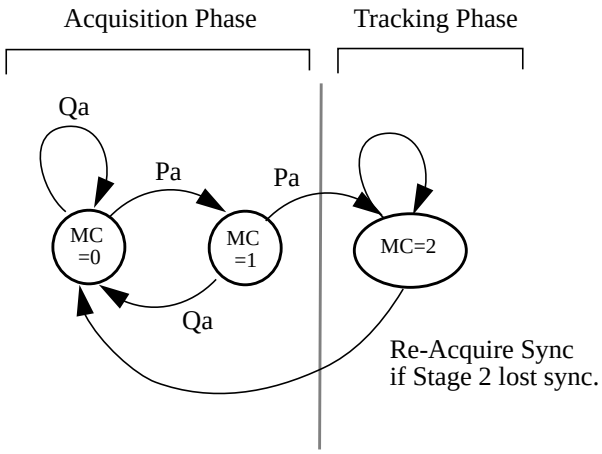
Descrambler Synchronization

The Descrambler is restarted every 8*N byte times. This restart is aligned with the complemented synchronization word that is present in the data stream once every eight Reed-Solomon code words (once every 8*N bytes).



For this third stage synchronization a very similar approach compared to stage two is taken for the acquisition phase to acquire proper data alignment. In difference to stage two the tracking phase for stage three is simplified since the detection of an out-of-sync condition in stage two will automatically force stage three to reacquire.

The flow chart below outlines the mechanism to determine synchronization, tracking and loss of synchronization for the third stage.



Pa: State Transition, Inverted Sync word detected (8*N, M, K)
Qa: State Transition, Inverted Sync word misdetected

Chapter 6
Viterbi Decoder Module

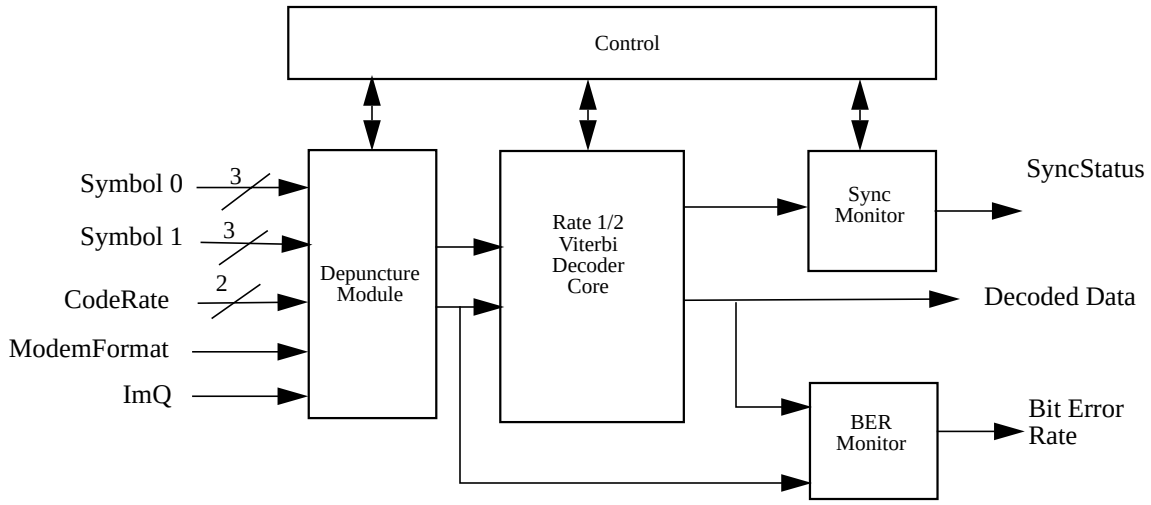
This chapter discusses the Viterbi Decoder module of the L64705.

This chapter contains the following sections:

- Section 6.1, Viterbi Decoder Architecture and Performance
- Section 6.2, Punctured Codes
- Section 6.3, Viterbi Bit Error Rate Monitor

6.1 Viterbi Decoder Architecture

Block Diagram of Viterbi Decoder Core



The design breaks down into the following major modules: a module to accommodate the depuncturing operation for code rates other than 1/2, a

rate 1/2 Viterbi decoder core that computes the serial output data stream given two sets of soft decision data input streams, a synchronization monitoring block to provide information on acquisition or loss of synchronization, a bit error rate monitoring block and a control module.

Features

- Basic rate 1/2 Viterbi Decoding Core
- Depuncturing for Code Rates 1/2, 2/3, 3/4, 5/6,7/8 supported
- 8-level soft decision data input
- Input in binary offset or sign magnitude format
- 96-State trace back memory for all code rates
- Constraint length 7
- Synchronization monitor
- Decoded Bit Error Rate monitor
- Maximal Likelihood (ML) decoding algorithm
- 5.2 dB coding gain for rate 1/2 (no erased input) code at BER of 10^{-5}
- Generating Polynomial 171 (Octal) and 133 (Octal)

Code Performance

The code performance for the Viterbi decoder was established on the basis of simulating a numerically accurate model of the architecture.

The following table reflects the results for a constraint length of 7 and code rates of 1/2, 3/4 and 7/8. The number of samples used to establish individual data points is shown as a measure of accuracy for the error rates stated below.

Code Rate	***K***	***Trace back***	***Soft Dec Bits***	***Eb/No***	***Sample Size***	***Bit Error Rate***	***Byte Error Rate***
1/2	7	96	3	3.0	134e6	7.7e-4	2.2e-3
1/2	7	96	3	3.5	134e6	1.7e-4	5.4e-4
1/2	7	96	3	4.0	134e6	3.5e-5	1.2e-4
1/2	7	96	3	4.5	134e6	6.6e-6	2.2e-5
1/2	7	96	3	5.0	134e6	9.5e-7	3.5e-6

Code Rate	*K*	*Trace back*	*Soft Dec Bits*	*Eb/No*	*Sample Size*	*Bit Error Rate*	*Byte Error Rate*
1/2	7	96	3	5.5	134e6	1.9e-7	8.3e-7
1/2	7	96	3	6.0	134e6	(N/A)	(N/A)
2/3	7	96	3	3.0	10e6	2.83e-3	6.88e-3
2/3	7	96	3	3.5	10e6	7.86e-4	1.94e-3
2/3	7	96	3	4.0	10e6	1.6e-4	4.05e-4
2/3	7	96	3	4.5	10e6	2.98e-5	6.35e-5
2/3	7	96	3	5.0	10e6	7.04e-6	1.90e-5
2/3	7	96	3	5.5	10e6	1.37e-6	3.97e-6
2/3	7	96	3	6.0	100e6	1.29e-7	3.97e-7
3/4	7	96	3	4.0	134e6	5.9e-4	1.5e-3
3/4	7	96	3	4.5	134e6	1.2e-4	3.1e-4
3/4	7	96	3	5.0	134e6	2.4e-5	6.6e-5
3/4	7	96	3	5.5	134e6	3.9e-6	1.1e-5
3/4	7	96	3	6.0	134e6	6.1e-7	2.2e-6
3/4	7	96	3	6.5	134e6	1.5e-7	5.4e-7
3/4	7	96	3	7.0	134e6	6.7e-8	1.8e-7
5/6	7	96	3	4.0	10e6	3.98e-3	9.72e-3
5/6	7	96	3	4.5	10e6	1.03e-3	2.67e-3
5/6	7	96	3	5.0	10e6	1.63e-4	4.44e-4
5/6	7	96	3	5.5	10e6	4.37e-5	1.11e-4
5/6	7	96	3	6.0	10e6	1.29e-5	3.17e-5
5/6	7	96	3	6.5	10e6	7.94e-7	2.38e-6
5/6	7	96	3	7.0	100e6	2.78e-7	1.03e-6
5/6	7	96	3	7.5	100e6	5.95e-8	3.17e-8
7/8	7	96	3	5.0	134e6	1.3e-3	3.2e-3
7/8	7	96	3	5.5	134e6	3.2e-4	8.7e-4
7/8	7	96	3	6.0	134e6	7.4e-5	2.2e-4
7/8	7	96	3	6.5	134e6	1.7e-5	5.3e-5
7/8	7	96	3	7.0	134e6	3.8e-6	1.4e-5
7/8	7	96	3	7.5	134e6	1.0e-6	3.8e-6
7/8	7	96	3	8.0	134e6	1.6e-7	6.6e-7

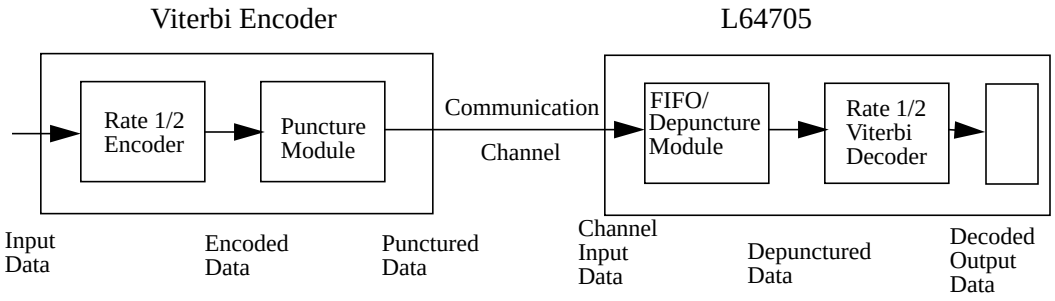
6.2 Punctured Codes

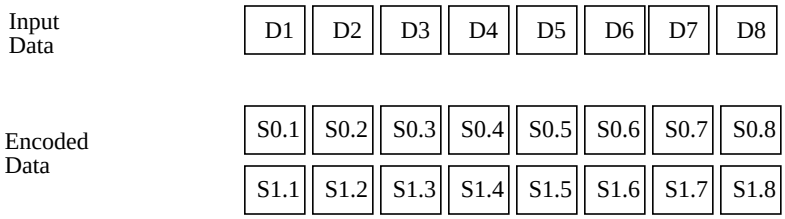
The L64705 supports not only the basic rate 1/2 decoding operations, but also code rates 2/3, 3/4, 5/6 and 7/8. The proper sequence of symbols on the S0 and S1 inputs is dictated by the code rate and underlying depuncture scheme chosen.

The puncture patterns supported are outlined below:

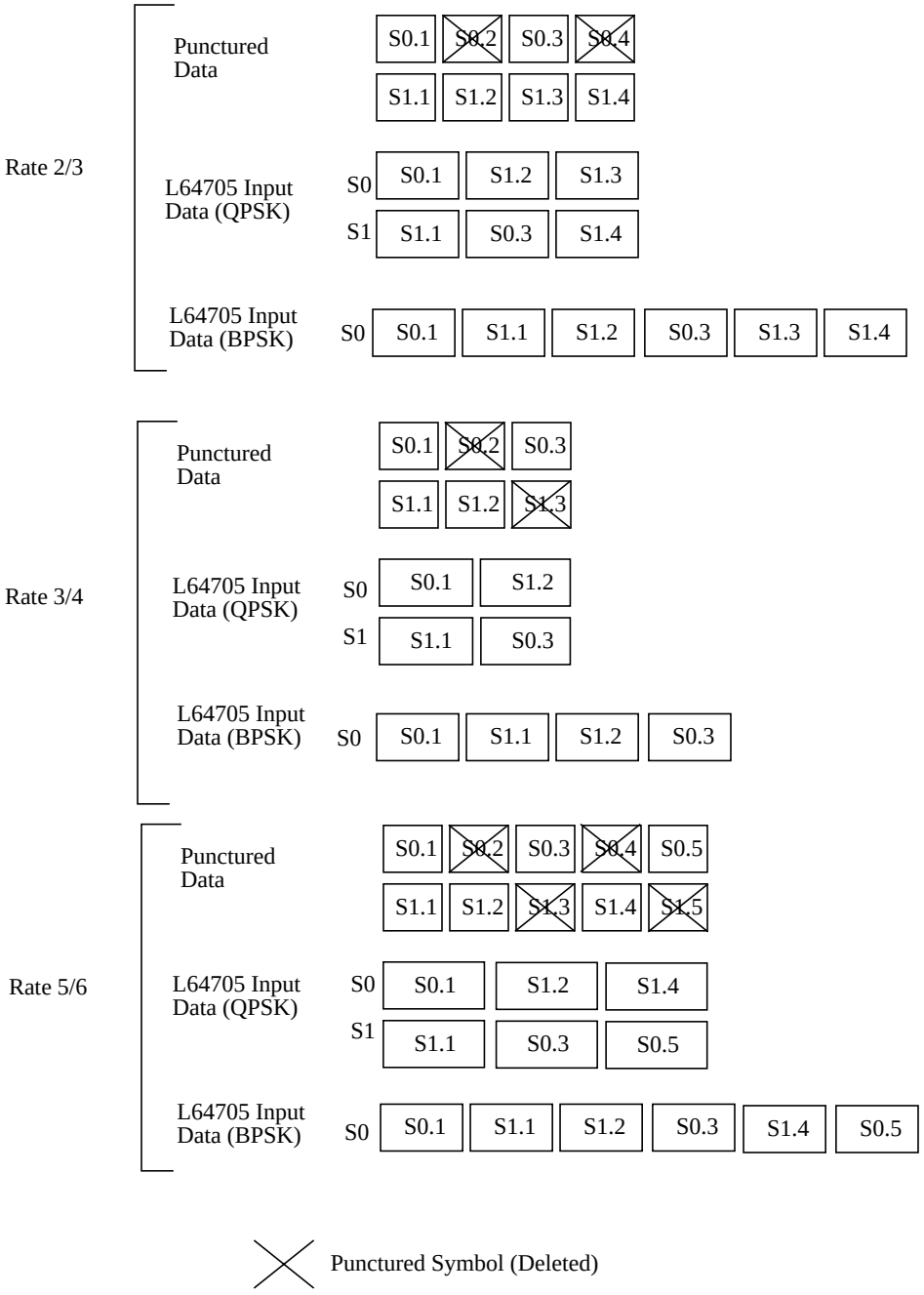
Code Rate	Puncture Pattern
1/2	S0: 1 S1: 1
2/3	S0: 1 0 S1: 1 1
3/4	S0: 1 0 1 S1: 1 1 0
5/6	S0: 1 0 1 0 1 S1: 1 1 0 1 0
7/8	S0: 1 0 0 0 1 0 1 S1: 1 1 1 1 0 1 0

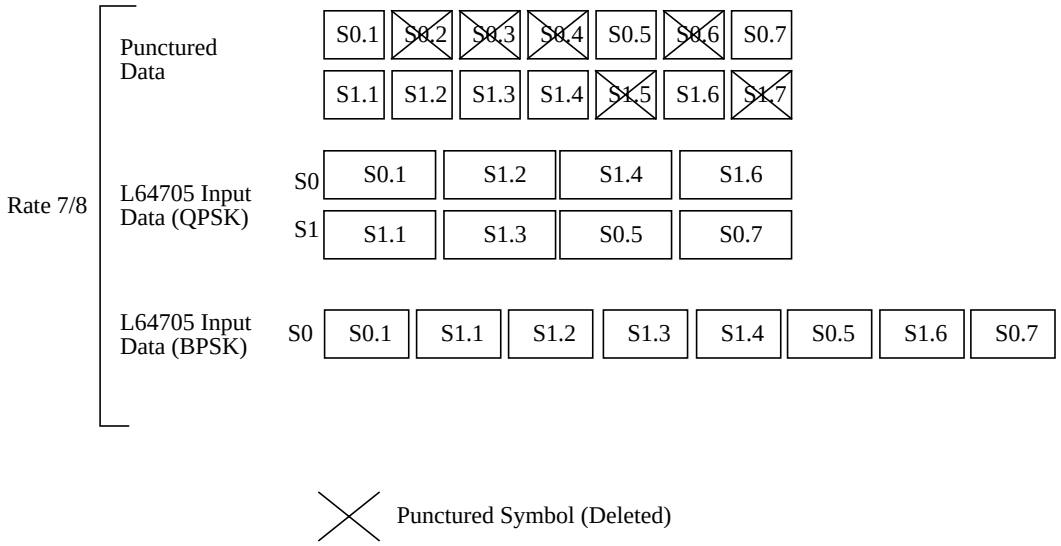
.The encoded data is punctured according to the pattern above:





The L64705 receives the symbols on the S0, S1 buses for QPSK format and on the S0 bus only for BPSK format in the order shown under L64705, Input Data. The depuncturing module handles the reordering and the insertion of erasures into the received symbol stream before decoding is performed in the rate 1/2 Viterbi decoder module.


Rate 2/3
Punctured Data
S0.1 S0.2 S0.3 S0.4
S1.1 S1.2 S1.3 S1.4
L64705 Input Data (QPSK)
S0 S0.1 S1.2 S1.3
S1 S1.1 S0.3 S1.4
L64705 Input Data (BPSK)
S0 S0.1 S1.1 S1.2 S0.3 S1.3 S1.4
Rate 3/4
Punctured Data
S0.1 S0.2 S0.3
S1.1 S1.2 S1.3
L64705 Input Data (QPSK)
S0 S0.1 S1.2
S1 S1.1 S0.3
L64705 Input Data (BPSK)
S0 S0.1 S1.1 S1.2 S0.3
Rate 5/6
Punctured Data
S0.1 S0.2 S0.3 S0.4 S0.5
S1.1 S1.2 S1.3 S1.4 S1.5
L64705 Input Data (QPSK)
S0 S0.1 S1.2 S1.4
S1 S1.1 S0.3 S0.5
L64705 Input Data (BPSK)
S0 S0.1 S1.1 S1.2 S0.3 S1.4 S0.5
Punctured Symbol (Deleted)



6.3 Viterbi Bit Error Rate Monitor

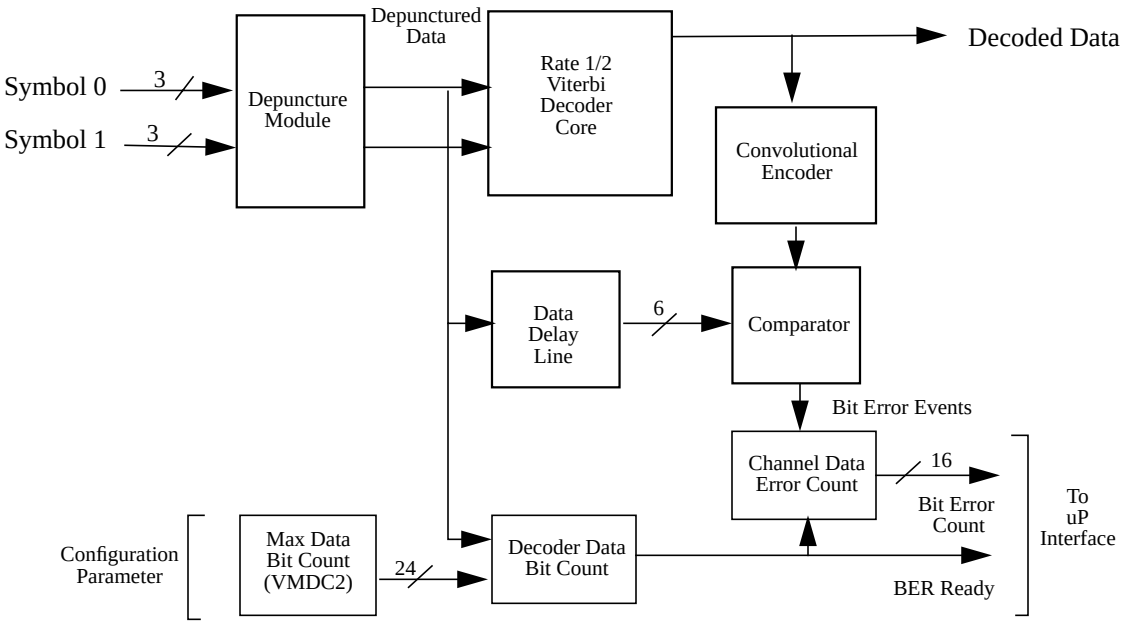
A performance monitor for the channel bit error rate is built into the L64705. Occurrences of bit errors are found by comparing an appropriately delayed version of the incoming channel data stream to the re-encoded Viterbi decoder output data stream.

Depunctured data is delayed by the Viterbi decoder core latency. The decoded bit stream produced by the rate 1/2 Viterbi decoder core is being convolutionaly re-encoded resulting in a symbol stream that can be compared on a symbol-by-symbol basis against the incoming depunctured channel stream. Any discrepancy between two respective symbols indicates a corrected error (or with a much smaller probability a erroneous output bit produced by a failure of the Viterbi decoder to decode correctly). For code rates other than 1/2, decoder input symbol that are marked as erasures are disregarded when the error events are detected.

The bit error events are further processed internally to produce a measure for the actual channel bit error rate. VMDC2 specifies the number of channel bits (and hence the time period) over which the number of occurring

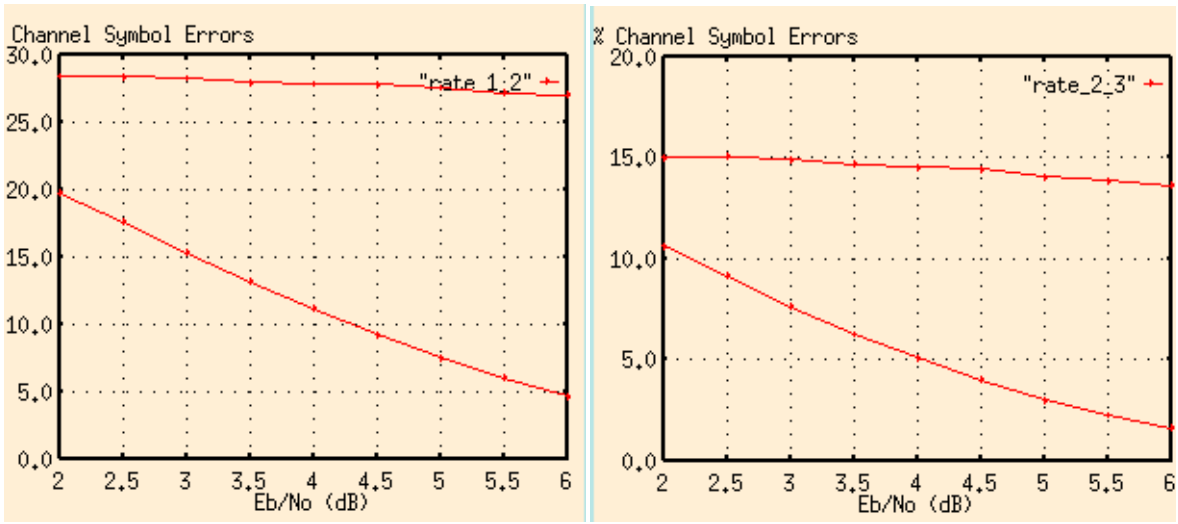
channel bit errors is to be counted. The actual number of bit is obtained as follows: Number of bits = VMDC2 * 4. The channel data error counter accumulates the errors internally and updates the Bit Error Count once at the end of the period specified by VMDC2 and indicated by the BER Ready flag. The Viterbi Bit Error Count (VBERC) is one of the values available to the user via the micro processor interface. (Number of errors = VBERC * 4). In addition, the BER Ready line causes the VBER flag in the STS (System Status Register) to be set. The interrupt pin is set if the corresponding interrupt enable bit (VBER_EN) is active in the SMR (System Mode Register).

Block Diagram of Viterbi Bit Error Detection Circuit.

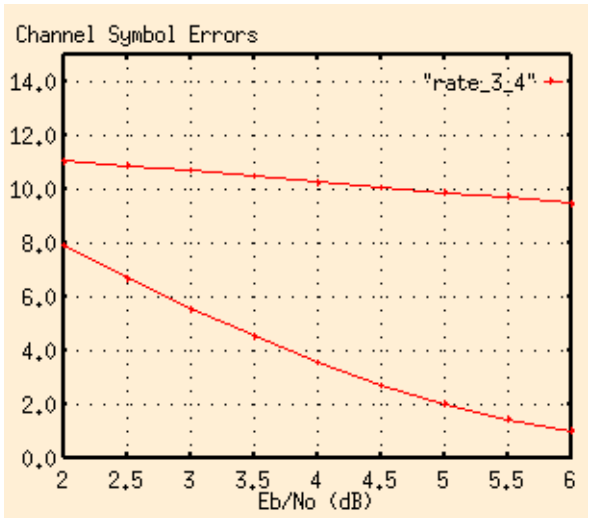


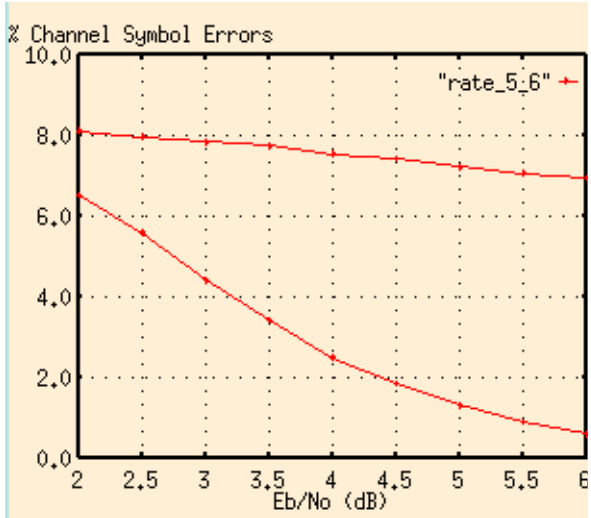
To assist the proper selection of the ratio of the threshold values VMDC2 and VBERC the percentages of error symbols are plotted for all the code rates supported by the L64705.

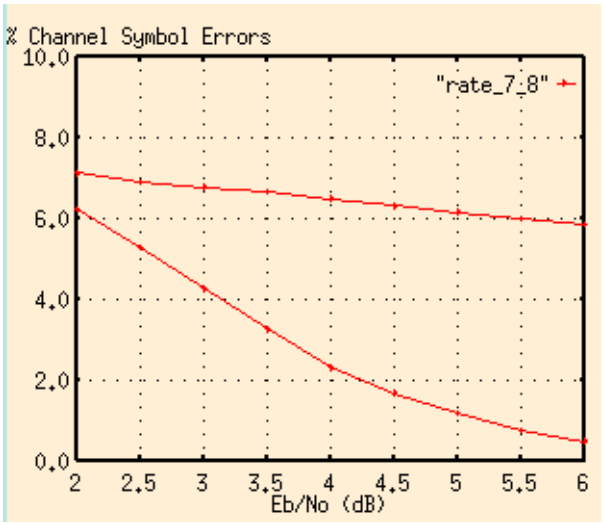
The upper curve in every graph represents the out-of-synchronization condition, the lower one the in-synchronization condition.


Channel Symbol Errors
"rate_1_2"
30.0
25.0
20.0
15.0
10.0
5.0
0.0
2
2.5
3
3.5
4
4.5
5
5.5
6
Eb/No (dB)

% Channel Symbol Errors
"rate_2_3"
20.0
15.0
10.0
5.0
0.0
2
2.5
3
3.5
4
4.5
5
5.5
6
Eb/No (dB)


Channel Symbol Errors
"rate_3_4"
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
2
2.5
3
3.5
4
4.5
5
5.5
6
Eb/No (dB)


% Channel Symbol Errors
"rate_5_6"
10.0
8.0
6.0
4.0
2.0
0.0
2
2.5
3
3.5
4
4.5
5
5.5
6
Eb/No (dB)



The value for the ratio VBERC/VMDC2 needs to be chosen in between the in-sync and the out-of-sync curves. For example, in the case of rate 1/2, a value of VBERC/VMDC2 = 0.24 (or 24%) establishes a valid decision threshold over the entire Eb/No range shown.

Chapter 7
Deinterleaver Module

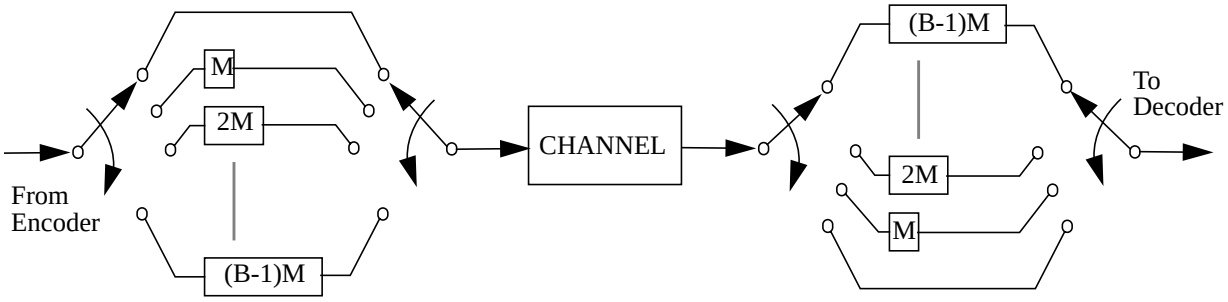
This chapter describes the Deinterleaver module contained in the L64705.

This chapter contains the following sections:

- Section 7.1, Deinterleaver Functionality
- Section 7.2, Deinterleaver Module Architecture
- Section 7.3, Functional Waveforms

7.1 Deinterleaver Functionality

Block Diagram of Deinterleaver Core



The interleaving/deinterleaving operation is outlined in the diagram above. The Interleaver is a device that rearranges the ordering of a sequence of symbols in a deterministic manner. A (B, N) Periodic Interleaver has the following characteristics:

- The minimum separation at the interleaver output is B symbols for any two symbols that are separated by less than N symbols at the interleaver input.

- Any burst of b < B errors inserted by the channel results in single errors at the de-interleaver output.

The scheme is also referred to as a convolutional interleaver/deinterleaver (based on the approach by Forney).

This L64705 module performs periodic de-interleaving. B the desired interleaving depth, and M defined as

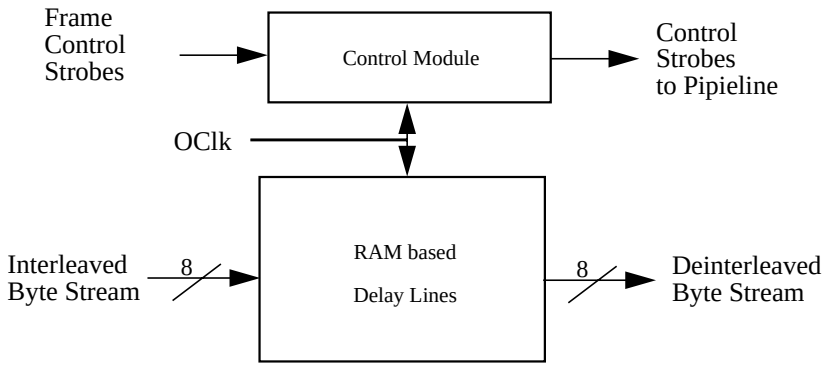
$$M = \left\lceil \frac{N}{B} \right\rceil$$

Features

- Convolutional Deinterleaving
- Block Length of 204 bytes
- Deinterleaving Depth of 12
- System clock rate up to 60 Mhz

7.2 Deinterleaver Block Diagram

Block Diagram of Deinterleaver Core



The main modules are a set of configurable RAM-based delay lines to implement the proper delay for individual data bytes and a controller to handle and generate the strobes needed by the following elements in the data path.

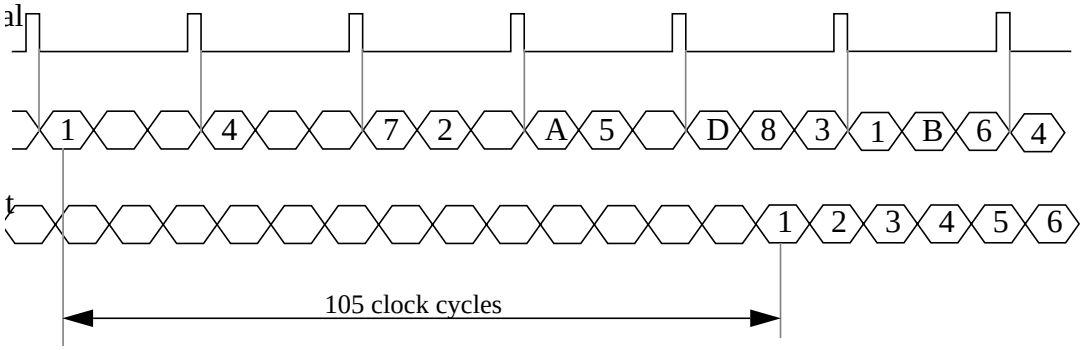
7.3 Functional Waveforms

The De-interleaver receives the rearranged byte stream and reconstructs the original one by inverting the Interleaver's function. The block boundaries must be recovered and are indicated by internal strobes.

The de-interleaver will output the original byte stream after a delay of:

$$\boldsymbol{Delay} = \{ (\boldsymbol{B} - \mathbf{1}) \times \boldsymbol{B} \times \lceil \boldsymbol{N} / \boldsymbol{B} \rceil + 1 \} \times 8 + 1$$

In the current example the total delay is **{2 x 3 x 2 + 1} x 8 + 1 = 105** clock cycles. Notice that the delay from the time the first input byte to the first valid output byte is indeed 105 clock cycles.



Chapter 8
Reed-Solomon Decoder Module

This chapter discusses the Reed-Solomon Decoder module contained in the L64705.

This chapter contains the following sections:

- Section 8.1, Reed-Solomon Overview
- Section 8.2, Performance Analysis
- Section 8.3, Reed-Solomon Decoder Architecture

8.1 Reed-Solomon Overview

ECC devices have a specific lexicon associated with their ability to correct transmission messages. This section defines the terms used for variables in the Reed-Solomon Core. The terms are used throughout this document.

R **Check Bytes**
The encoder generates and appends check bytes to the incoming message according to the Reed-Solomon error correction encoding. The decoder uses check bytes to locate and correct errors due to transmission. The customer specifies the size of the check byte field within the limitations.

d **Detection power**
Detection power has a minimum value of $\left\lfloor \frac{R}{2} \right\rfloor$ and a maximum value of R.

K **Message Length**
The message is comprised of multiple bytes. The size of the message varies depending on the code word length and the check bytes used, where K = N – R.

m **Symbol Size**
A data transfer is comprised of multiple symbols and the symbol size m is eight bits.

N **Codeword Length**
This variable is the sum of the number of message bytes and the number of check bytes (K + R). The value of N is 204:

T **Number of Error Corrections**
This variable is the maximum number of error corrections performed by the decoder. The value is 8:

.

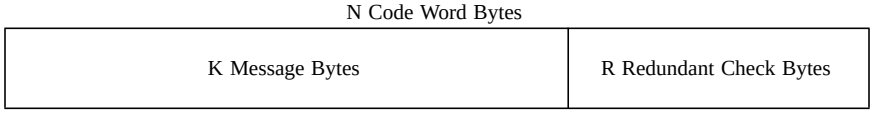
Digital communications and mass storage applications that require highly accurate data must avoid corrupting data when it is transmitted. Transmission channels can be designed with expensive, low-noise components to guard data integrity, but a more cost-effective technique is to implement forward error correction encoding into the message data before transmission.

Forward Error Correction

Forward error correction requires an encoder that appends redundant check bytes to a message before transmission. The bytes, with an indeterminate number of bits, are referred to as symbols. The message symbols followed by redundant check symbols are called code words. The check symbols are redundant in the sense that they are derived from the message and are appended to the message. Check symbols are also referred to as "redundant check bytes," and sometimes as "correction bytes."

Figure 8.1 illustrates a code word. Explanatory text follows the figure.

Figure 8.1 Code Word Structure

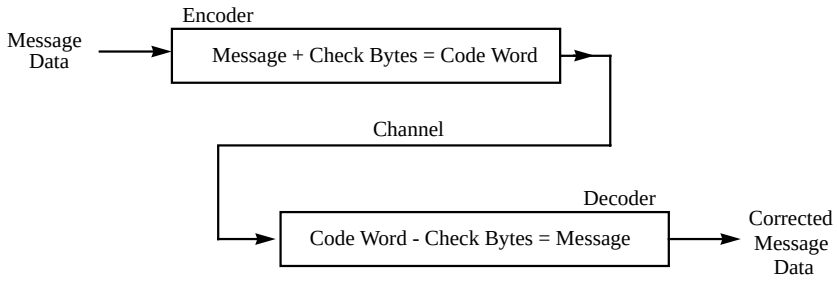


A code word is a block of N bytes that includes K message symbols and N – K check bytes (R). The check bytes or symbols are some fraction of the message symbols. A large number of check symbols allows the decoder to correct a large number of transmission errors.

The redundant check symbols in a message allow a decoder at the receiving end of a transmission line to detect transmission errors and reconstruct

the original message content. Figure 8.2 shows a block diagram of the basic encoder and decoder functions in a transmission system.

Figure 8.2 Forward Error Correction Data Path



After generating a code word, the encoder transmits it through a low cost channel to a decoder. The decoder compares the bit stream in the message data to the encoding in the check bytes to detect transmission errors. The original message can be precisely reconstructed from the check symbols, as long as the number of errors in the code word is within the range

$$errors \leq \left(\frac{R}{2} \right) \cdot$$

Reed-Solomon Correction Codes

Reed-Solomon (RS) error correction codes are systematic and operate on bytes rather than single-bit data streams. The importance of RS codes is illustrated by their adoption as international and domestic standards in various areas of applications. The codes are expressed by convention as two numbers, the first indicating the total codeword length (N), and the second indicating the number of message bytes (K). The difference between these two numbers (N-K) is the number of check bytes. A (255, 223) RS code, for instance, with eight-bit bytes, was adopted as part of the standard for space missions by both the European Space Agency and NASA. The compact disc digital-audio system uses a combination of a (32, 28) RS code and a (28, 24) RS code. The MIL-STD-2179/ANSI X3B.6 media exchange standard uses a
(161, 153) RS code and a (128, 118) RS code for high-density magnetic recording.

LSI Logic uses this generator polynomial for RS codes: $\prod_{i=0}^{R-1}\left(x+\alpha^{i}\right)$

where α is a root of the binary primitive polynomial:

$$\alpha^8 + x^4 + x^3 + x^2 + 1$$

A data byte (d_7, d_6,....d_1, d_0) is identified with the element $d_7\alpha^7 + d_6\alpha^6 +....+ d_1\alpha + d_0$ in GF(256), the finite field with 256 elements.

The error correcting power of an RS code is related to the number of redundant check symbols in its code words. In general, an RS code with 2t check symbols per code word can correct up to “t” byte errors per code word. Higher redundancy allows more errors to be corrected

The remainder of this section describes the process of correcting transmission errors with Reed-Solomon codes.

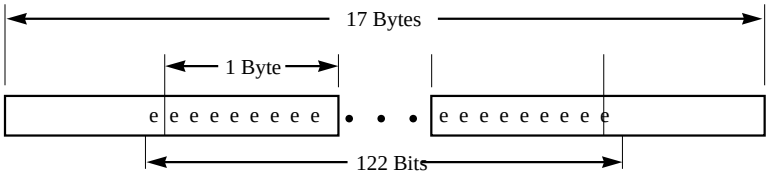
Error Handling and Correction

A bit error occurs when a transmitted zero is received as a one or vice versa. A byte error occurs when one or more bits in the byte have errors. For example, a byte with only one bit error is counted as one byte error, and a byte with m bit errors (all bits are inverted) is also counted as one byte error. As long as a code word has no more than $t = \lfloor (R)/2 \rfloor$ byte errors, the RS decoder corrects all errors. When a code word has more than

t = $\lfloor (R) / 2 \rfloor$ byte errors, the RS decoder detects the presence of excessive errors and asserts the ERROROUT signal LOW to notify the user.

Assume that the byte size is eight, the redundant check parameter is 32, and a 122-bit burst error is input to the decoder. The decoder can correct up to
t = 16 byte errors. A 122-bit burst can be divided into 17 bytes as shown in Figure 8.3, where each *e* represents a one bit error. Because the redundancy is 32, the decoder corrects up to 16 byte errors. Because the 122-bit burst corrupts 17 consecutive bytes, the maximum guaranteed correctable burst length in this example is 121 bits.

Figure 8.3
122-bit Burst Example



Features

- 60 Mbits/s throughput
- Flag for corrected errors
- Complies with CCITT recommended CCIR723 standard for digital TV transmission
- Decoder channel output counts for uncorrected data and error vector data.
- UNCORR pin flags uncorrectable errors.
- (204/188) Reed-Solomon Code Format

8.2 Performance Analysis

The performance of the code against independent random byte errors can be computed by the equation:

$$q = \sum_{i=t+1}^{N} \frac{i}{N}\binom{N}{i} p^i (1-p)^{N-i}$$

where:

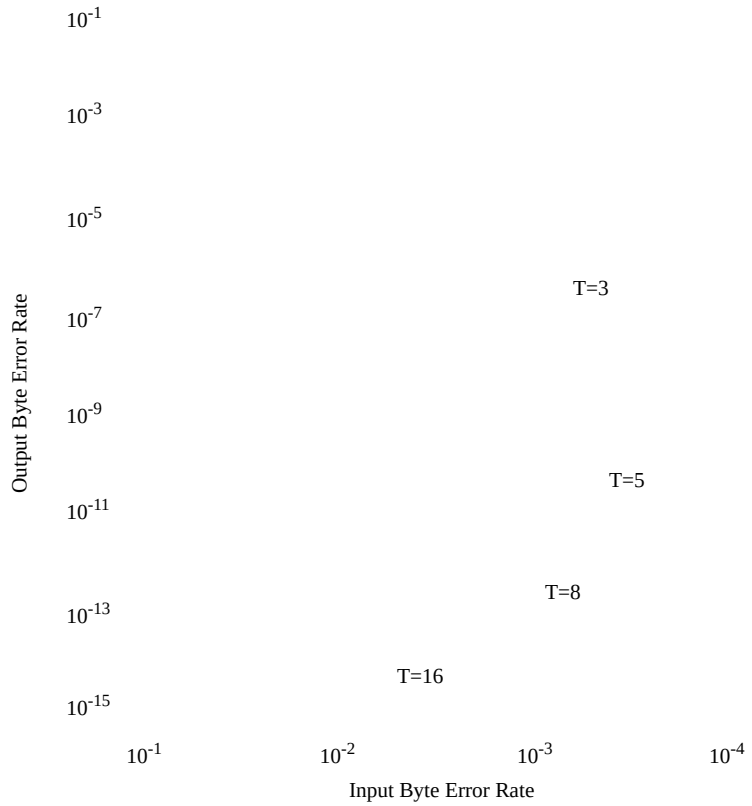
N	Code word length in bytes
p	Input byte error rate
q	Output byte error rate
$\binom{N}{i}$	Binomial coefficient that represents the number of ways of choosing i items from a collection of N distinct items

When there are more than t byte errors in a code word, the RS decoders usually detect the presence of excessive errors and notify the user by rasing the uncorrectable error flag. However, there is a small probability that the erroneous decoded code word remains undetected. The undetected erroneous code word rate is:

$$\frac{1}{t!}\left(\frac{N}{2^m - 1}\right)^t \sum_{i=t+1}^{N} \binom{N}{i} p^i (1-p)^{N-i}$$

For the code format (255, 223), the percentage redundancy of the RS code is 32/255 = 12.5%. With this modest amount of overhead, the coding system corrects error bursts of 16 bytes for t = 16. Figure 8.4 illustrates the random error correction capability with a codeword length of 255 when various correction values expressed as “T” are programmed into the device.

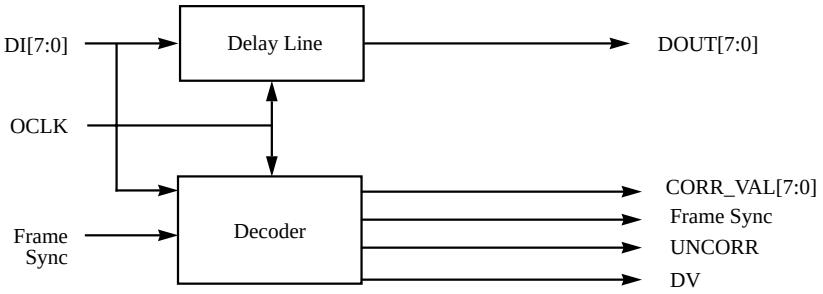
Figure 8.4
(255, 255-2T) Code Performance



8.3 Reed-Solomon Decoder Module Architecture

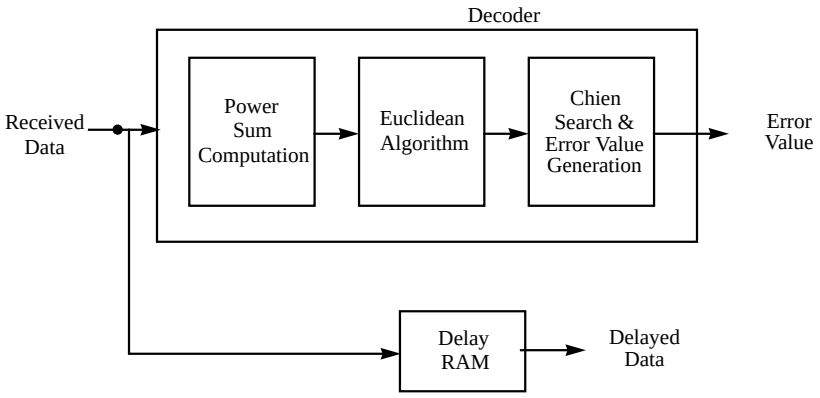
The basic components in the decoder are shown in Figure 8.5. Incoming data is retained in a delay line until error correction has been applied to data in the decoder block.

Figure 8.5
Block Diagram of
RS Decoder Core



To achieve a high throughput, three decoding stages are mapped into three separate, fully pipelined, hardware units that apply finite field computations to decoder input. Each unit is dedicated to the computation of one stage of the encoder algorithm, as shown in Figure 8.6. A brief description of each stage of the decoding process follows the figure.

Figure 8.6
Decoder Block
Diagram



Power Sum Computation

A finite field polynomial whose degree is one less than the code length is evaluated at various finite field elements. The number of such evaluations is equal to the number of check bytes in a code word. The result of the computation is summarized in a finite field polynomial called the power sum polynomial.

Euclidean Algorithm

This Euclidean block determines two polynomials, the error locator and the error evaluator polynomial. The decoder uses a version of the Euclidean algorithm (similar to the one for finding the greatest common divisor of two integers), which is applied to the power sum polynomial and another predefined polynomial.

Chien Search	The Chien Search functional block provides the roots of the error locator polynomial. This block also evaluates the error evaluator polynomial at the appropriate locations to obtain the actual values of the errors. The error value generation circuit outputs the bit errors from the incoming message.
Code Word Length	In the Reed-Solomon Core, the code word length is 204 bytes.

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Chapter 9
Descrambler Module

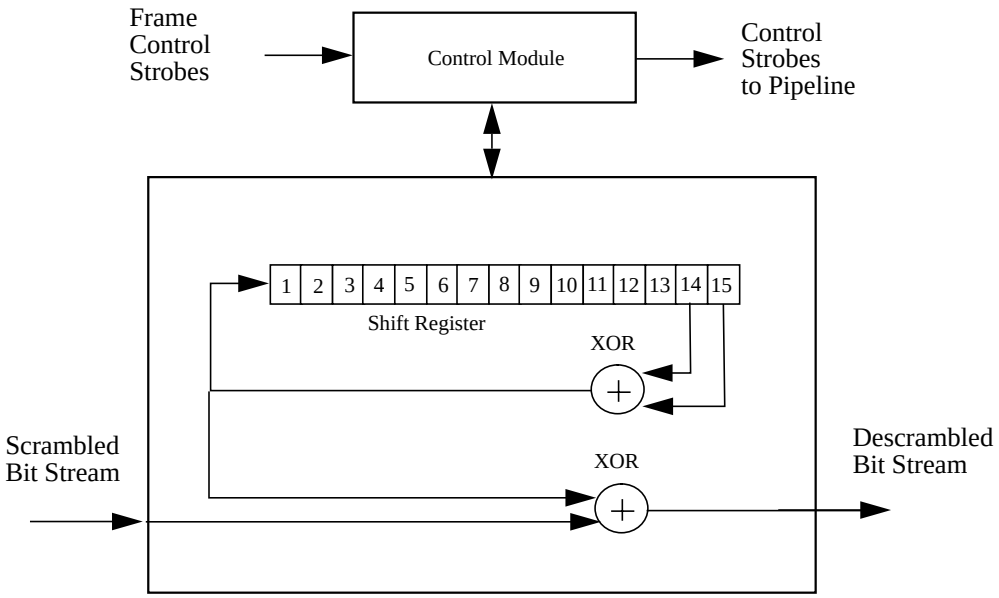
This chapter discusses the Descrambler module contained in the L64705.

This chapter contains the following sections:

- Section 9.1, Descrambler Architecture
- Section 9.2, Descrambler Operation

9.1 Descrambler Architecture

Block Diagram of Descrambler Module



The descrambler block breaks down into the following major modules: a module to perform the generation of a pseudo random binary sequence (PBRS) used to modify the incoming data stream and a control module to properly align data with the PRBS.

9.2 Descrambler Operation

Block Diagram of Descrambler Module

The pseudo random bit sequence produced in the descrambler module is characterized by the following generator polynomial:

$$1 + x^{14} + x^{15}$$

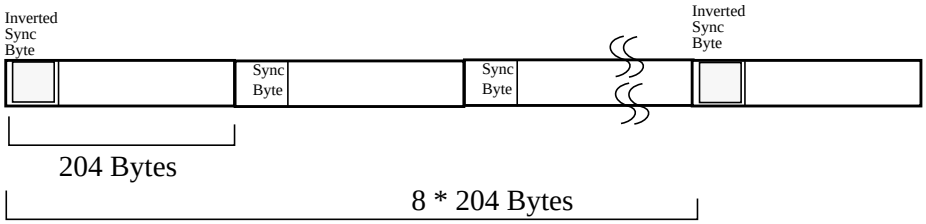
For initialization a specific value is chosen for the 15-tap shift register:

Shift Register Initialization Sequence

1	0	0	1	0	1	0	1	0	0	0	0	0	0	0
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

A sync word (B8 H) generated by inverting every eighth MPEG sync transport sync word (47 H) is used to align the descrambler with the incoming data stream. The first bit of the PRBS is applied to the first data bit following the inverted MPEG sync byte.

During the following seven non-inverted MPEG sync words the descrambler sequence generator is kept in operation, but the data stream is not modified. The descrambler is reset after every inverted MPEG sync word.


Inverted
Sync
Byte
Sync
Byte
Sync
Byte
Inverted
Sync
Byte
204 Bytes
8 * 204 Bytes

Chapter 10
L64705 Concatenated Decoder Specifications

Chapter 10 provides the specifications for the L64705 concatenated decoder device from LSI Logic. The DC characteristics and AC timing, a pin list, and pinout diagram are included in the specifications.

The decoders are implemented in LSI Logic LEA500K process.

This chapter contains the following sections:

- Electrical Requirements
- Power Sequence Requirements
- L64705 AC Timing
- L64705 Packaging

10.1 Electrical Requirements

This section specifies the electrical requirements for the L64705 decoder. Three tables list electrical data in the following categories:

- L64705 Absolute Maximum Ratings
- L64705 Recommended Operating Conditions
- L64705 DC Characteristics

Table 10.1 L64705 Absolute Maximum Rating (Referenced to VSS)

Parameter	Symbol	Limits[1]	Unit
DC Supply Voltage	V_{DD}	-0.3 to +3.9	V
LVTTL Input Voltage	V_{IN}	-1.0 to V_{DD}+0.3	V
5 V Compatible Input Voltage	V_{IN}	-1.0 to 6.5	V
DC Input Current	I_{IN}	10	mA
Storage Temperature Range (Plastic)	T_{STG}	-40 to +125	C

1. Note that the ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation.

Table 10.2 L64705 Recommended Operating Conditions

Parameter	Symbol	Limits[1]	Unit
DC Supply Voltage	V_{DD}	+3.0 to 3.6	V
Operating Ambient Temperature Range Commercial	T_A	0 to +70	C
Junction Temperature	T_J	£150	C

1. For normal device operation, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, may result in permanent device damage or impaired device reliability. Device functionality to stated DC and AC limits is not guaranteed if conditions exceed recommended operating conditions.

The following table lists the DC characteristics of the L64705 concatenated decoder. The device is produced with the LEA500K process, which is characterized by 0.5-micron drawn gate length cell based process. Characteristics in the table are the same for any device that has a buffer with the parameters listed in column two.

Symbol	Parameter	Condition[1]	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IL}	Input Low Voltage		V_{SS} - 0.5		0.8	V
V_{IH}	Input High Voltage	LVTTL Com/Ind/Mil Temp Range	2.0		V_{DD}+0.3	V
		5-volt Compatible	2.0		5.5	V
V_T	Switching Threshold			1.4	2.0	V
V_{T+}	Schmitt Trigger, Positive-going Threshold			1.7	2.0	V
V_{T-}	Schmitt Trigger, Negative-going Threshold		0.8	1.0		V
	Schmitt Trigger, Hysteresis		0.6	0.7		V
I_{IN}	Input Current Inputs with Pulldown Resistors Inputs with Pullup Resistors	$V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	-10 35 -35	±1 115 -115	10 222 -214	mA mA mA

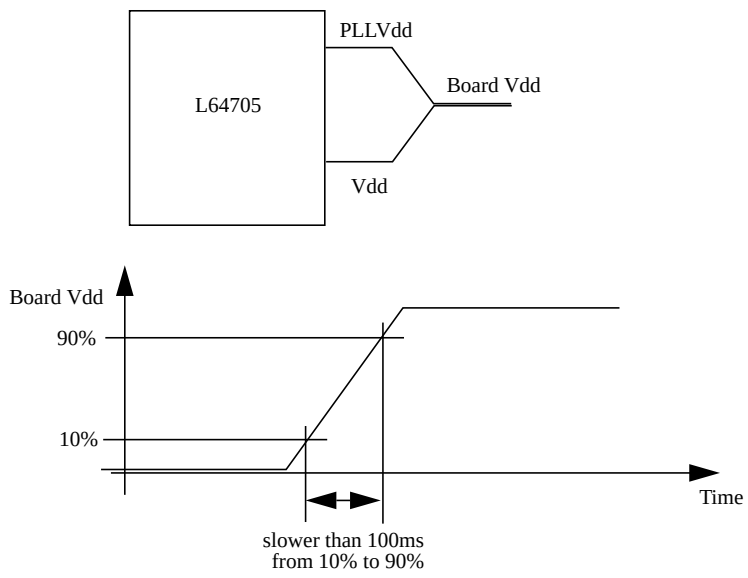
Symbol	Parameter	Condition[1]	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	Commercial and Military				
	Type B1	I_{OH} = -1 mA[3]	2.4		V_{DD}	V
	Type B2	I_{OH} = -2 mA[3]	2.4		V_{DD}	V
	Type B4	I_{OH} = -4 mA[3]	2.4		V_{DD}	V
	Type B6	I_{OH} = -6 mA[3]	2.4		V_{DD}	V
	Type B8	I_{OH} = -8 mA[3]	2.4		V_{DD}	V
	Type B12[2]	I_{OH} =-12 mA[3]	2.4		V_{DD}	V
V_{OL}	Output Low Voltage	Commercial and Military				
	Type B1	I_{OL} = 1 mA		0.2	0.4	V
	Type B2	I_{OL} = 2 mA		0.2	0.4	V
	Type B4	I_{OL} = 4 mA		0.2	0.4	V
	Type B6	I_{OL} = 6 mA		0.2	0.4	V
	Type B8	I_{OL} = 8 mA		0.2	0.4	V
	Type B12[2]	I_{OL} =12 mA		0.2	0.4	V
I_{OZ}	3-state Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	-10	±1	10	mA
I_{OS}	Output Short Circuit Current[4], BT4	$V_O = V_{DD}$			140	mA
		$V_O = V_{SS}$			-40	mA
	Output Short Circuit, BT4F	$V_O = V_{DD}$			67	mA
		$V_O = V_{SS}$			-86	mA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}				
I_{CC}	Dynamic Supply Current	f = 60MHz, V_{DD} = Max	270 (estimate)			mA
C_{IN}	Input Capacitance[5]	Input and Bidirectional Buffers	2.5			pF
		5-volt Compatible	3.0			pF
C_{OUT}	Output Capacitance[5]	Output Buffer[6]	2.0			pF
		5-volt Compatible	3.0			pF

1. Military junction temperature range: -55 to +150 ˚C, 10% power supply (ceramic packages only). Industrial junction temperature range: -40 to +125 ˚C, 5% power supply . Commercial junction temperature range: 0 to 115 ˚C, 5% power supply .
2. Requires two output pads.
3. See the “Interfacing to 5 V Signals Using 500K Technologies” application note for “F” series output buffer I_{OH} values.
4. Type B4 output. Output short circuit current for other outputs will scale.
5. Excluding package capacitance.
6. Output using single buffer structure (excluding package).

10.2 Power Sequence Requirements

To prevent latch up due to the power differences between the PLL block and the core logic, the following rule must be strictly followed: Board VDD on and off ramp time must be slower than 100 ms, as measured from 10% to 90% points (see figure below)

Figure 10.1 L64705 Synchronous AC Timing



10.3 AC Timing

This section presents AC timing information for the L64705 lists the AC timing parameters for the timing diagrams shown below.

Figure 10.2 L64705 Synchronous AC Timing

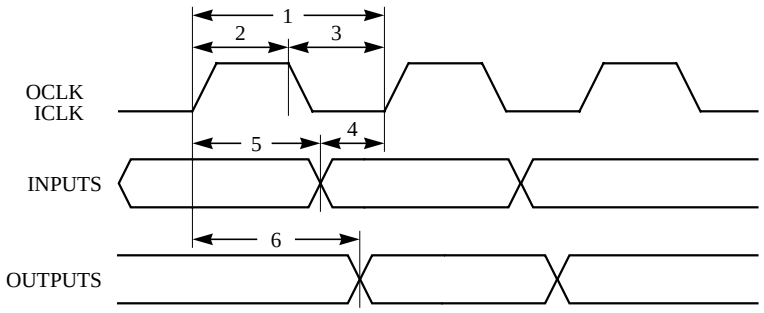


Figure 10.3 L64705 Decoder Read Cycle

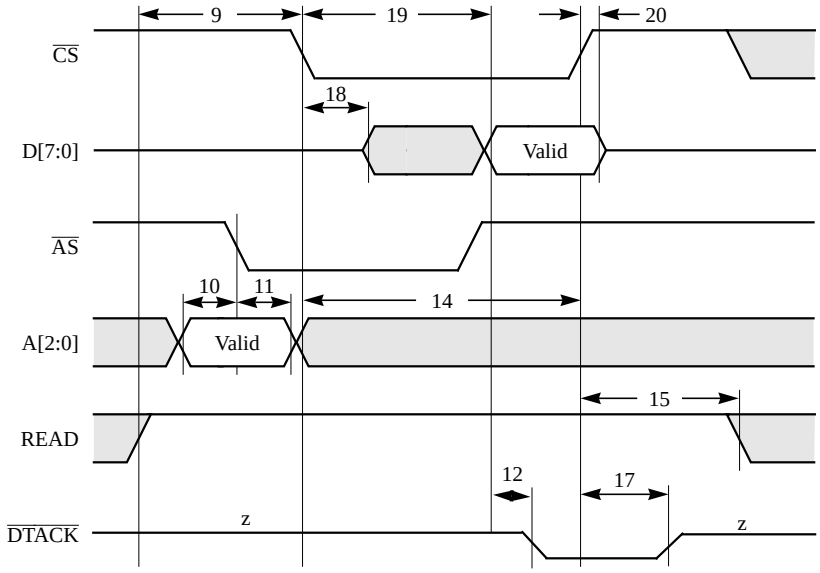


Figure 10.4
L64705 Decoder
Write Cycle

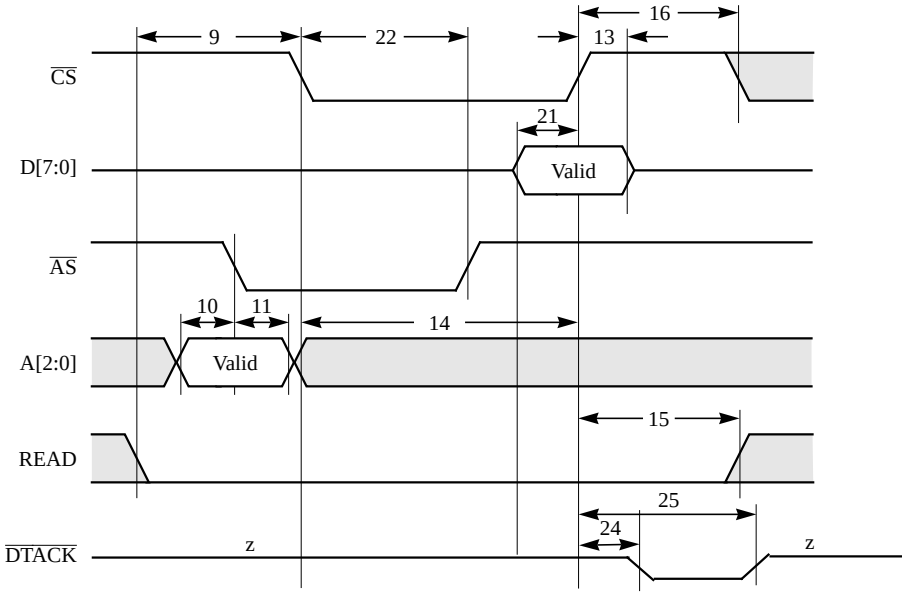


Figure 10.5
L64705 RESET
Timing Diagram

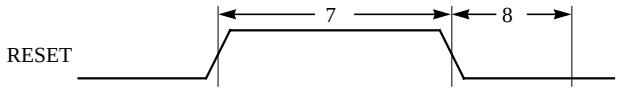
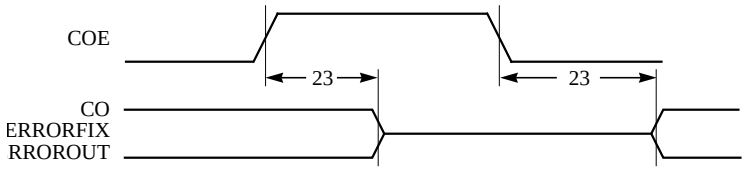


Figure 10.6
L64705 Bus
3-State Delay
Timing



AC Timing Values

The numbers in column 1 in Table 10.5 refer to the timing parameters shown in the preceding figures.

Table 10.3
L64705
Timing Parameters

Parameter		***Description***		***60 MHz***		***Unit***
				Min	***Max***	
1	t_{CYCLE}	Clock Cycle OCLK		16.0	–	ns
2	t_{PWH}	Clock Pulse Width High		7.0	–	ns
3	t_{PWL}	Clock Pulse Width Low		7.0	–	ns
4	t_{S}	Input Setup time to CLK		3.0	–	ns
5	t_{H}	Input Hold to CLK		1.0	–	ns
6	t_{OD}	Output Delay from CLK		3.0	12.0	ns
7	t_{RWH}	Reset Pulse Width High		3	–	OCLK Cycles
8	t_{WK}	Wake-Up Time		280	–	OCLK Cycles
9	t_{SURCS}	READ Setup Before $\overline{CS}$ Low		0.0	–	ns
10	t_{SUA}	A[2:0] Setup Before $\overline{AS}$ Low		15.0	–	ns
11	t_{HLDA}	A[2:0] Hold After $\overline{AS}$ Low	Groups 0,1,2,4 Groups 3,5	0.0 3.0	–	ns OCLK Cycles
12	t_{DCSDTL}	Data Valid to $\overline{DTACK}$ Low	Groups 0,1,2,4 Groups 3,5	–	10.0 3.0	ns OCLK Cycles
13	t_{HLDD}	Write Data Hold After $\overline{CS}$ High		0.0	–	ns
14	t_{CYCLE_CS}	Minimum $\overline{CS}$ Width	Groups 0,1,2,4 Groups 3,5	30.0 4.0	–	ns OCLK Cycles
15	t_{HLDRCS}	READ Hold After $\overline{CS}$ High		0.0	–	ns
16	t_{WRREC}	Write Recovery Time	Groups 0,1,2,4 Groups 3,5	30.0 3.0	–	ns OCLK Cycles
17	t_{DCSDTH}	$\overline{CS}$ High to DTACK Three-State	Groups 0,1,2,4 Groups 3,5	–	10.0 5.0	ns OCLK Cycles
18	t_{DELZL}	$\overline{CS}$ Low to Data Driven	Groups 0,1,2,4 Groups 3,5	9.0 1.0	–	ns OCLK Cycles
19	t_{DELD}	$\overline{CS}$ Low to Data Valid	Groups 0,1,2,4 Groups 3,5	–	15.0 3.0	ns OCLK Cycles
20	t_{DELLZ}	$\overline{CS}$ High to Data Three-State	Groups 0,1,2,4 Groups 3,5	5.0 0.5	–	ns OCLK Cycles
21	t_{SUD}	Data Setup Before $\overline{CS}$ Change		15.0	–	ns
22	t_{HLDW}	AS Hold after $\overline{CS}$ Low	Groups 0,1,2,4 Groups 3,5	10.0 2.0	–	ns OCLK Cycles
23	t_{TDLY}	Delay from $\overline{COE}$		–	15	ns
24	t_{DELDTL}	$\overline{CS}$ High to $\overline{DTACK}$ Low	Groups 0,1,2,4 Groups 3,5	–		ns OCLK Cycles
25	t_{DELDTH}	$\overline{CS}$ High to $\overline{DTACK}$ High	Groups 0,1,2,4 Groups 3,5	–		ns OCLK Cycles

All parameters in the timing tables apply for T_A = 0 °C to 70 °C, .

10.4 L64705 Pin Descriptions

This section describes the signal pins of the L64705 concatenated decoder.

The pin descriptions include a pin description summary, which lists the electrical characteristics of each pin. The summary is followed by a pin list, which relates the signal on each pin to a pin number on the 100 pin PQFP. A figure is also provided to show the pin location for each signal on the package. Mechanical descriptions of packaging and ordering information follow this section.

L64705 Pin Description

Table 10.4 summarizes the pins on the L64705. The table provides the signal types for both output and input pins, and the drive capacity for outputs.

Table 10.4 L64705 Pin Description Summary

Mnemonic	*Description*	*Type*	*Drive (mA)*	*Active*
A[2:0]	Address	TTL Input with pulldown	–	–
$\overline{AS}$	Address Strobe	TTL Input with pullup	–	Low
BCLKOUT	Byte Clock Out	Output	4	-
CO[7:0]	Channel Output	3-State Output	4	–
$\overline{COE}$	Channel Output Enable	TTL Input with pullup	–	Low
$\overline{CS}$	Chip Select	TTL Input with pullup	–	Low
D[7:0]	Data	Bidirectional TTL IO	–	–
DVALIDIN	Data Enable Input	TTL Input with pullup	–	High
DVALIDOUT	Data Valid Out	Output	4	High
$\overline{DTACK}$	Data Acknowledge	3-State Output	4	Low
ERRORFIX	Error Fixed	3-State Output	4	High
$\overline{ERROROUT}$	Uncorrected Error Flag	3-State Output	4	Low
ICLK	Input Clock	TTL Input	–	–
$\overline{INT}$	Interrupt Request	3-State Output	4	Low
LP2	PLL Loop Filter	Input	–	–
OCLK	Output Clock	Output	–	–
PCLK	PLL Output Clock	Output	4	–
PLLVDD	PLL Vdd	Input	–	–
PLLVSS	PLL Vss	Input	–	–

Mnemonic	*Description*	*Type*	*Drive (mA)*	*Active*
PLLAGND	PLL Analog Ground	Input	–	–
PLLVSS	PLL Vss	Input	–	–
READ	Read/Write Strobe	TTL Input with pullup	–	Low
SYNC	Sync Status Flag	Output	4	–
S0[2:0]	Symbol 0 Input	TTL Input	–	–
S1[2:0]	Symbol 1 Input	TTL Input	–	–
S2[1:0]	Symbol 2 Input	TTL Input	–	–

Decoder Pin List

Table 10.7 is the pin list for the L64705.

Table 10.5
Pin List for the 100-pin PQFP

Pin	***Signal***	***Pin***	***Signal***	***Pin***	***Signal***	***Pin***	***Signal***
1	VDD	26	*reserved*	51	VDD	76	PLLVSS
2	*reserved*[1]	27	VSS	52	*reserved*	$\overline{77}$	VSS
$\overline{3}$	VDD	28	VDD	53	VDD	*78*	VDD
$\overline{4}$	VSS	29	*reserved*	54	VSS	*79*	*reserved*
5	*reserved*	30	VDD	55	*reserved*	80	VDD
6	CO.0	31	*reserved*	56	S1.2	81	*reserved*
7	CO.1	32	$\overline{\text{COE}}$	57	S1.1	82	$\overline{\text{INT}}$
8	*reserved*	33	A.0	58	S1.0	83	$\overline{\text{DTACK}}$
9	CO.2	34	A.1	59	*reserved*	84	D.7
10	CO.3	35	*reserved*	60	S0.2	85	D.6
11	CO.4	36	*reserved*	61	S0.1	86	*reserved*
12	VDD	37	RESET	62	S0.0	87	D.5
13	VSS	38	VSS	63	*reserved*	88	D.4
14	CO.5	39	*reserved*	64	ICLK	89	SYNC
15	CO.6	40	VSS	65	*reserved*	90	VSS
16	CO.7	41	VDD	66	VSS	91	VDD
17	*reserved*	42	*reserved*	67	OCLK	92	*reserved*
18	BCLKOUT	43	A.2	68	VDD	93	VSS
19	DVALIDOUT	44	$\overline{\text{AS}}$	69	*reserved*	94	S2.1
20	ERRORFIX	45	$\overline{\text{CS}}$	70	DVALIDIN	95	D.3
21	VDD	46	READ	71	VSS	96	D.2
22	VSS	47	VSS	72	PCLK	97	*reserved*
23	$\overline{\text{ERROROUT}}$	48	*reserved*	73	PLLVDD	98	D.1
24	FSTARTOUT	49	*reserved*	74	PLLAGND	99	D.0
25	*reserved*	50	*reserved*	75	LP2	100	S2.0

1. Reserved Pins must be left unconnected by the user.

Figure 10.7
100-Pin PQFP Pinout

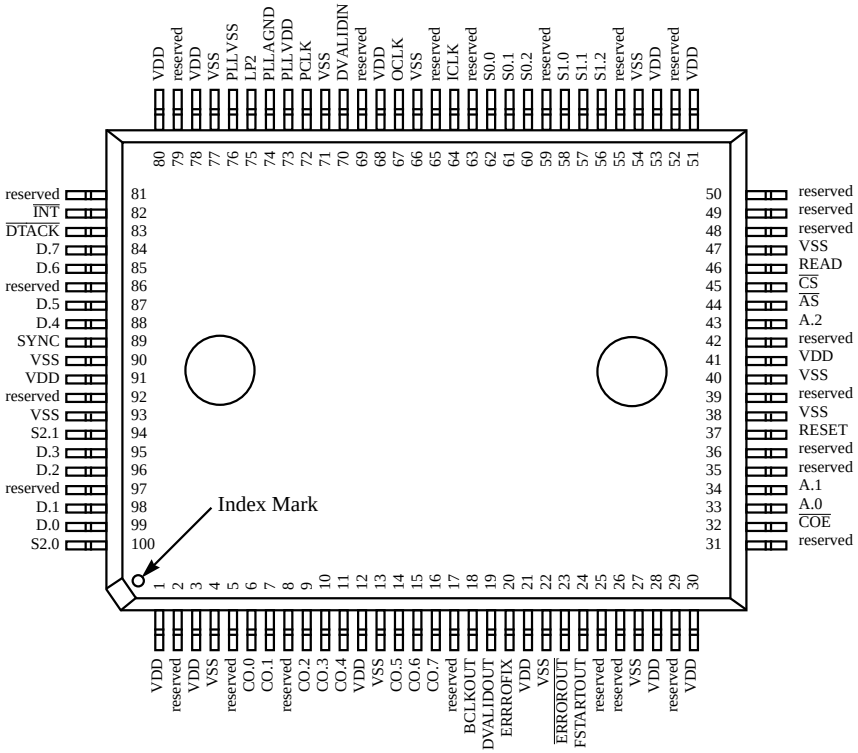
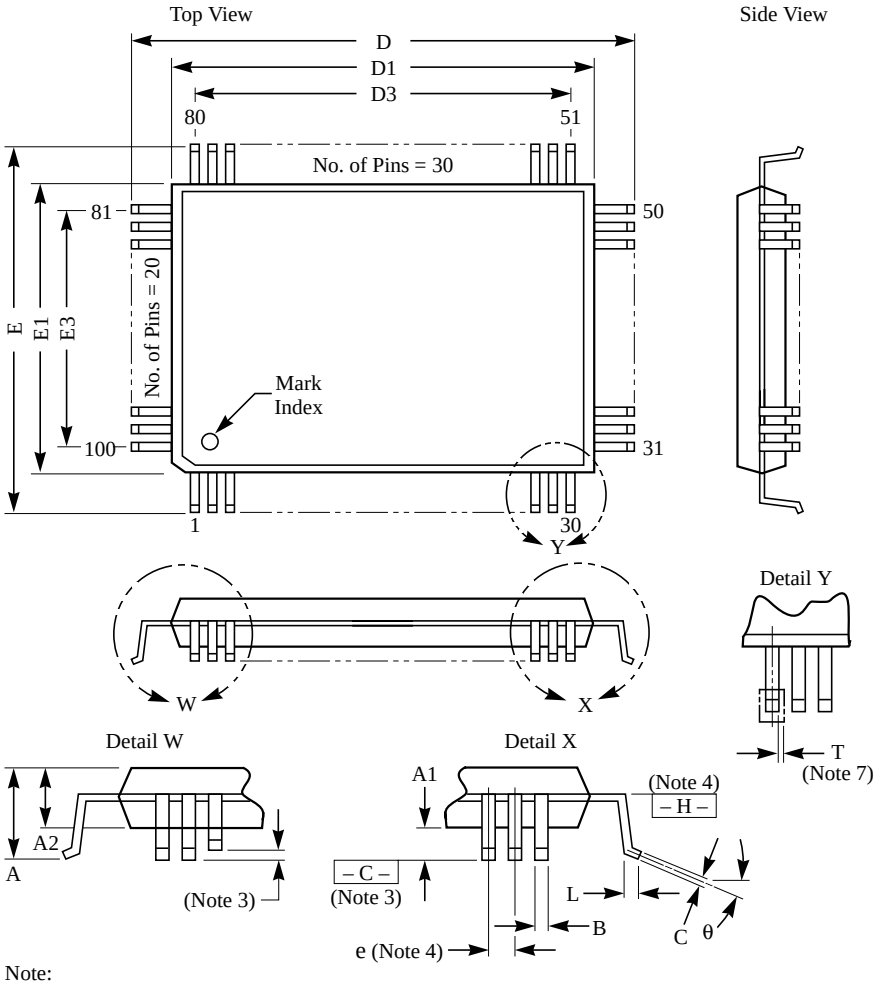


Figure 10.8
100-Pin PQFP
Mechanical Drawing



Dimension		mm
A	**Max**	3.40
A1	**Min**	0.25
	Max	0.35
A2	**Min**	2.55
	Nom	2.80
	Max	3.05
B	**Min**	0.22
	Nom	0.30
	Max	0.38
C	**Min**	0.12
	Max	0.25
D	**Min**	23.6
	Nom	23.9
	Max	24.1
D1	**Min**	19.9
	Nom	20.0
	Max	20.1
D	**Ref**	18.8
e	**BSC**	0.65
E	**Min**	17.6
	Nom	17.9
	Max	18.1
E1	**Min**	13.9
	Nom	14.0
	Max	14.1
E	**Ref**	12.3
L	**Min**	0.65
	Nom	0.80
	Max	0.95
T	**Max**	0.10
θ	**Min**	0°
	Max	7°

Note:
1. Total number of pins is 100.
2. Drawing is not to scale.
3. Coplanarity of all leads shall be within 0.10 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4. Datum plane – H – is located at mold parting line and is coincident with the bottom of the lead, where the lead exits the plastic body. Lead pitch determined at – H –.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. These dimensions to be determined at – H –.
6. Dimensions D3 and E3 to be centered relative to dimensions D1 and E1, respectively, ±0.200 mm.
7. Tolerance window for lead skew from true position is determined at seating plane – C –.
8. For board layout and manufacturing, you may obtain engineering drawings from your LSI Logic Products marketing representative by requesting the outline drawing for package code PB.

MD92.PB