High-Frequency Signal Processing IC for GSM/EGSM Digital Cellular Standards

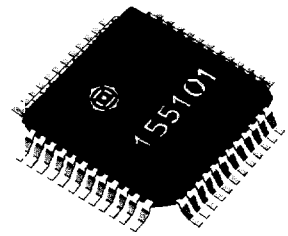
HD155101F

The GSM digital cellular system, developed and constructed in Europe, has also been introduced in various other parts of the world, including Asia, Oceania, and parts of America, and with approximately 30 million subscribers to date, represents the world's largest digital cellular market. With the constant demand for smaller and lighter portable phones, together with longer call and standby times and higher performance, drastic improvements are also demanded of the electronic components used in these products, including higher levels of integration, higher speed, a smaller mounting area, and lower power consumption.

- Offset PLL [1] system used on transmission side: major reduction in out-of-band noise
- High-level integration of major part of high-frequency signal processing unit
- Linear control possible for AGC [2] amplifier

In response to these needs, the HD155101F was developed in collaboration with the British GSM system consulting company The Technology Partnership plc (TTP), as a single-chip RF/IF*3 unit signal processing IC for GSM/EGSM*4 applications that offers the possibility of smaller and cheaper systems.

Extension to the PCN*5/PCS standards was also taken into consideration in designing the HD155101F, and development is currently under way in this area using the same package and pin arrangement. Further developments based on this technology are planned for the future to support systems such as CDMA and PDC.



Features

■ High-level integration

• The transmitter includes an orthogonal modulation circuit, offset PLL-type frequency conversion circuit, and fre-

Table 1 HD155101F Specifications

Item		Specification
Operating voltage range		2.7 V to 3.6 V
Operating temperature range		–20 to +75°C
Current dissipation (at 3 V)	Reception	34 mA [+LNA] (typ.)
	Transmission	31 mA (typ.)
	Power save mode	1 µA (max.)
Operating frequency	Reception side	925 to 960 MHz
	Transmission side	880 to 915 MHz
AGC gain range		–30 to +50 dB (typ., at 0.15 V to 2.3 V voltage setting)
Transmission side spurious output suppression ratio	Carrier	–40 dBc (typ.), –33 dBc (min.)
	Upper sideband	–40 dBc (typ.), –33 dBc (min.)
Transmission side out-of-band noise	925 MHz	–157 dBc/Hz (typ.)
	935 MHz	–165 dBc/Hz (typ.)
Package		LQFP-48

quency divider, and the receiver includes a first mixer, second mixer, AGC amplifier, and orthogonal demodulation circuit. A low-noise amplifier (LNA) negative feedback bias circuit is also provided on-chip, simplifying the configuration of a highly stable LNA circuit.

• A superheterodyne method is employed that enables commonality of the RF local frequency and IF local frequency during transmission/reception, with the first IF frequency set to 225 MHz. This setting resulted from investigations into the prevention of spurious signal leakage into the transmission band in PCN/PCS (DCS1800/PCS1900) applications.

■ Offset PLL system

• An offset PLL system is used in which VCO output is used directly in frequency conversion on the transmission side, resulting in a major reduction in out-of-band noise. This eliminates the need for an RF band SAW*6 filter and duplexer, reducing the number of parts and avoiding power loss due to filter insertion. In addition, this system provides compatibility with the EGSM standard.

• With previous systems, AM-AM conversion distortion occurred in the power amp stage due to the AM waveform generated after mixing, but with the offset PLL system, the direct use of VCO output as the output signal ensures a steady output signal and eliminates the need for anti-distortion measures.

■ AGC amplifier

• Linear control over a wide range of –30 dB to +50 dB is possible with a gain control voltage setting between 0.15 V and 2.3 V.

• By simultaneously controlling attenuator attenuation and amplifier gain, taking the dynamic range into consideration, it is possible to achieve a 10.4 dB (typ.) noise figure at 50 dB gain and a –17 dBm (typ.) compression point at –30 dB gain.

■ LNA negative feedback bias circuit

• Use of an on-chip negative feedback bias circuit enables the LNA block to be configured with a small number of parts. This circuit monitors the current flowing in external transistors and performs control to ensure a steady current, enabling stable reception characteristics to be achieved.

■ Power saving

• Three control signals are used to control the reception RF, reception IF, and transmission systems.

*1: Phase-locked loop
*2: Automatic gain control
*3: Intermediate frequency
*4: Extended GSM (extended GSM frequency band specifications)
*5: Personal Communications Network
*6: Surface acoustic wave

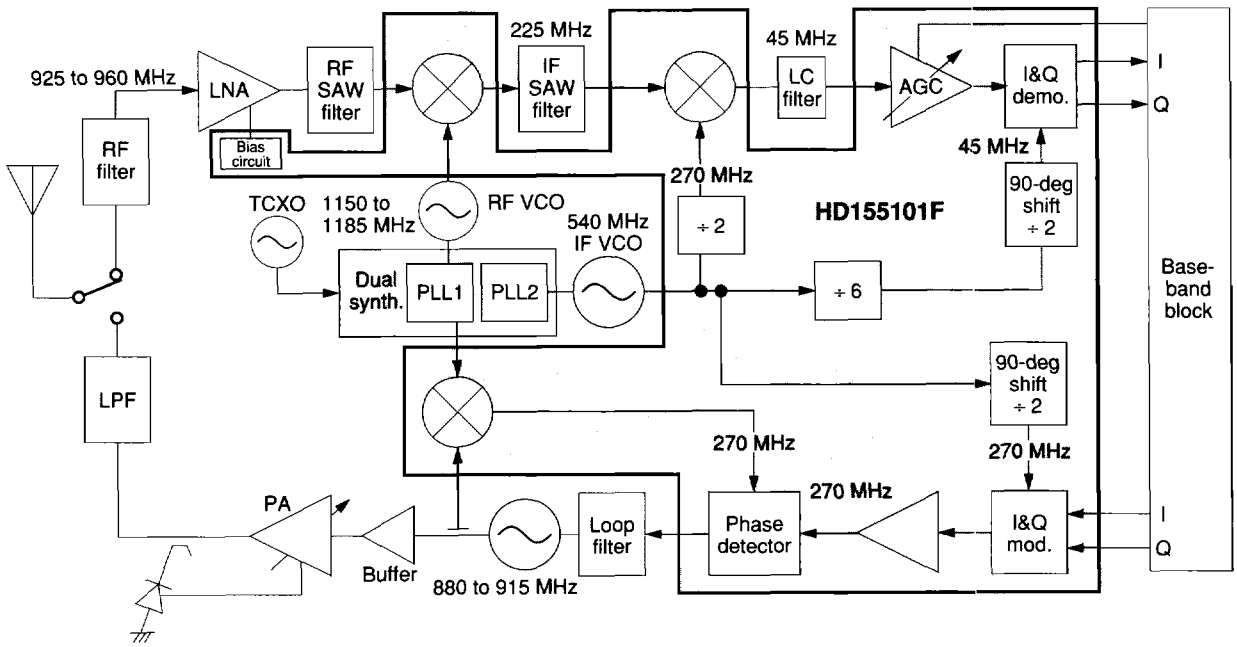


Fig. 1 HD155101F Configuration