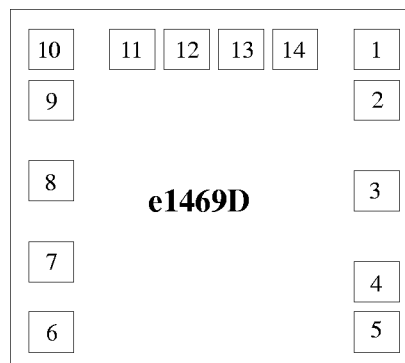


32 kHz Clock CMOS IC with Electroset & Crescendo Alarm

Features

- 32 kHz crystal oscillator
- 1.1 - 1.8 V operating voltage range
- Integrated capacitors, mask-selectable
- Low impedance output for bipolar stepping motors
- Crescendo alarm with autostop function and snooze (for repeated alarm) with light
- Electroset
- Pin compatible to e1466D, e1467D
- Suitable for up to 12.5 pF quartz

Pad Configuration



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Figure 1.

General Description

The e 1469D is an integrated circuit in CMOS Silicon Gate Technology for analog clocks. It consists of an oscillator, frequency divider, output pulse formers, push-pull motor drivers, electroset for electronic time setting and alarm output with volume modulation. Integrated capacitors are mask-selectable to accommodate the external quartz crystal. Additional capacitance can be selected through pad bonding, for trimming the oscillator frequency. This circuit is used mainly in applications using quartz-synchronized alarm clocks driven by a bipolar stepping motor. Here, the IC's low-power requirement, low operating voltage, increasing alarm volume and repeated snooze function (with light and the autostop facility) are used to an advantage.

| Pin | Symbol | Function |
|-------------|------------------------|--|
| 2 or 10 | V _{DD} | Positive supply voltage |
| 0 | V _{SS} | Negative supply voltage |
| 1 | OSCIN | Oscillator input |
| 10 or 2 | OSCOUT | Oscillator output |
| 5 or 6 or 7 | MOT1 | Motor drive output 1 |
| 4 | MOT2 | Motor drive output 2 |
| 6 or 7 | ALIN/ SNZ/ MTEST | Alarm activation and snooze or motor test |
| 6 or 7 | LIGHT | Light output driver |
| 3 | ALOUT | Alarm output driver |
| 8 | ESET/ TEST | Electroset or motor test input |
| 14-11 | SC1 to SC4 | Trimming capacitor inputs |

Absolute Maximum Ratings

| Parameters | Symbol | Value | Unit |
|--|------------------|--|------|
| Supply voltage | V _{SS} | -0.3 to +5 V | V |
| Input voltage range, all inputs | V _{IN} | (V _{SS} - 0.3V) ≤ V _{IN} ≤ (V _{DD} + 0.3 V) | V |
| Output short circuit duration | | Indefinite | |
| Power dissipation (DIL package) | P _{tot} | 125 mW | mW |
| Operating ambient temperature range | T _{amb} | -20 to +70 | °C |
| Storage temperature range | T _{stg} | -40 to +125 | °C |
| Lead temperature during soldering at 2 mm distance, 10 seconds | T _{sld} | 260 | °C |

Absolute maximum ratings define parameter limits which, if exceeded, may permanently change or damage the device. All inputs and outputs on TEMIC Semiconductors circuits are protected against electrostatic

discharges. However, precautions to minimize the build-up of electrostatic charges during handling are recommended. The circuit is protected against supply voltage reversal for typically 5 minutes.

Functional Description

Oscillator

An oscillator inverter with feedback resistor is provided for generation of the 32768 Hz clock frequency. Values for the fixed capacitors at OSCIN and OSCOUT are mask-selectable (see note 3 of operating characteristics). Four capacitor switches SC1 to SC4 enable the addition of integrated trimming capacitors to OSCIN and OSCOUT, providing 15 tuning steps.

Trimming Capacitors

A frequency variation of typ. 3 ppm for each tuning step is obtained by bonding the capacitor switch pads to V_{DD} . As none of these pads are bonded, the IC is in an untrimmed state. Figure 4 shows the trimming curve characteristic.

Note: For applications which utilize this integrated trimming feature, TEMIC will determine optimum values for the integrated capacitors C_{OSCIN} and C_{OSCOUT} .

| Capacitor switches | | | | Trimming Step |
|--------------------|-----|-----|-----|---------------|
| SC4 | SC3 | SC2 | SC1 | |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 |
| 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 0 | 0 | 12 |
| 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 1 | 0 | 14 |
| 1 | 1 | 1 | 1 | 15 |

Motor Drive Output

The e1469D contains two push-pull output buffers for driving bipolar stepping motors. During a motor pulse, the n-channel device of one buffer and the p-channel device of the other buffer is activated. Both n-channel transistors are on and conducting, between output pulses. The outputs are protected against inductive voltage spikes with diodes to both supply pins. The motor output period and pulse width are mask programmable over a wide range of values, as listed below:

Available motor periods (T_M):

62.5, 125, 250, 500 ms

and 1, 2, 4, 6, 8, 10, 12, 16, 20, 24, 30, 40, 60, 120 s

Available pulse widths (t_M):

7.8, 11.7, 15.6, 23.4, 31.2, 46.9, 62.5, 117 and 125 ms

Available motors periods during electroset (T_{M2}): 0.125, 0.250, 0.500, 1.0, 2.0 s

Note: Restrictions prohibit combinations of certain motor pulse widths with motor periods.

Electroset

When electroset is activated, all the counters are reset and a single motor pulse is generated. If electroset is then held active for longer than 1 s or 500 ms (mask-selectable), the e1469D generates a constant series of accelerated motor pulses thus enabling the fast setting of the time. On releasing electroset all the counters are again reset. This avoids the risk of a natural pulse arising whilst waiting for a time standard. Fine tuning and synchronization can therefore be carried out by single stepping. When the electroset function is activated, any motor pulse in progress is completed. A mask option also enables an electroset to be activated either by connection to V_{DD} or V_{SS} . The principle of electroset is illustrated in figure 3.

Alarm Output

The alarm output driver consists of a push-pull stage for driving a speaker via an external bipolar transistor. The output is configured for npn bipolar capability. The output is an alarm tone modulated by a low frequency. The crescendo alarm enables the output volume level to rise in two distinct crescendo steps. At the end of the second crescendo step, the highest level of the alarm volume is achieved and held. By using a metal mask option, the crescendo steps can be selected to be either in 4 seconds or 8 seconds. The mask option also enables a range of volume levels, tone frequencies, modulation frequencies, and the on/off times to be selected.

Alarm Input

Alarm activation is either to V_{DD} or V_{SS} by a mask option. By connecting the alarm input to V_{DD} (V_{SS}), the alarm is activated for the duration of the autostop time. Thereafter, it stops automatically. In order to restart the alarm after automatic stop, the alarm input must be momentarily disconnected from V_{DD} (V_{SS}) and then reconnected. The alarm can be stopped before the autostop time by disconnecting the alarm input from V_{SS} (V_{DD}). Connecting the alarm input to V_{SS} (V_{DD}) whilst the alarm is active stops the alarm for the duration of the snooze time. At the onset of this snooze time the LIGHT pad sinks the current (suitable for a pnp driver) for a duration of some seconds (optional 0.5 to 15.5 s in 0.5 s increments). Thereafter, the alarm becomes active again. Once snooze is activated, the snooze time cannot be extended by renewed connection to V_{SS} (V_{DD}). The snooze activation polarity is always opposite to alarm activation. The metal mask option enables the snooze and the autostop periods to be selected from a range of values.

Test Functions

For test purposes, the ALIN/SNZ/MTEST pad is open. With a high resistance probe, ($R \geq 10 \text{ M}\Omega$, $C \leq 20 \text{ pF}$) a test frequency of 128 Hz can be measured at the ALIN/SNZ/MTEST pad. An additional test feature on the e1469D enables the fast testing of the device's alarm functions. It is activated by forcing both MOT1 and MOT2 pads to V_{DD} . This results in the alarm counters being accelerated by a factor of 64. They remain in this state as long as both MOT1 and MOT2 are held to V_{DD} . This test enables the e1469D's alarm modulation (on/off, autostop and snooze times) to be fast tested with the device clocked by the crystal. Releasing MOT1 and MOT2 returns the e1469D to normal operation.

Operating Characteristics

$V_{DD} = 0$, $V_{SS} = -1.5$, $T_{amb} = +25^{\circ}\text{C}$; unless otherwise specified

All voltage levels are measured with reference to V_{DD} . Test crystal as specified below.

| Parameters | Test Conditions / Pins | Symbol | Min. | Typ. | Max. | Unit |
|---|---|----------------------------|-----------|-------------|-----------|--------------------------------|
| Operating voltage | | V_{SS} | -1.1 | -1.5 | -1.8 | V |
| Operating temperature | | T_{amb} | -20 | | +70 | $^{\circ}\text{C}$ |
| Operating current | SC1 to SC4 = V_{DD} , $R_L = \infty$ | I_{SS} | | -0.8 | -3 | μA |
| Motor drive output | | | | | | |
| Motor output current | $V_{SS} = -1.2\text{ V}$, $R_L = 200\ \Omega$ | I_M | ± 4.3 | | | mA |
| Motor period | | T_M | | Mask option | | |
| Motor period during electroset | | T_{M2} | | Mask option | | |
| Motor pulse width | | t_M | | Mask option | | |
| Oscillator | | | | | | |
| Startup voltage | Within 2 s | V_{START} | -1.2 | | -1.8 | V |
| Frequency stability | $\Delta V_{SS} = 100\text{ mV}$ $V_{SS} = -1.3\text{ to }-1.8$ | $\Delta f/f$ | | 0.2 | 0.6 | ppm |
| Integrated input capacitance | Note 3 | C_{OSCIN} | | Mask option | | |
| Integrated output capacitance | Note 3 | C_{OSCOUT} | | Mask option | | μA |
| Input current SC1 to SC4 | $V_{IN} = -1.0\text{ V}$ $V_{IN} = V_{DD}$, peak current | I_{SCINL} I_{SCINH} | 1 0.2 | 5 0.6 | 25 2.0 | μA μA |
| Alarm/ light output | | | | | | |
| Output current for driving nnp-transistor n-channel | $V_{SS} = -1.2\text{ V}$ $R_3 = 100\text{ k}\Omega$ | I_{ANn} | 1 | 3 | 10 | μA |
| p-channel | $R_2 = 1\text{ k}$, note 2 | I_{ANp} | -0.5 | -1 | | mA |
| Output current for driving pnp-transistor n-channel | $V_{SS} = -1.2\text{ V}$ $R_3 = 1\text{ k}\Omega$ | I_{APn} | 0.5 | 1 | | mA |
| p-channel | $R_2 = 100\text{ k}\Omega$, note 2 | I_{APp} | -1 | -3 | -10 | μA |
| Alarm options | | | | | | |
| Tone frequency | | f_A | | | | Hz |
| Crescendo duties | | D_{CRES} | | | | |
| Crescendo times | | t_{CRES} | | | | s |
| Modulation frequency | | f_{MOD} | | | | Hz |
| On/ Off time | Note 4 | $t_{ON/OFF}$ | | | | s |
| Autostop time | | t_{ASTOP} | | | | s |
| Snooze time | | t_{SNZ} | | | | s |
| Light option | | | | | | |
| On-time | | t_{LIGHT} | | Mask option | | s |
| Alarm input/ motor test input/ snooze input | | | | | | |
| Input current | $ALIN = V_{DD}$ | I_{AINavg} | 1 | 3 | 10 | μA |
| Input current | $ALIN = V_{SS}$, peak current | I_{AINL} | -1 | -3 | -10 | μA |
| Input debounce delay | | | 23.4 | | 31.2 | ms |
| Snooze debounce time | Optional | t_{SNZd} | 23.4 | | 31.2 | ms |
| | Optional | | 7.8 | | 15.6 | ms |

Note 1: Typical parameters represent the statistical mean value

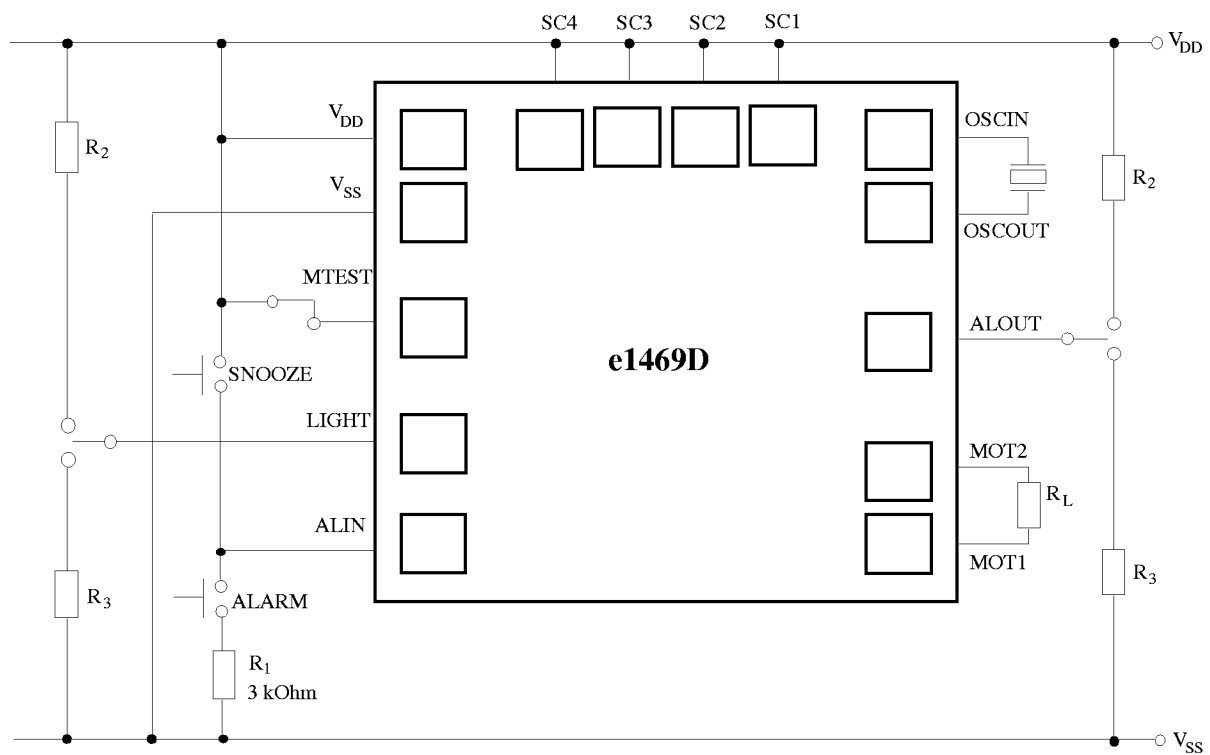
Note 2: See test circuit

Note 3: Values can be selected in 1 pF steps. A total capacitance ($C_{OSCIN} + C_{OSCOUT}$) of 38.5 pF is available

Note 4: On/Off or continuous alarm signal in 3rd stage

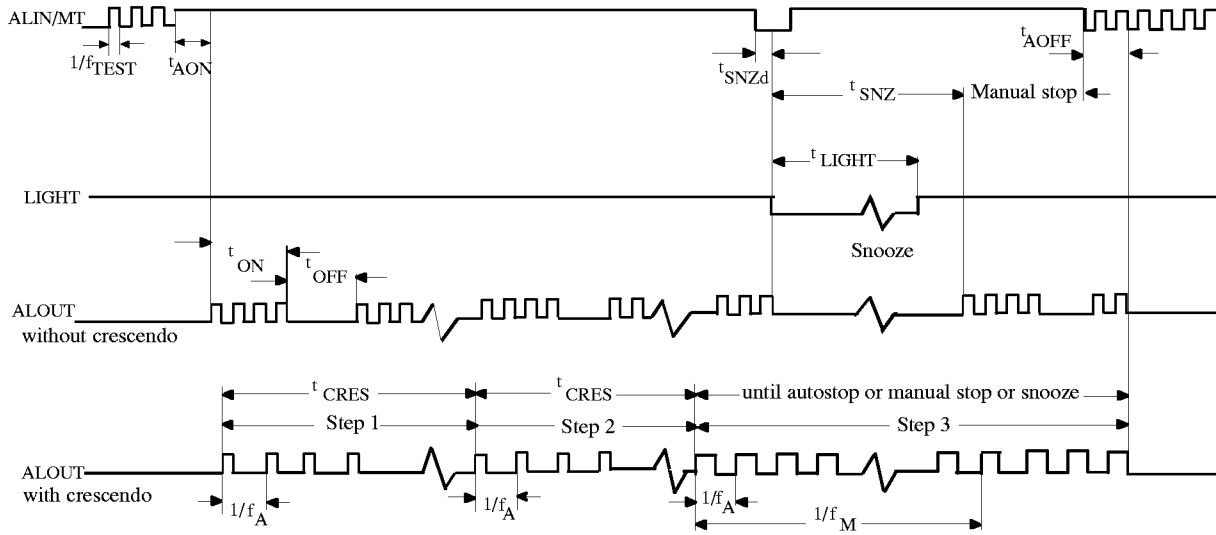
Test Crystal Specification

| | |
|-----------------------|------------------------------|
| Oscillation frequency | $f_{OSC} = 32768 \text{ Hz}$ |
| Series resistance | $R_S = 30 \text{ k}\Omega$ |
| Static capacitance | $C_O = 1.5 \text{ pF}$ |
| Dynamic capacitance | $C_1 = 3.0 \text{ fF}$ |
| Load capacitance | $C_L = 10 \text{ pF}$ |



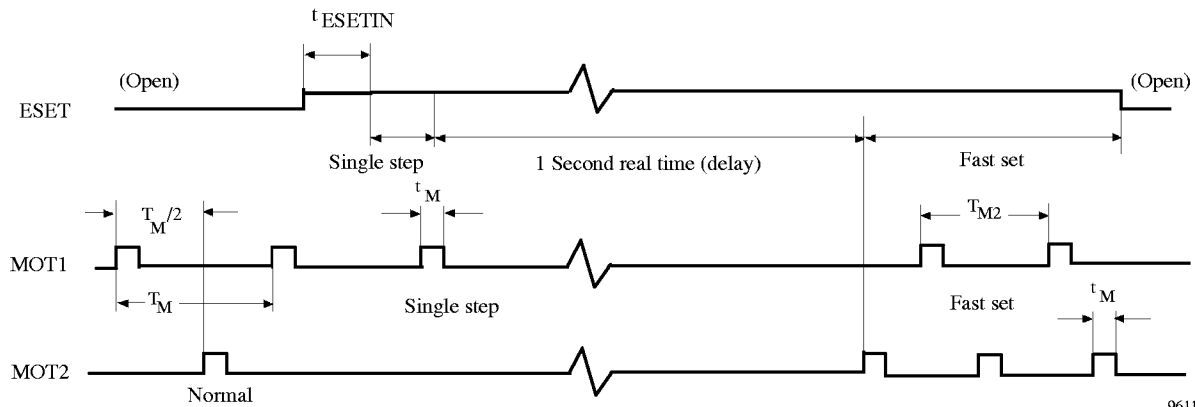
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Figure 1. Functional test



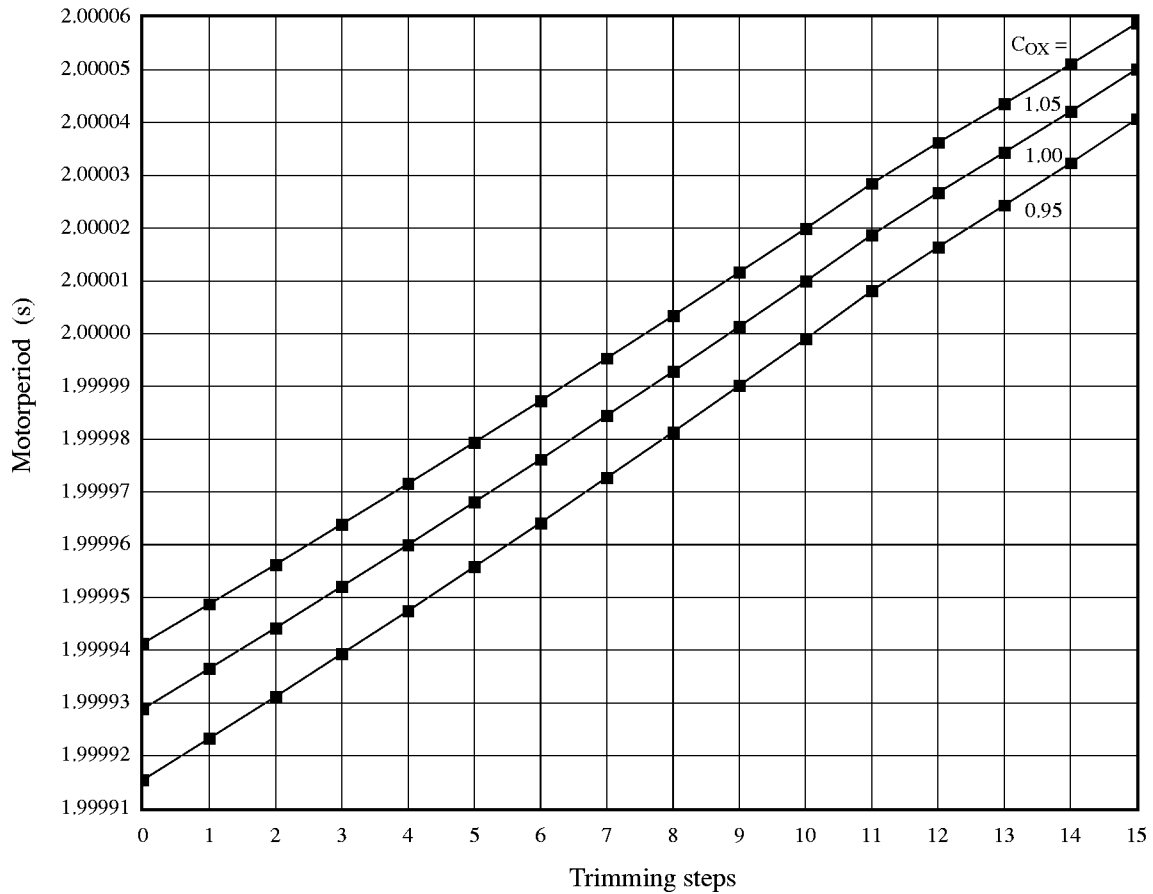
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Figure 2. Timing diagram for alarm function



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Figure 3. Electroset



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Figure 4. Typical trimming curve characteristic for T_M of 2 secs

C_{OX} means frequency deviation due to production process variations.

Trimming inputs SC1 ... SC4 are binary weighted, i.e., SC1 ... SC4 = 0 corresponds to trimming step 0
 SC1 ... SC4 = 1 corresponds to trimming step 15

LSB = SC1

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