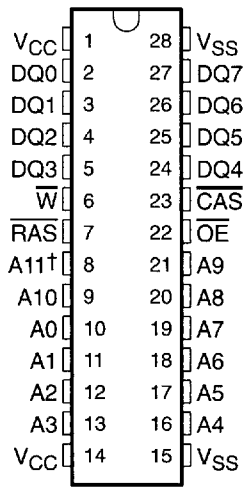
This data sheet is applicable to all TMS41x800As and TMS42x800A/Ps symbolized by Revision "E" and subsequent revisions as described in the device symbolization section.

- **Organization . . . 2097152 × 8**
- **Single 3.3-V or 5-V Power Supply**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR EDO CYCLE MIN
'41x800A-50	50 ns	13 ns	25 ns	20 ns
'41x800A-60	60 ns	15 ns	30 ns	25 ns
'41x800A-70	70 ns	18 ns	35 ns	30 ns
'42x800A/P-50	50 ns	13 ns	25 ns	20 ns
'42x800A/P-60	60 ns	15 ns	30 ns	25 ns
'42x800A/P-70	70 ns	18 ns	35 ns	30 ns

- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ ($\overline{CBR}$) Refresh**
- **Long Refresh Period and Self-Refresh Option (TMS42x800AP)**
- **High-Impedance State Unlatched Output**
- **Low Power Dissipation**
- **High-Reliability Plastic 28-Lead 400-Mil-Wide Surface-Mount Thin Small-Outline Package (TSOP) (DGC Suffix) and 28-Lead 400-Mil-Wide Surface-Mount Small Outline J-Lead (SOJ) Package (DZ Suffix)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Fabricated Using Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)**

DZ/DGC PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A11†	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ7	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{CC}	3.3-V or 5-V Supply‡
V_{SS}	Ground
$\overline{W}$	Write Enable

† A11 is NC (no internal connection) for TMS417800A and TMS427800A/P.

‡ See Available Options Table

description

The TMS41x800A and TMS42x800A series are sets of high-speed, 16777216-bit dynamic random-access memories (DRAMs) organized as 2097152 words of eight bits each. The TMS42x800AP series is a set of high-speed, low-power, self-refresh, 16777216-bit DRAMs organized as 2097152 words of eight bits each. Both series employ TI's state-of-the-art EPIC technology for high performance, reliability, and low power.

AVAILABLE OPTIONS

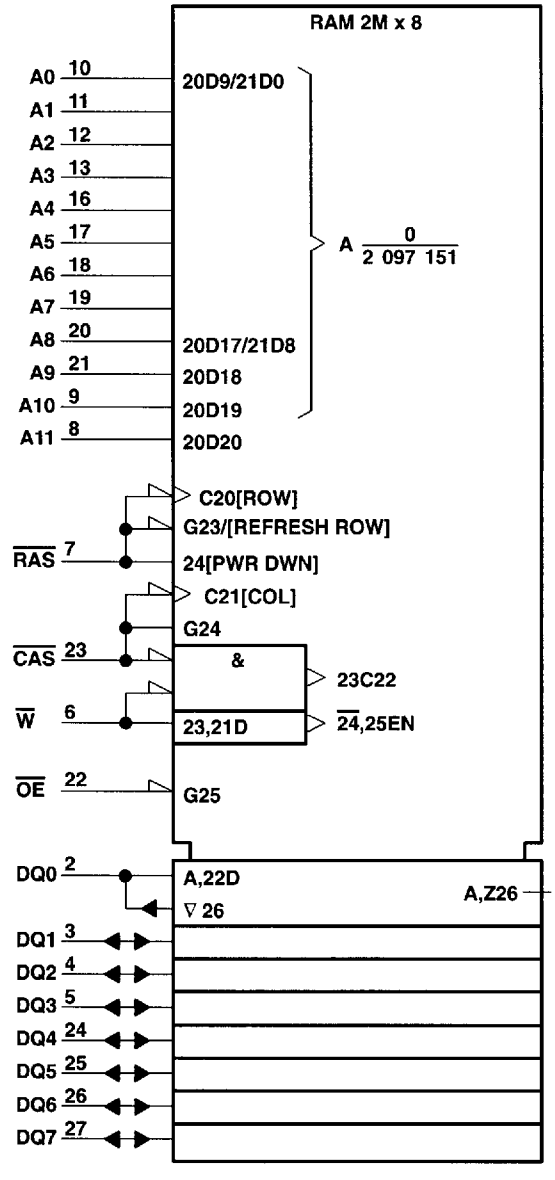
DEVICE	POWER SUPPLY	SELF-REFRESH BATTERY-BACKUP	REFRESH CYCLES
TMS417800A	5 V	—	2048 in 32 ms
TMS416800A	5 V	—	4048 in 64 ms
TMS426800A	3.3 V	—	4096 in 64 ms
TMS426800AP	3.3 V	Yes	4096 in 128 ms
TMS427800A	3.3 V	—	2048 in 32 ms
TMS427800AP	3.3 V	Yes	2048 in 128 ms

description (continued)

These devices feature maximum $\overline{RAS}$ access times of 50, 60, and 70 ns. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

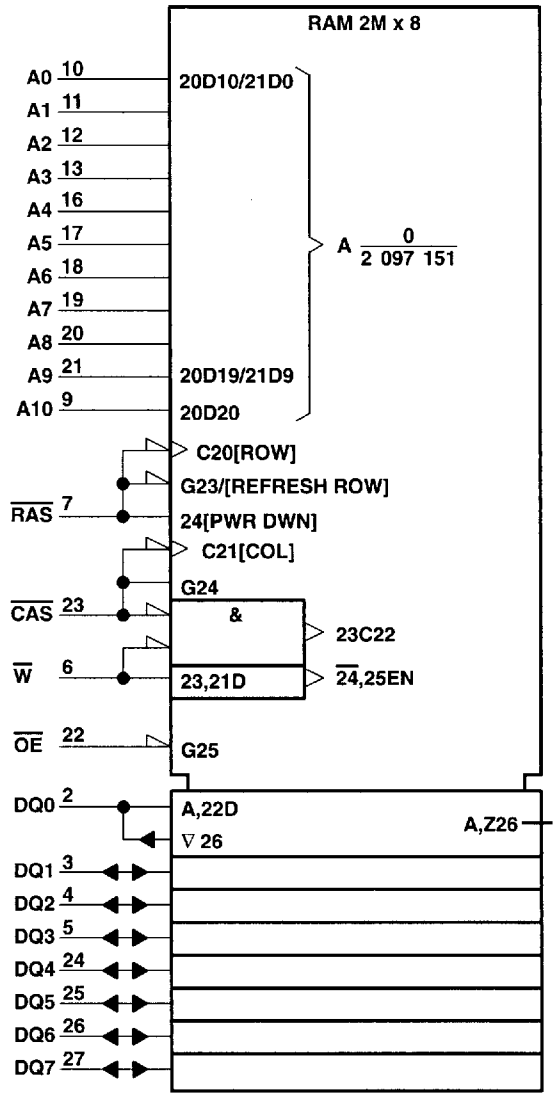
The TMS416800A and TMS417800A are offered in a 28-lead plastic surface-mount SOJ package (DZ suffix). The TMS426800A/P and TMS427800A/P are offered in a 28-lead plastic surface-mount SOJ package (DZ suffix) and a 28-lead plastic surface-mount TSOP (DGC suffix). These packages are designed for operation from 0°C to 70°C.

logic symbol for TMS416800A and TMS426800A/P†



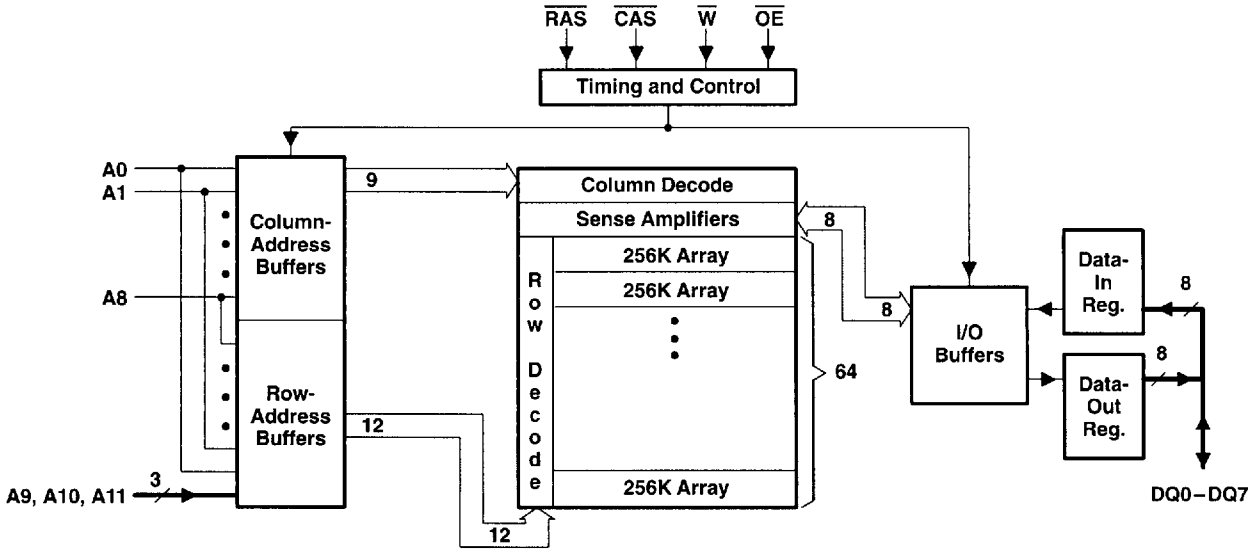
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

logic symbol for TMS417800A and TMS427800A/P†

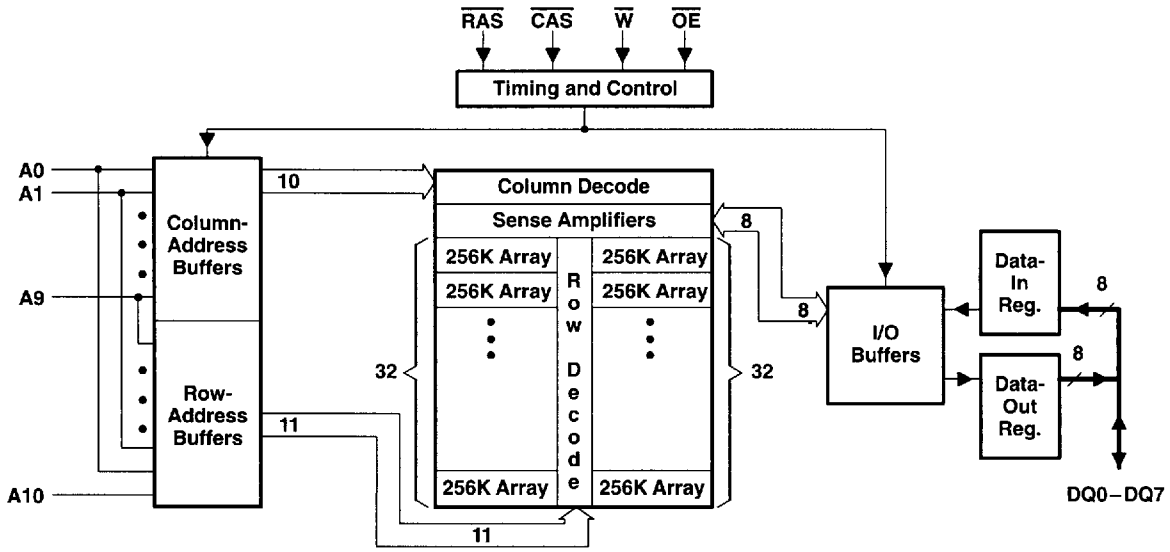


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

functional block diagram (TMS416800A and TMS426800A/P)



functional block diagram (TMS417800A and TMS427800A/P)



operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold, and for address multiplex, is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum row-address strobe ($\overline{RAS}$) low time.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while column-address strobe ($\overline{CAS}$) is high. The falling edge of $\overline{CAS}$ latches the column addresses and enables the output, which allows the devices to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ goes low. This performance improvement is referred to as enhanced-page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{AA} max (access time from column address) and t_{RAC} (access time from $\overline{RAS}$) have been satisfied. In the event that column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CPA} (access time from $\overline{CAS}$ precharge) or t_{CAC}.

address: A0–A11 (TMS416800A and TMS426800A/P) and A0–A10 (TMS417800A and TMS427800A/P)

Twenty-one address bits are required to decode each of the 2097152 storage cell locations. For the TMS416800A and TMS426800A/P, 12 row-address bits are set up on A0 through A11 and latched on the chip by the $\overline{RAS}$. Nine column-address bits are set up on A0 through A8. For TMS417800A and TMS427800A/P, eleven row-address bits are set up on inputs A0 through A10 and latched on the chip by $\overline{RAS}$. Ten column-address bits are set up on A0 through A9. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable because it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffers and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode, and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0–DQ7)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ is already low, and the data is strobed in by $\overline{W}$ with setup and hold time referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0–DQ7)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{CAS}$) as long as t_{RAC} and t_{AA} are satisfied.

$\overline{\text{RAS}}$-only refresh

TMS416800A, TMS426800A/P

A refresh operation must be performed once every 64 ms (128 ms for TMS426800AP) to retain data. The refresh operation can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

TMS417800A, TMS427800A/P

A refresh operation must be performed once every 32 ms (128 ms for TMS427800AP) to retain data. The refresh operation can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. The hidden refresh operation is accomplished by holding $\overline{\text{CAS}}$ at V_{IL} after a read or write operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$-only refresh cycle. The external address is ignored, and the refresh address is generated internally.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR) refresh

CBR refresh is used by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and then holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored, and the refresh address is generated internally.

battery-backup refresh

TMS426800AP

A low-power battery-backup refresh mode that requires less than 350 µA refresh current is available on the TMS426800AP. Data integrity is maintained using CBR refresh with a period of 31.25 µs while holding $\overline{\text{RAS}}$ low for less than 300 ns. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} < 0.2$ V, $V_{IH} > V_{CC} - 0.2$ V).

TMS427800AP

A low-power battery-backup refresh mode that requires less than 350 µA refresh current is available on the TMS427800AP. Data integrity is maintained using CBR refresh with a period of 62.5 µs while holding $\overline{\text{RAS}}$ low for less than 300 ns. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} < 0.2$ V, $V_{IH} > V_{CC} - 0.2$ V).

self refresh (TMS42x800AP)

The self-refresh mode is entered by dropping $\overline{\text{CAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 µs. The chip is refreshed internally by an on-board oscillator. No external address is required because the CBR counter keeps track of the address. To exit the self-refresh mode, both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are brought high to satisfy t_{CHS} (hold time, $\overline{\text{CAS}}$ referenced to $\overline{\text{RAS}}$). Upon exiting self-refresh mode, a burst refresh (refresh of a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures that the DRAM is fully refreshed.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. The eight initialization cycles must include at least one refresh ($\overline{\text{RAS}}$-only or CBR) cycle.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}: TMS41x800A ..... – 1 V to 7 V
TMS42x800A, TMS42x800AP ..... – 0.5 V to 4.6 V
Voltage range on any pin (see Note 1): TMS41x800A ..... – 1 V to 7 V
TMS42x800A, TMS42x800AP ..... – 0.5 V to 4.6 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 55 C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS41x800A			TMS42x800A/P			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	3	3.3	3.6	V
V_{SS}	Supply voltage		0			0		V
V_{IH}	High-level input voltage	2.4		6.5	2		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	– 0.3		0.8	V
T_A	Operating free-air temperature	0		70	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TMS416800A

PARAMETER		TEST CONDITIONS†	'416800A-50		'416800A-60		'416800A-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{CAS}$ high, V_{CC} = 5.5 V, V_O = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		100		80		70	mA
I_{CC2}	Average standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		1		1		1	mA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		100		80		70	mA
I_{CC4}‡¶	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		80		70		60	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each page-mode cycle, t_{PC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

TMS417800A

PARAMETER		TEST CONDITIONS†	'417800A-50		'417800A-60		'417800A-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		130		110		100	mA
I_{CC2}	Average standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		1		1		1	mA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		130		110		100	mA
I_{CC4}‡¶	Average page current	V_{CC} = 5.5 V, t_{PC} = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		90		70		60	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each page-mode cycle, t_{PC}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

TMS426800A/P

PARAMETER		TEST CONDITIONS†		'426800A-50 '426800AP-50		'426800A-60 '426800AP-60		'426800A-70 '426800AP-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write- cycle current	V_{CC} = 3.6 V, Minimum cycle			90		70		60	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'426800A		2		2		2	mA
			'426800AP		1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'426800A		1		1		1	mA
			'426800AP		150		150		150	µA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			90		70		60	mA
I_{CC4}‡¶	Average page current	V_{CC} = 3.6 V, $\overline{RAS}$ low, t_{PC} = MIN, $\overline{CAS}$ cycling			80		60		50	mA
I_{CC6}#	Average self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			250		250		250	µA
I_{CC10}#	Average battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 31.25 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each page-mode cycle, t_{PC}
# For TMS426800AP only

electrical characteristics over recommended ranges of supply voltage and operating free-air conditions (unless otherwise noted) (continued)

TMS427800A/P

PARAMETER		TEST CONDITIONS†		'427800A-50 '427800AP-50		'427800A-60 '427800AP-60		'427800A-70 '427800AP-70		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 2 mA	LVTTL	2.4		2.4		2.4		V
		I_{OH} = – 100 µA	LVCMOS	V_{CC}–0.2		V_{CC}–0.2		V_{CC}–0.2		
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	LVTTL		0.4		0.4		0.4	V
		I_{OL} = 100 µA	LVCMOS		0.2		0.2		0.2	
I_I	Input current (leakage)	V_{CC} = 3.6 V, V_I = 0 V to 3.9 V, All others = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 3.6 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}‡§	Average read- or write- cycle current	V_{CC} = 3.6 V, Minimum cycle			120		100		90	mA
I_{CC2}	Average standby current	V_{IH} = 2 V (LVTTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'427800A		2		2		2	mA
			'427800AP		1		1		1	mA
		V_{IH} = V_{CC} – 0.2 V (LVCMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'427800A		1		1		1	mA
			'427800AP		150		150		150	µA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	V_{CC} = 3.6 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only refresh), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			120		100		90	mA
I_{CC4}‡¶	Average page current	V_{CC} = 3.6 V, $\overline{RAS}$ low, t_{PC} = MIN, $\overline{CAS}$ cycling			80		60		50	mA
I_{CC6}#	Average self-refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} min			200		200		200	µA
I_{CC10}#	Average battery back-up operating current (equivalent refresh time is 128 ms), CBR only	t_{RC} = 62.5 µs, t_{RAS} ≤ 300 ns, V_{CC} – 0.2 V ≤ V_{IH} ≤ 3.9 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and data stable			350		350		350	µA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change during each page-mode cycle, t_{PC}
# For TMS427800AP only

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11†		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance‡		7	pF

† A11 is NC (no internal connection) for TMS417800A and TMS427800A/P.
‡ $\overline{CAS}$ = V_{IH} to disable outputs
NOTE 3: V_{CC} = NOM supply voltage ± 10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER		'417800A-50		'417800A-60		'417800A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 5)		25		30		35	ns
t_{CAC}	Access time from $\overline{CAS}$ (see Note 5)		13		15		18	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (see Note 5)		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ (see Note 5)		50		60		70	ns
t_{OEA}	Access time from $\overline{OE}$ (see Note 5)		13		15		18	ns
t_{CLZ}	Delay time, $\overline{CAS}$ to output in the low-impedance state	0		0		0		ns
t_{OH}	Output data hold time from $\overline{CAS}$	3		3		3		ns
t_{OHO}	Output data hold time from $\overline{OE}$	3		3		3		ns
t_{OFF}	Output buffer turn-off delay from $\overline{CAS}$ (see Note 6)	0	13	0	15	0	18	ns
t_{OEZ}	Output buffer turn-off delay from $\overline{OE}$ (see Note 6)	0	13	0	15	0	18	ns

PARAMETER		'416800A-50 '42x800A/P-50		'416800A-60 '42x800A/P-60		'416800A-70 '42x800A/P-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address (see Note 5)		25		30		35	ns
t_{CAC}	Access time from $\overline{CAS}$ (see Note 5)		13		15		18	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (see Note 5)		30		35		40	ns
t_{RAC}	Access time from $\overline{RAS}$ (see Note 5)		50		60		70	ns
t_{OEA}	Access time from $\overline{OE}$ (see Note 5)		13		15		18	ns
t_{CLZ}	Delay time, $\overline{CAS}$ to output in the low-impedance state	0		0		0		ns
t_{OH}	Output data hold time from $\overline{CAS}$	3		3		3		ns
t_{OHO}	Output data hold time from $\overline{OE}$	3		3		3		ns
t_{OFF}	Output buffer turn-off delay from $\overline{CAS}$ (see Note 6)	0	13	0	15	0	18	ns
t_{OEZ}	Output buffer turn-off delay from $\overline{OE}$ (see Note 6)	0	13	0	15	0	18	ns

NOTES: 4. With ac parameters, it is assumed t_T = 5 ns.
5. For TMS42x800A/P, access times are measured with output reference levels of V_{OH} = 2 V and V_{OL} = 0.8 V.
6. t_{OFF} and t_{OEZ} are specified when the output is no longer driven. Data-in should not be driven until one of the maximum values is satisfied.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

		'417800A-50		'417800A-60		'417800A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read	90		110		130		ns
t_{WC}	Cycle time, write	90		110		130		ns
t_{RWC}	Cycle time, read-write	131		155		181		ns
t_{PC}	Cycle time, page-mode read or write (see Note 7)	35		40		45		ns
t_{PRWC}	Cycle time, page-mode read-write	76		85		96		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ active, page mode (see Note 8)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ active, nonpage mode (see Note 8)	50	10 000	60	10 000	70	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ active (see Note 9)	13	10 000	15	10 000	18	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ precharge	8		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ precharge	30		40		50		ns
t_{WP}	Pulse duration, write command	10		10		10		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data in (see Note 10)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{CAS}$ precharge	13		15		18		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$ precharge	13		15		18		ns
t_{WCS}	Setup time, write command before $\overline{CAS}$ active (early-write only)	0		0		0		ns
t_{CSR}	Setup time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)	5		5		5		ns
t_{WRP}	Setup time, write before $\overline{RAS}$ active (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address	10		10		15		ns
t_{DH}	Hold time, data in (see Note 10)	10		10		15		ns
t_{RAH}	Hold time, row address	8		10		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{CAS}$ (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}$ (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{CAS}$ active (early-write only)	10		10		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ active from $\overline{CAS}$ precharge	30		35		40		ns
t_{OEH}	Hold time, $\overline{OE}$ command	13		15		18		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{WRH}	Hold time, write after $\overline{RAS}$ active (CBR refresh only)	10		10		10		ns
t_{AWD}	Delay time, column address to write command (read-write operation only)	48		55		63		ns

NOTES: 4. With ac parameters, it is assumed t_T = 5 ns.
7. To ensure t_{PC} MIN, t_{ASC} should be ≥ to t_{CP}.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'417800A-50		'417800A-60		'417800A-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ precharge to $\overline{RAS}$	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ active to $\overline{CAS}$ precharge	50		60		70		ns
t_{CWD}	Delay time, $\overline{CAS}$ to write command (read-write operation only)	36		40		46		ns
t_{OED}	Delay time, $\overline{OE}$ to data in	13		15		18		ns
t_{RAD}	Delay time, $\overline{RAS}$ to column address (see Note 12)	13	25	15	30	15	35	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ precharge	25		30		35		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ precharge	25		30		35		ns
t_{RCD}	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (see Note 12)	18	37	20	45	20	52	ns
t_{RPC}	Delay time, $\overline{RAS}$ precharge to $\overline{CAS}$	5		5		5		ns
t_{RSH}	Delay time, $\overline{CAS}$ active to $\overline{RAS}$ precharge	13		15		18		ns
t_{RWD}	Delay time, $\overline{RAS}$ to write command (read-write operation only)	73		85		98		ns
t_{CPW}	Delay time, $\overline{CAS}$ precharge to write command (read-write only)	53		60		68		ns
t_{REF}	Refresh time interval		32		32		32	ms
t_T	Transition time	2	30	2	30	2	30	ns

NOTE 12: The maximum value is specified only to ensure access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

		'416800A-50 '42x800A/P-50		'416800A-60 '42x800A/P-60		'416800A-70 '42x800A/P-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read	90		110		130		ns
t_{WC}	Cycle time, write	90		110		130		ns
t_{RWC}	Cycle time, read-write	131		155		181		ns
t_{PC}	Cycle time, page-mode read or write (see Note 7)	35		40		45		ns
t_{PRWC}	Cycle time, page-mode read-write	76		85		96		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ active, page mode (see Note 8)	50	100 000	60	100 000	70	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ active, nonpage mode (see Note 8)	50	10 000	60	10 000	70	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ active (see Note 9)	13	10 000	15	10 000	18	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ precharge	8		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ precharge	30		40		50		ns
t_{WP}	Pulse duration, write command	10		10		10		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data in (see Note 10)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{WRP}	Setup time, write before $\overline{RAS}$ active (CBR refresh only)	10		10		10		ns
t_{CWL}	Setup time, write command before $\overline{CAS}$ precharge	13		15		18		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$ precharge	13		15		18		ns
t_{WCS}	Setup time, write command before $\overline{CAS}$ active (early-write only)	0		0		0		ns
t_{CSR}	Setup time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)	5		5		5		ns
t_{WRP}	Setup time, write before $\overline{RAS}$ active (CBR refresh only)	10		10		10		ns
t_{CAH}	Hold time, column address	10		10		15		ns
t_{DH}	Hold time, data in (see Note 10)	10		10		15		ns
t_{RAH}	Hold time, row address	8		10		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{CAS}$ (see Note 11)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}$ (see Note 11)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{CAS}$ active (early-write only)	10		10		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ active from $\overline{CAS}$ precharge	30		35		40		ns
t_{OEH}	Hold time, $\overline{OE}$ command	13		15		18		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns
t_{CHS}	Hold time, $\overline{CAS}$ referenced to $\overline{RAS}$ (self refresh only)	– 50		– 50		– 50		ns
t_{WRH}	Hold time, write after $\overline{RAS}$ active (CBR refresh only)	10		10		10		ns
t_{AWD}	Delay time, column address to write command (read-write operation only)	48		55		63		ns

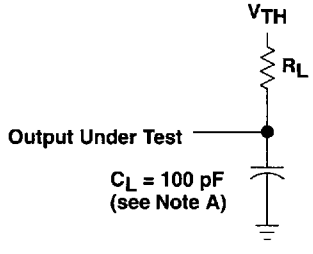
NOTES: 4. With ac parameters, it is assumed t_T = 5 ns.
7. To ensure t_{PC} MIN, t_{ASC} should be ≥ to t_{CP}.
8. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
9. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
10. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

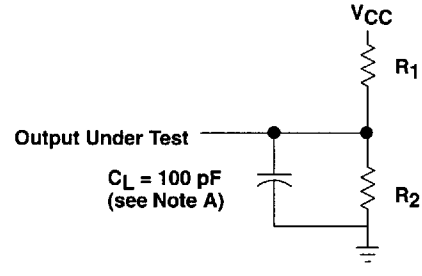
			'416800A-50 '42x800A/P-50		'416800A-60 '42x800A/P-60		'416800A-70 '42x800A/P-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ precharge to $\overline{RAS}$		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ active to $\overline{CAS}$ precharge		50		60		70		ns
t_{CWD}	Delay time, $\overline{CAS}$ to write command (read-write operation only)		36		40		46		ns
t_{OED}	Delay time, $\overline{OE}$ to data in		13		15		18		ns
t_{RAD}	Delay time, $\overline{RAS}$ to column address (see Note 12)		13	25	15	30	15	35	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ precharge		25		30		35		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ precharge		25		30		35		ns
t_{RCD}	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (see Note 12)		18	37	20	45	20	52	ns
t_{RPC}	Delay time, $\overline{RAS}$ precharge to $\overline{CAS}$		5		5		5		ns
t_{RSH}	Delay time, $\overline{CAS}$ active to $\overline{RAS}$ precharge		13		15		18		ns
t_{RWD}	Delay time, $\overline{RAS}$ to write command (read-write operation only)		73		85		98		ns
t_{CPW}	Delay time, $\overline{CAS}$ precharge to write command (read-write only)		53		60		68		ns
t_{RASS}	Pulse duration, $\overline{RAS}$ active, self refresh (see Note 13)		100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self refresh		90		110		130		ns
t_{REF}	Refresh time interval	'416800A		64		64		64	ms
		'426800A		64		64		64	ms
		'427800A		32		32		32	ms
		'42x800AP		128		128		128	ms
t_T	Transition time		2	30	2	30	2	30	ns

NOTES: 12. The maximum value is specified only to ensure access time.
13. During the period of 10 µs ≤ t_{RASS} ≤ 100 µs, the device is in a transition state from normal operation mode to self-refresh mode.

PARAMETER MEASUREMENT INFORMATION



(a) LOAD CIRCUIT



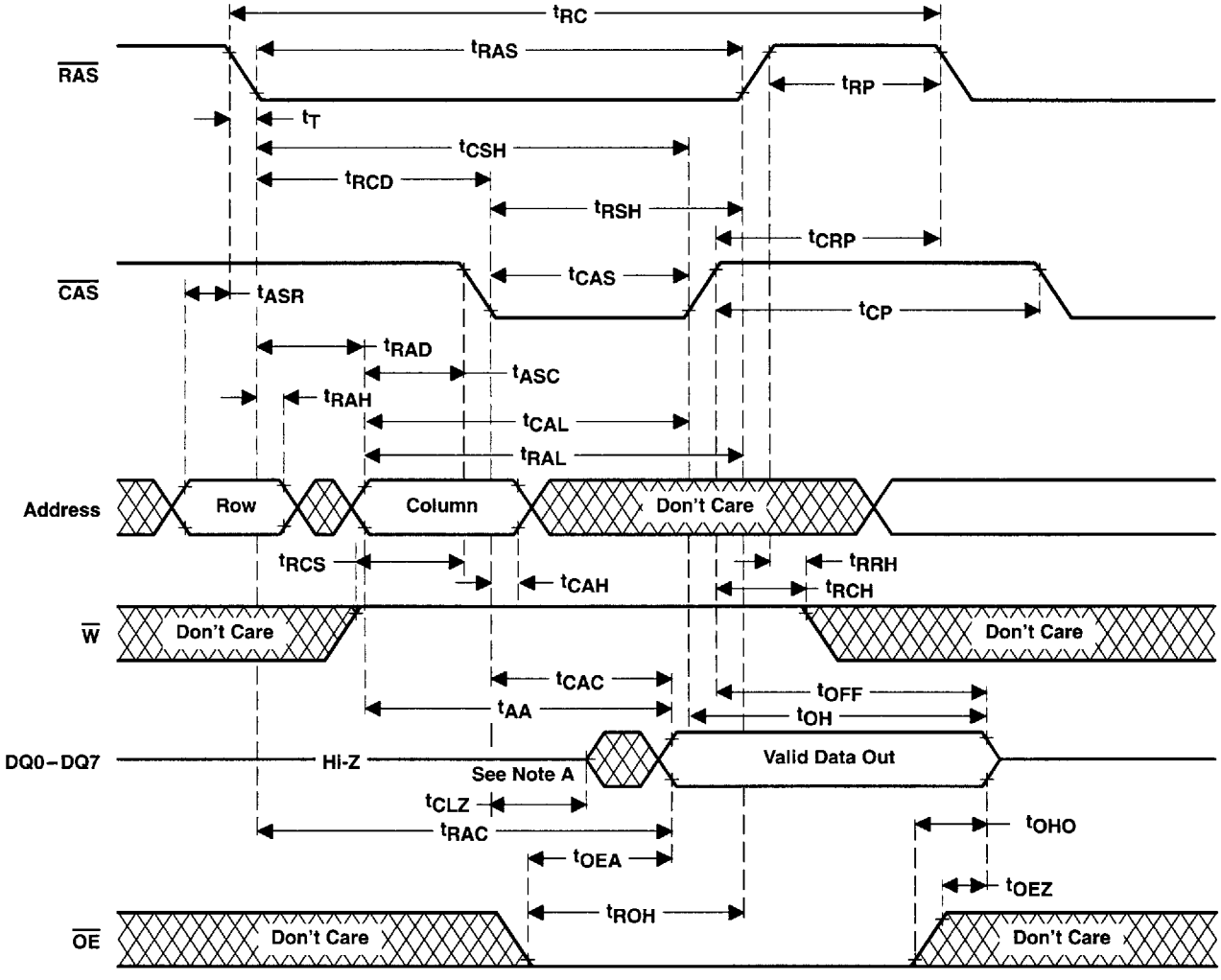
(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

DEVICE	V_{CC} (V)	R_1 (Ω)	R_2 (Ω)	V_{TH} (V)	R_L (Ω)
'41x800A	5	828	295	1.31	218
'42x800A/P	3.3	1178	868	1.4	500

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

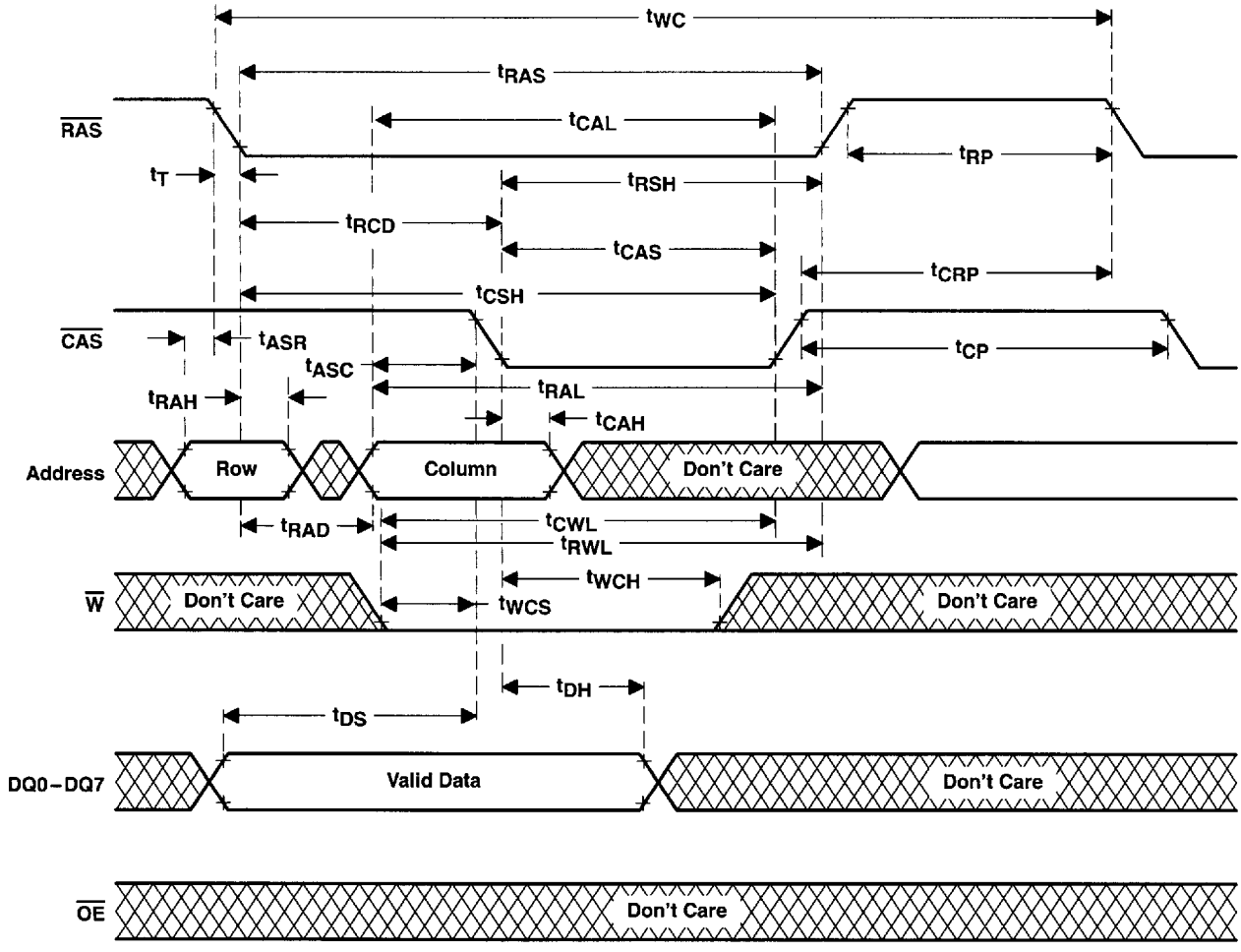


Figure 3. Early-Write-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

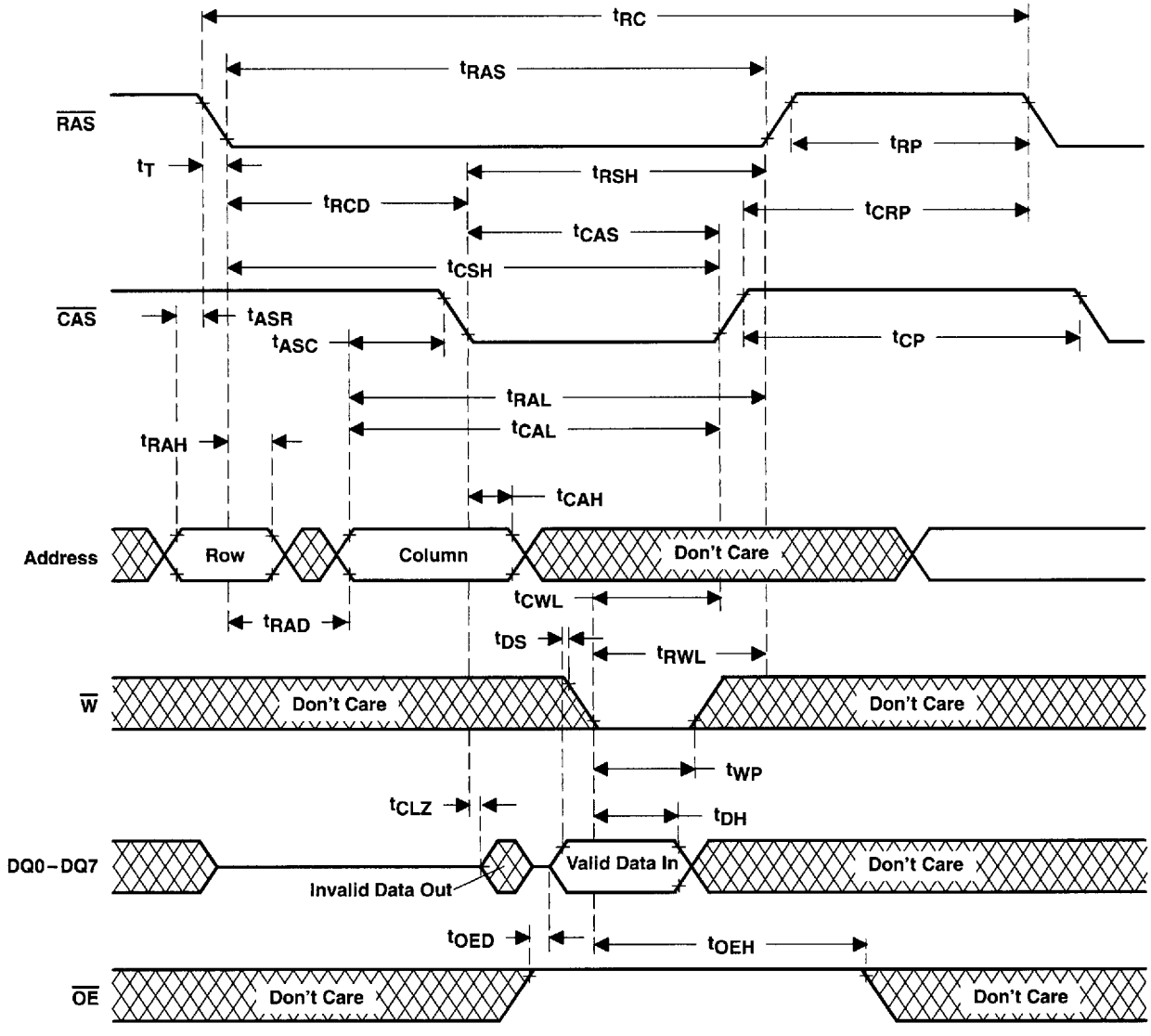
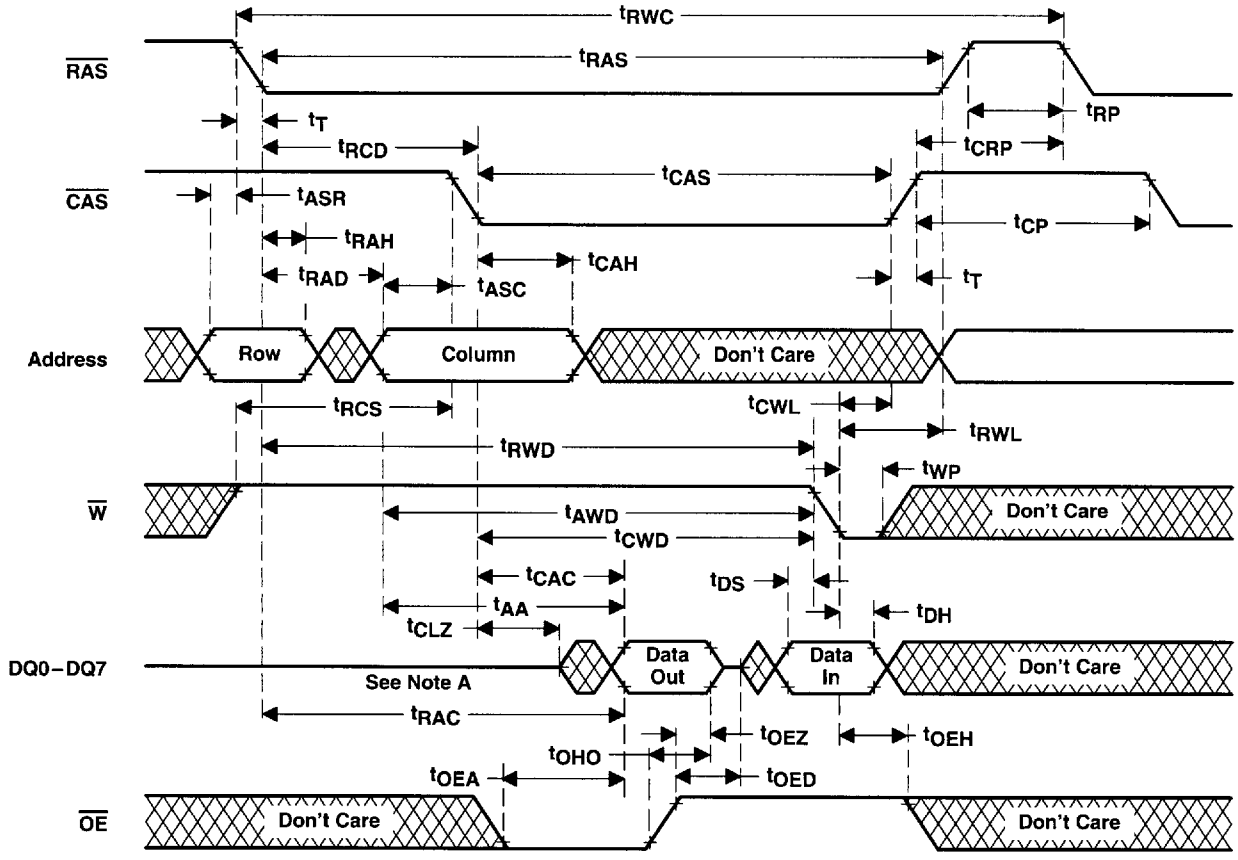


Figure 4. Write-Cycle Timing

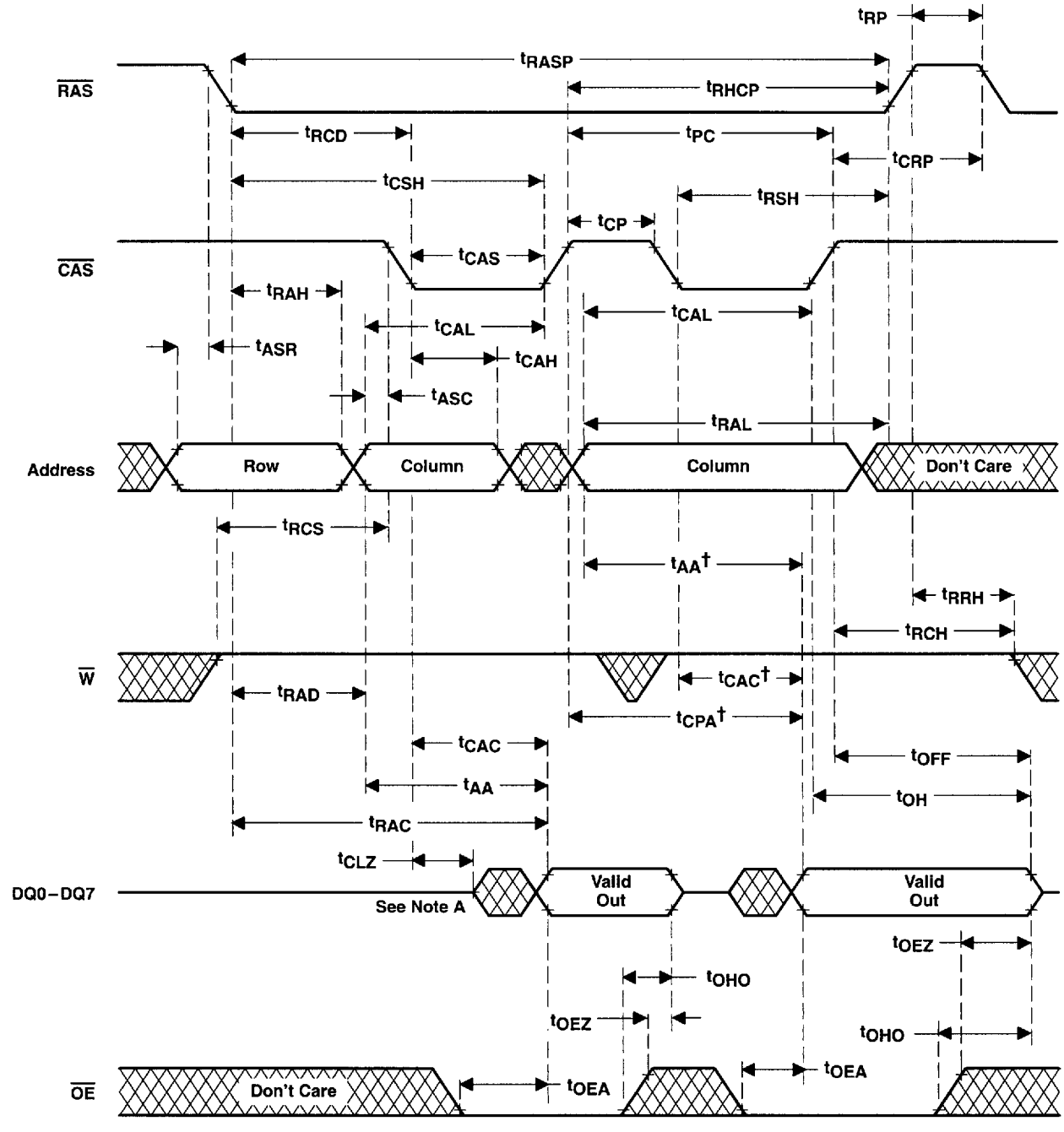
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-Cycle Timing

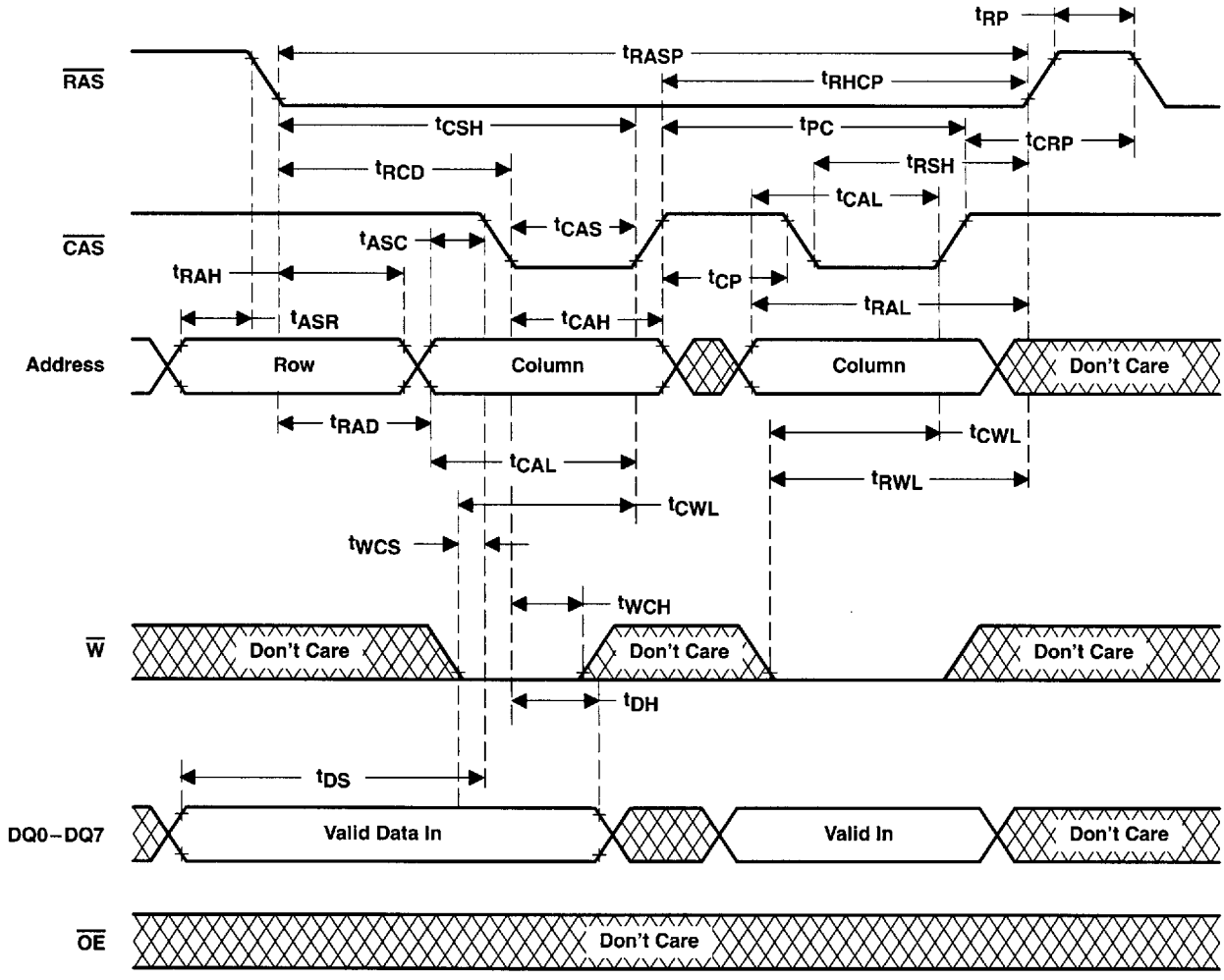
PARAMETER MEASUREMENT INFORMATION



† Access time is t_{CPA}-, t_{CAC}-, or t_{AA}-dependent.
NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

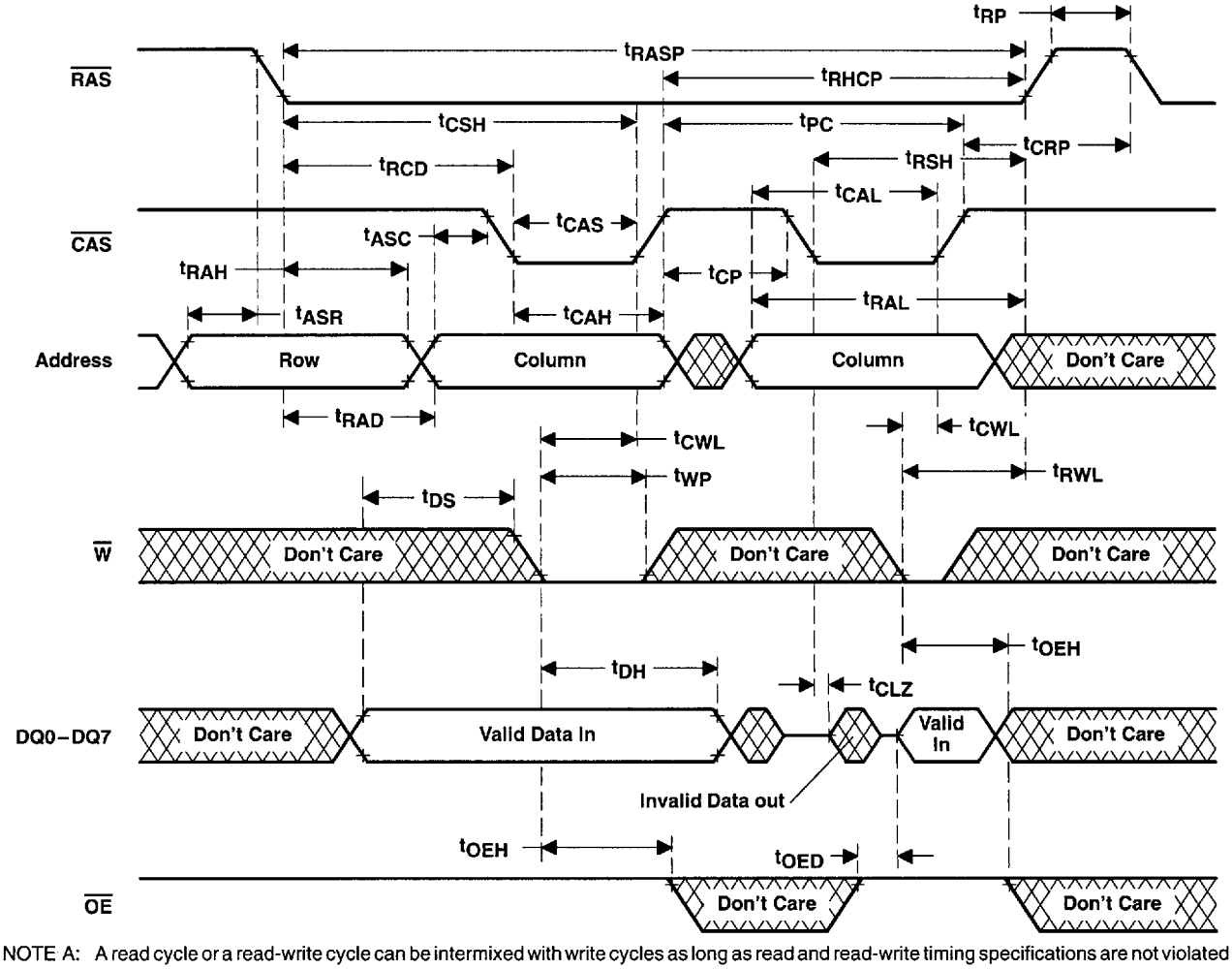
PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated

Figure 7. Enhanced-Page-Mode Early-Write-Cycle Timing

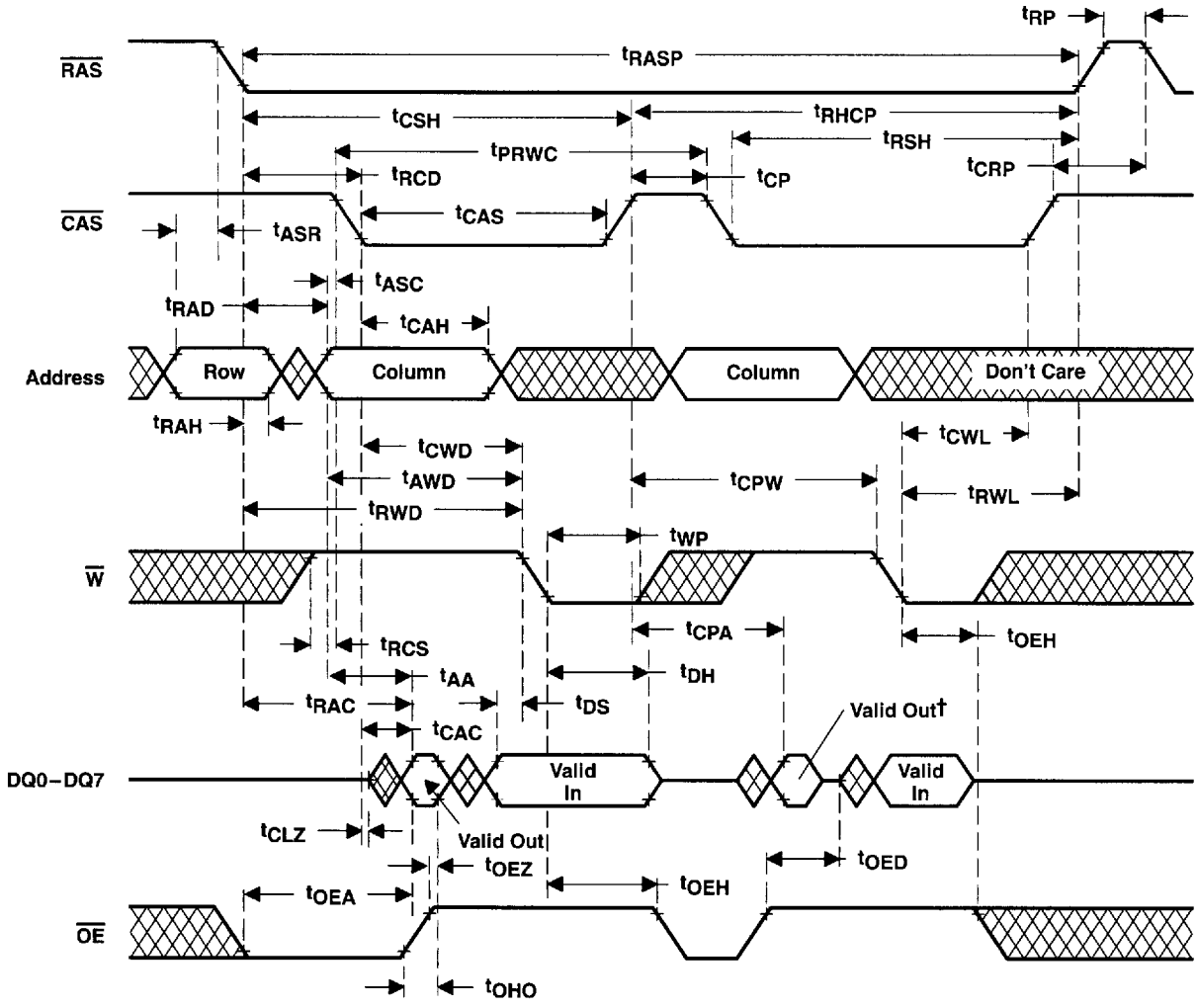
PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated

Figure 8. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
NOTE A: A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

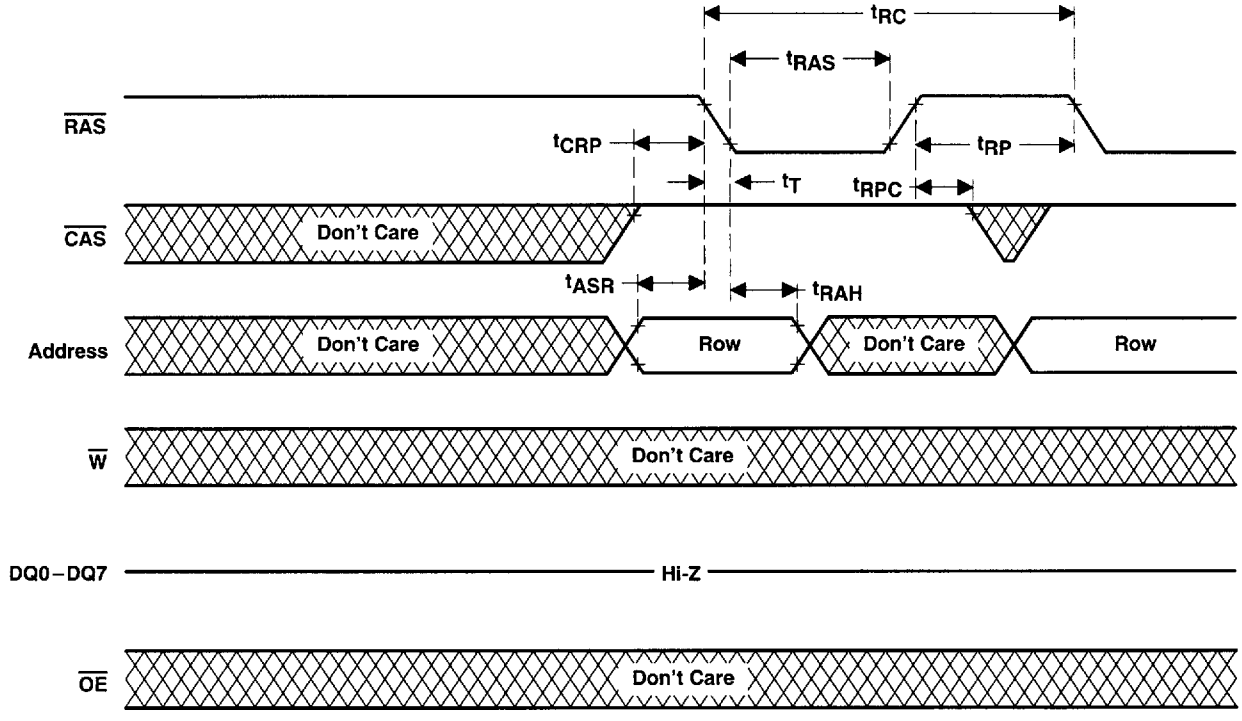


Figure 10. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

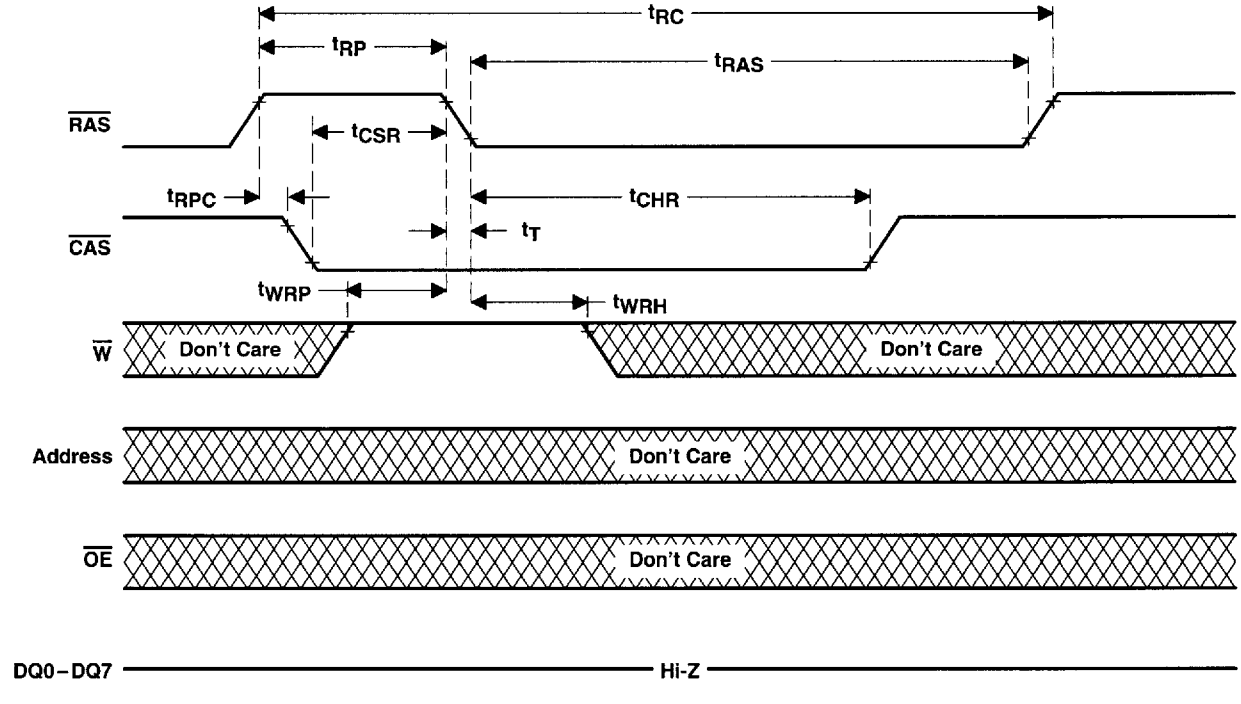


Figure 11. Automatic CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

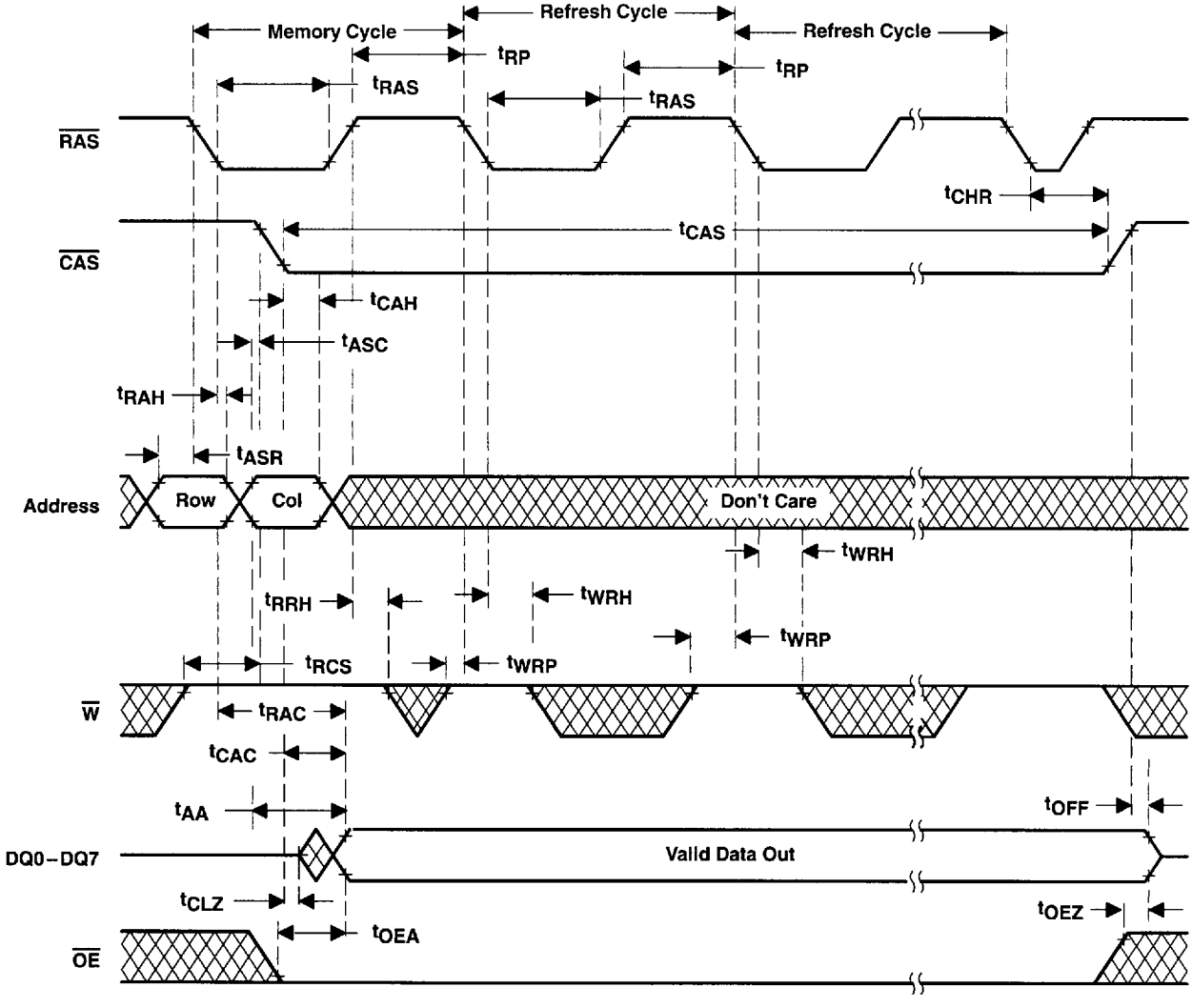


Figure 12. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

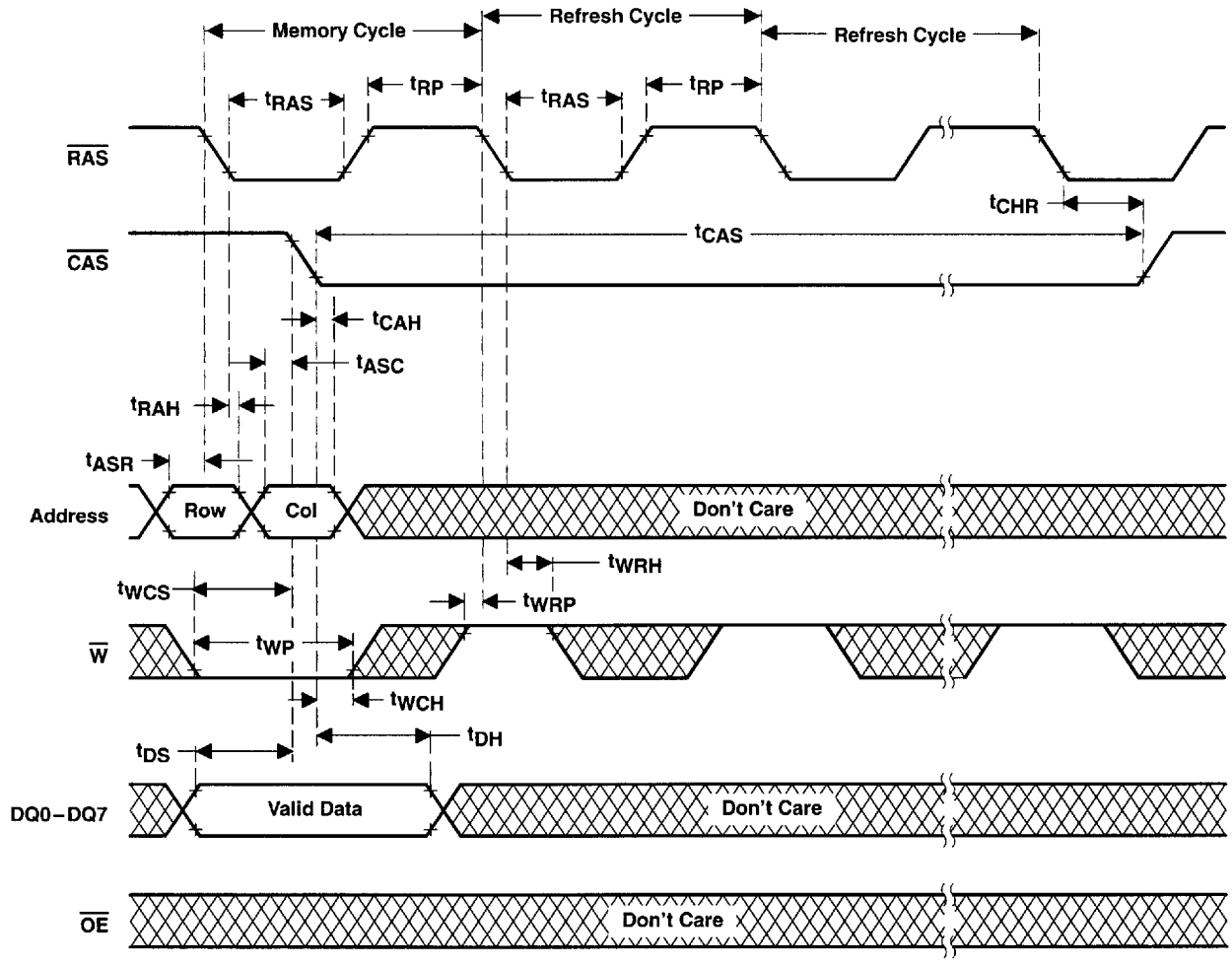


Figure 13. Hidden-Refresh-Cycle (Write) Timing

PARAMETER MEASUREMENT INFORMATION

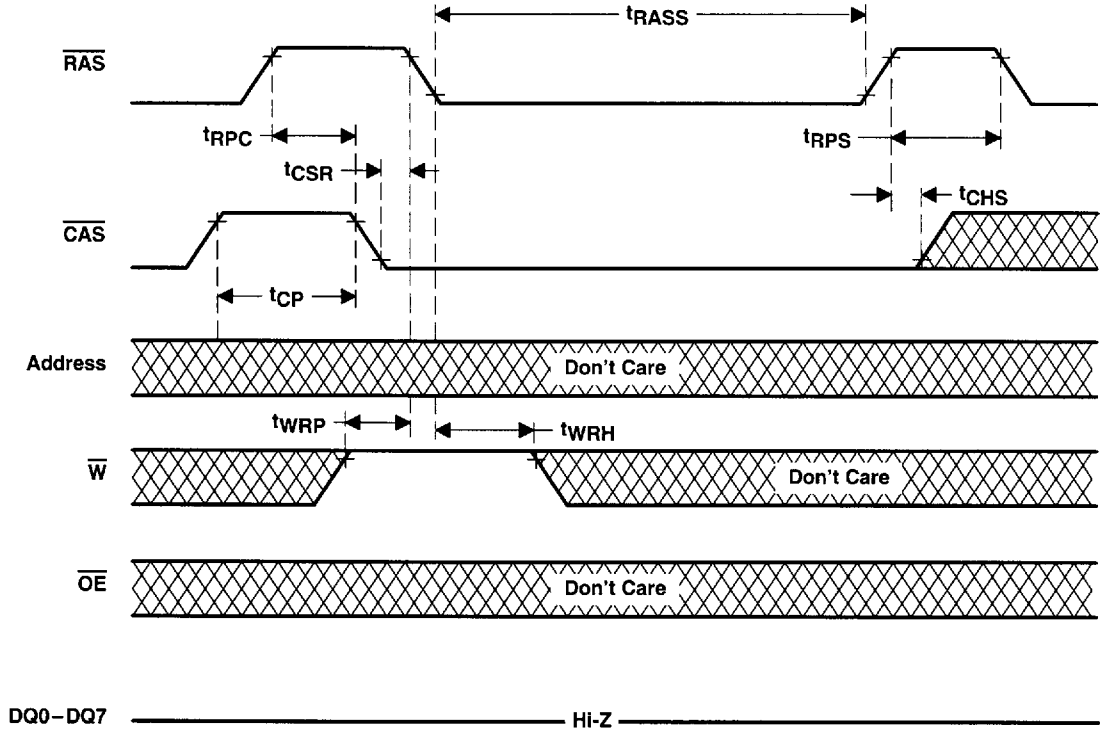
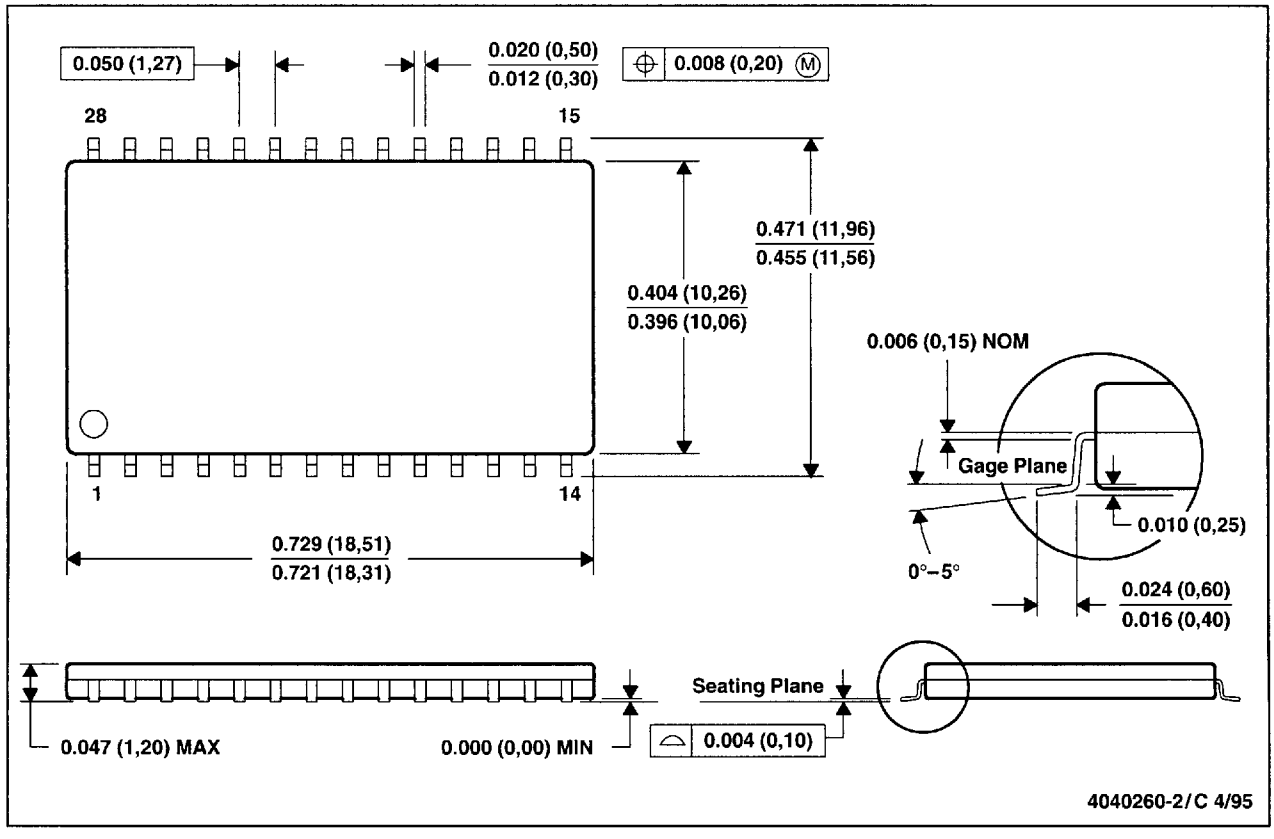


Figure 14. Self-Refresh-Cycle Timing

MECHANICAL DATA

DGC (R-PDSO-G28) **PLASTIC SMALL-OUTLINE PACKAGE**

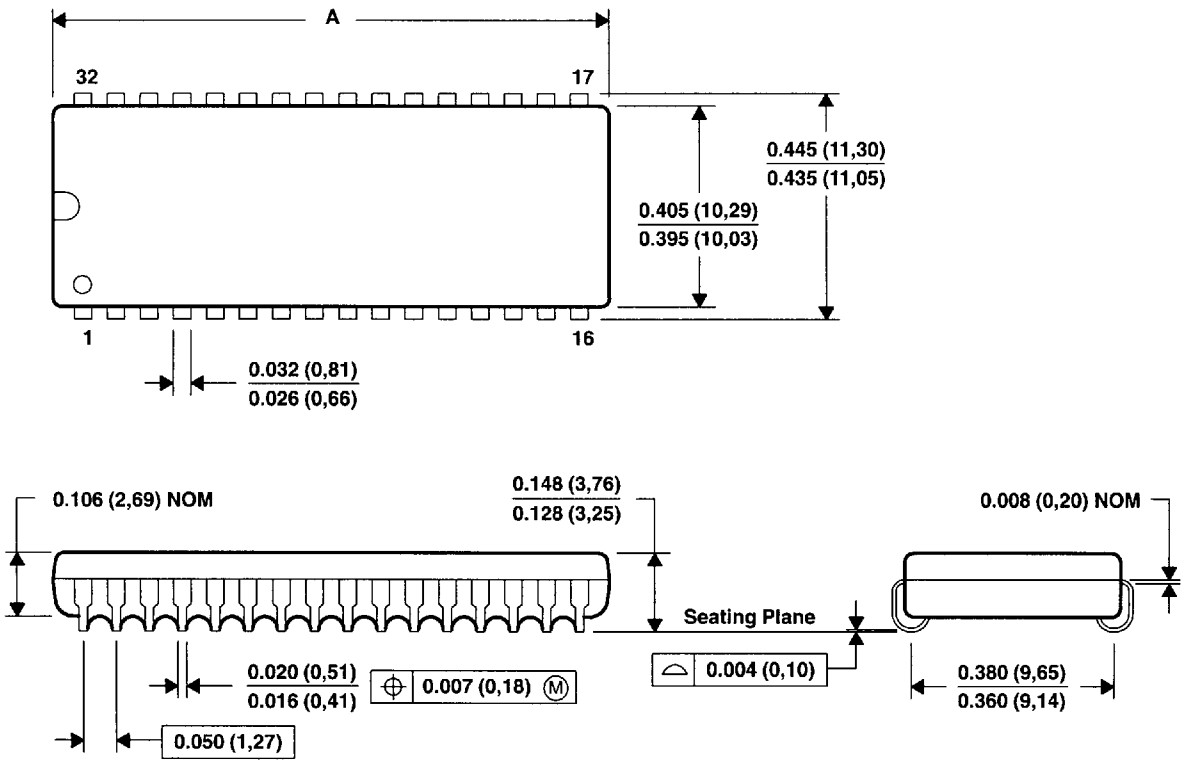


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL DATA

DZ (R-PDSO-J)** **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**

32 PIN SHOWN



DIM \ PINS **	24	28	32	40	42
A MAX	0.730 (18,54)	0.730 (18,54)	0.830 (21,08)	1.030 (26,16)	1.080 (27,43)
A MIN	0.720 (18,29)	0.720 (18,29)	0.820 (20,83)	1.020 (25,91)	1.070 (27,18)

4040094/C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,13).
D. The 24 pin package has the center two pins removed on both sides.

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device symbolization (TMS417800A illustrated)