REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

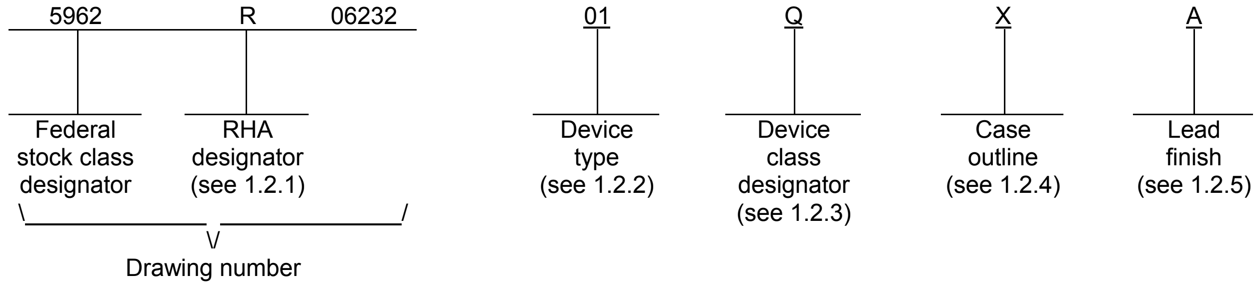
REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23											
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Charles F. Saffle	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Charles F. Saffle	
	APPROVED BY Thomas M. Hess	MICROCIRCUIT, DIGITAL, RADIATION HARDENED, SPACEWIRE PHYSICAL LAYER TRANSCEIVER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 06-07-06	
	REVISION LEVEL -	SIZE A | CAGE CODE **67268** | **5962-06232**
		SHEET 1 OF 23

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT200SpWPHY01	SpaceWire physical layer transceiver
02	UT200SpWPHY01	SpaceWire physical layer transceiver, extended industrial temperature range 1/

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1.	28	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Device type 02 has an extended industrial temperature range of -40°C to +125°C.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V dc to 4.0 V dc
Voltage on any pin during operation ($V_{I/O}$)	-0.3 V dc to (V_{DD} + 0.3 V)
Voltage on any pin during cold spare ($V_{I/O}$)	-0.3 V dc to 4.0 V dc
DC input current (I_I)	±10 mA
Maximum power dissipation (P_D)	120 mW
Thermal resistance, junction-to-case (θ_{JC})	10°C/W
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	3.0 V dc to 3.6 V dc
DC input voltage range (V_{IN})	0 V dc to V_{DD}

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	> 100 krads(Si)
Single event latchup (SEL)	> 110 MeV-cm^2/mg
Single event upset (SEU) saturated cross-section (σ_{sat})	2.9E-8 cm^2/device
Onset single event upset (SEU) linear energy threshold (LET), no upset	38 MeV-cm^2/mg
Neutron fluence	1 x 10^{14} neutrons/cm^2 2/
Dose rate upset	3/
Dose rate survivability	3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Guaranteed, but not tested.
3/ When characterized as a result of procuring activities request, the condition will be specified.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Functional block diagram. The functional block diagram shall be as specified on figure 4.

3.2.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as specified on figures 5 through 12.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 77 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions V_{DD} = 3.3 V ± 0.3 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
DC Electrical Characteristics 1/							
High-level input voltage (CMOS)	V_{IH}		1, 2, 3	All	2.0		V
Low-level input voltage (CMOS)	V_{IL}					0.8	V
Low-level output voltage (LVCMOS)	V_{OL}	I_{OL} = 12mA				0.4	V
High-level output voltage (LVCMOS)	V_{OH}	I_{OH} = -12mA			2.4		V
Input leakage current (LVCMOS)	I_{INCMOS}	$V_{IN} = V_{DD}$ or GND, V_{DD} = 3.6 V			-10	+10	µA
Input leakage current (LVDS)	I_{INLVDS}	$V_{IN} = V_{DD}$ or GND, V_{DD} = 3.6 V			-20	+20	µA
Cold spare leakage current (LVDS pins)	I_{CS}	V_{IN} = 3.6 V, $V_{DD} = V_{SS}$ = 0 V			-20	+20	µA
Differential input high threshold	V_{TH}	V_{CM} = +1.2 V				+100	mV
Differential input low threshold	V_{TL}	V_{CM} = +1.2 V			-100		mV
Differential output voltage	V_{OD}	R_L = 100Ω			250	400	mV
Change in magnitude of V_{OD} for complimentary output states	ΔV_{OD}	R_L = 100Ω				35	mV
Offset voltage	V_{OS}	RL = 100Ω, ($V_{OS} = (V_{OH} + V_{OL})/2$)			1.125	1.450	V
Change in magnitude of V_{OS} for complimentary output states	ΔV_{OS}	R_L = 100Ω				25	mV
LVDS output three-state current	I_{OZ}	TxOE = GND, V_{OUT} = 0 V or V_{DD}, V_{DD} = 3.6 V			-10	+10	µA
Loaded supply current, drivers enabled	I_{CCL}	R_L = 100Ω all channels, running in full duplex $V_{IN} = V_{DD}$ or V_{SS} (all inputs) C_L = 35 pF, f = 200 MHz				120	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{DD} = 3.3 V ± 0.3 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC Electrical Characteristics - Continued 1/							
Loaded supply current, drivers disabled	I_{CCZ}	D_{IN} = V_{DD} or V_{SS}, Clock and Data not toggling.	1, 2, 3	All		10	mA
Supply current, data toggling, clocks running, device and standby	I_{CCI}	Clock at 200 MHz, TxOE = 0 Data at 200 Mbits/sec, $\overline{RST}$ = 0				25	mA
LVCMOS input capacitance	C_{IN} 2/	f = 1 MHZ at 0 V	4			7	pF
LVCMOS output capacitance	C_{OUT} 2/	f = 1 MHZ at 0 V				15	pF
LVDS input capacitance	C_{INLVDS} 2/	f = 1 MHZ at 0 V				6	pF
LVDS output capacitance	$C_{OUTLVDS}$ 2/	f = 1 MHZ at 0 V				7	pF
Functional tests		See 4.4.1b	7, 8				
AC Switching Characteristics							
TxCLK to differential Data output low to high propagation delay	t_{CDLH}	R_L = 50Ω, C_L = 37 pF See figure 5.	9, 10, 11	All	2	4	ns
TxCLK to differential Data output high to low propagation delay	t_{CDHL}	R_L = 50Ω, C_L = 37 pF See figure 5.			2	4	ns
TxCLK to differential Strobe output low to high propagation delay	t_{CSLH}	R_L = 50Ω, C_L = 37 pF See figure 5.			2	4	ns
TxCLK to differential Strobe output high to low propagation delay	t_{CDHL}	R_L = 50Ω, C_L = 37 pF See figure 5.			2	4	ns
Differential channel skew	t_{DCS}					0.4	ns
Channel to channel skew	t_{CCS}					0.5	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{DD} = 3.3 V ± 0.3 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
AC Switching Characteristics - Continued							
Rise time LVDS driver	t_{TLH} 3/	R_L = 100Ω, C_L = 37 pF See figure 5.	9, 10, 11	All		1.5	ns
Fall time LVDS driver	t_{THL} 3/	R_L = 100Ω, C_L = 37 pF See figure 5.				1.5	ns
Output enable low to Data or Strobe high to Z	t_{OEHZ}	R_L = 50Ω, C_L = 37 pF See figures 6 and 7.				5	ns
Output enable low to Data or Strobe low to Z	t_{OELZ}	R_L = 50Ω, C_L = 37 pF See figures 6 and 7.				5	ns
Output enable high to Data or Strobe Z to high	t_{OEZH}	R_L = 50Ω, C_L = 37 pF See figures 6 and 7.				5	ns
Output enable high to Data or Strobe Z to low	t_{OEZL}	R_L = 50Ω, C_L = 37 pF See figures 6 and 7.				5	ns
Minimum required setup of Data or Strobe with respect to WrClk	$t_{SETUP\ TX}$	See figure 8.			2		ns
Minimum required hold of Data or Strobe with respect to WrClk	$t_{HOLD\ TX}$	See figure 8.			0		ns
Maximum rise time into Data/Strobe inputs	t_{INRISE} 4/	0.8 V to 2.0 V See figure 9.				14	% of bit width
Maximum fall time into Data/Strobe inputs	t_{INFALL} 4/	2.0 V to 0.8 V See figure 9.				14	% of bit width
Minimum number of full clock cycles (WrClk) between rising edge of RST and rising edge of first valid data or strobe (TxD0, TxD1, Tx20, TxS1)	t_{DRST}	See figure 10.			3		Wclk cycles
Minimum number of full clock cycles (WrClk) that RST must remain low before RST can transition high	t_{CRST}	See figure 10.			3		Wclk cycles
Delay between RxCLK falling and data edge	t_{CO}	See figure 11.				1	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{DD} = 3.3 V ± 0.3 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC Switching Characteristics - Continued							
Delay between $\overline{RST}$ going low and CMOS output three-state	t_{RLZ}	CL = 37 pF See figure 11.	9, 10, 11	All		5	ns
Delay between $\overline{RST}$ going high and CMOS output valid	t_{RLZ}	CL = 37 pF See figure 11.				5	ns
CMOS 20-80% receiver output rise time	t_{RISE}	CL = 37 pF See figure 9.				1	ns
CMOS 20-80% receiver output fall time	t_{FALL}	CL = 37 pF See figure 9.				1	ns
LVDS Rx input data to strobe separation	t_S 5/	See figure 12.			2.5		ns
Minimum Transmit clock period	$TxClk_{PMIN}$					5	ns
Minimum Write clock period	$WrClk_{PMIN}$					10	ns
Minimum high or low clock pulse width	t_{CPMIN}				2		ns

1/ Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.
2/ Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS} at a frequency of 1 MHz, and signal amplitude of 50 mV maximum.
3/ Guaranteed by characterization.
4/ Specified as a design guideline only, not tested.
5/ 2.5 ns of separation requires a R_{XOUT} Load of <= 10 pF.

TABLE IB. SEP test limits. 1/

Device type	SEP	T_C = temperature ±10°C	V_{DD}	Effective LET 2/
All	SEL	125	3.6 V	109 MeV-cm^2/mg
All	SEU	25	3.0 V	38 MeV-cm^2/mg

1/ For SEP conditions, see 4.4.4.4 herein.
2/ No SEL, no upset.

Case X

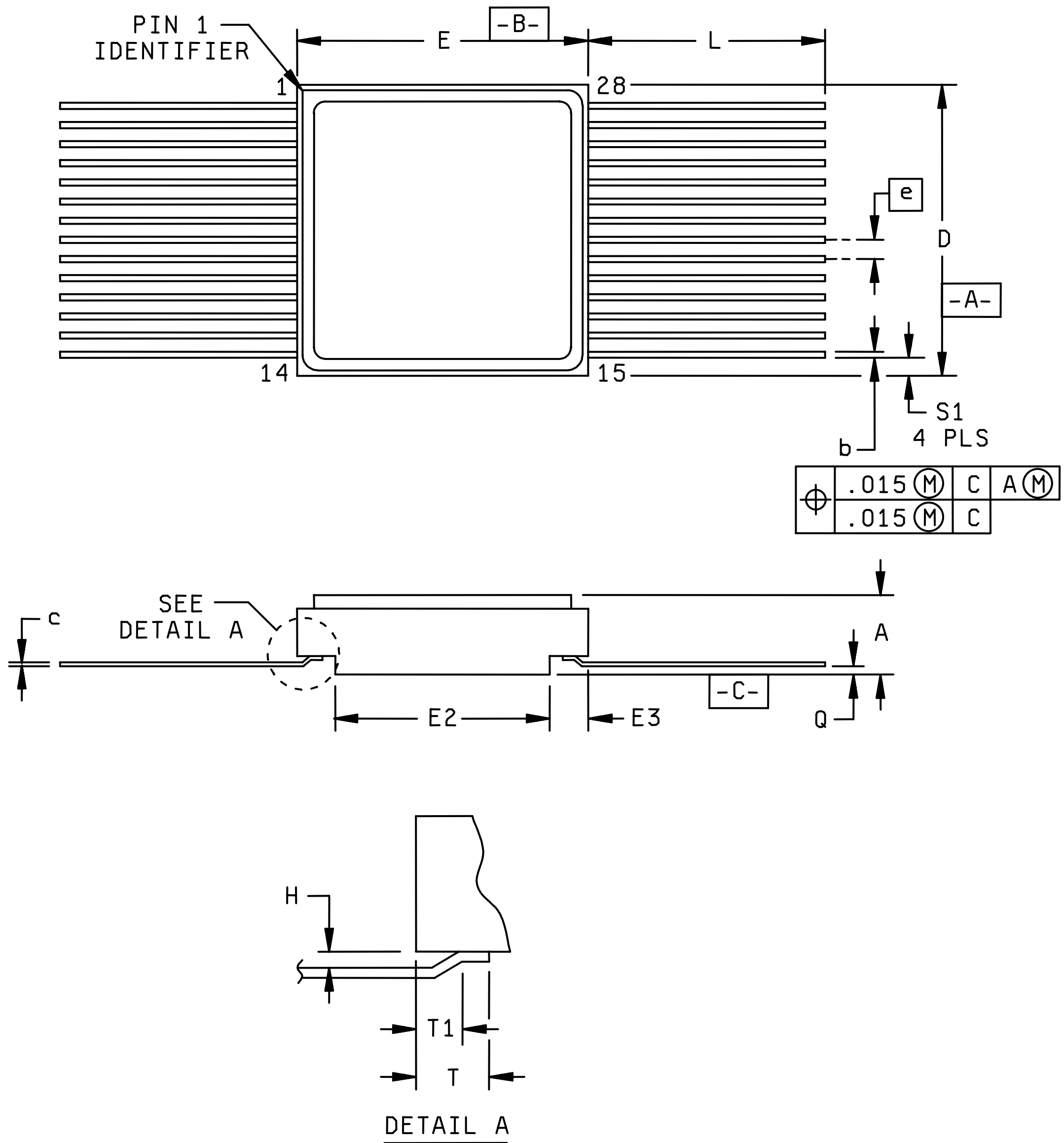


FIGURE 1. Case outline.

Case X

Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.093	0.115	2.36	2.92
b	0.006	0.010	0.15	0.25
c	0.004	0.007	0.10	0.18
D	0.375	0.385	9.52	9.78
E	0.375	0.385	9.52	9.78
E2	0.274	0.286	6.96	7.26
E3	0.030	---	0.76	---
e	0.025 BSC		0.64 BSC	
H	0.002	0.014	0.05	0.36
L	0.300	0.320	7.62	8.13
Q	0.011 NOM		0.28 NOM	
S1	0.005	---	0.13	---
T	0.033 NOM		0.84 NOM	
T1	0.018 NOM		0.46 NOM	

NOTES:

1. All exposed metallized areas are gold plated over electrically plated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbology is in accordance with MIL-PRF-38535.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option: no alphanumerics.
7. All linear dimensions are in inches (millimeters).

FIGURE 1. Case outline - Continued.

Device Type:	All		
Case Outline:	X		
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	LclLBE	15	TxD1
2	RmtLBE	16	TxD0
3	RxD+	17	TxS1
4	RxD-	18	TxS0
5	RxS+	19	WrClk
6	RxS-	20	TxClk
7	V_{DD}	21	GND
8	GND	22	V_{DD}
9	TxS+	23	$\overline{RST}$
10	TxS-	24	RxClk
11	TxD+	25	RxDF
12	TxD-	26	RxDR
13	TxOE	27	GND
14	GND	28	V_{DD}

FIGURE 2. Terminal connections.

Inputs				Outputs	
TxOE	$\overline{RST}$	LclLBE	RmtLBE	Tx Outputs	Rx Outputs
0	0	X	X	Hi-Z	Hi-Z
1	1	0	0	CMOS Tx Inputs	LVDS Rx Inputs
0	1	0	X	Hi-Z	LVDS Rx Inputs
0	1	1	X	Hi-Z	CMOS Tx Inputs
1	0	X	0	0	Hi-Z
1	0	X	1	LVDS Rx Inputs	Hi-Z
1	1	0	1	LVDS Rx Inputs	LVDS Rx Inputs
1	1	1	0	CMOS Tx Inputs	CMOS Tx Inputs
1	1	1	1	LVDS Rx Inputs	CMOS Tx Inputs

FIGURE 3. Truth table.

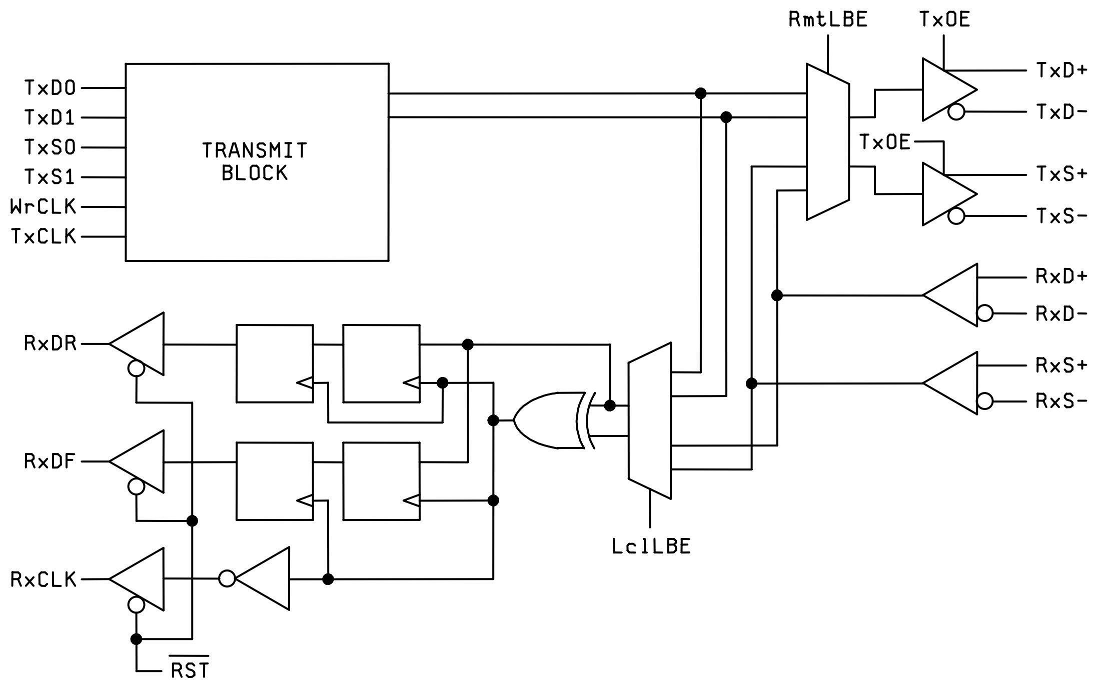
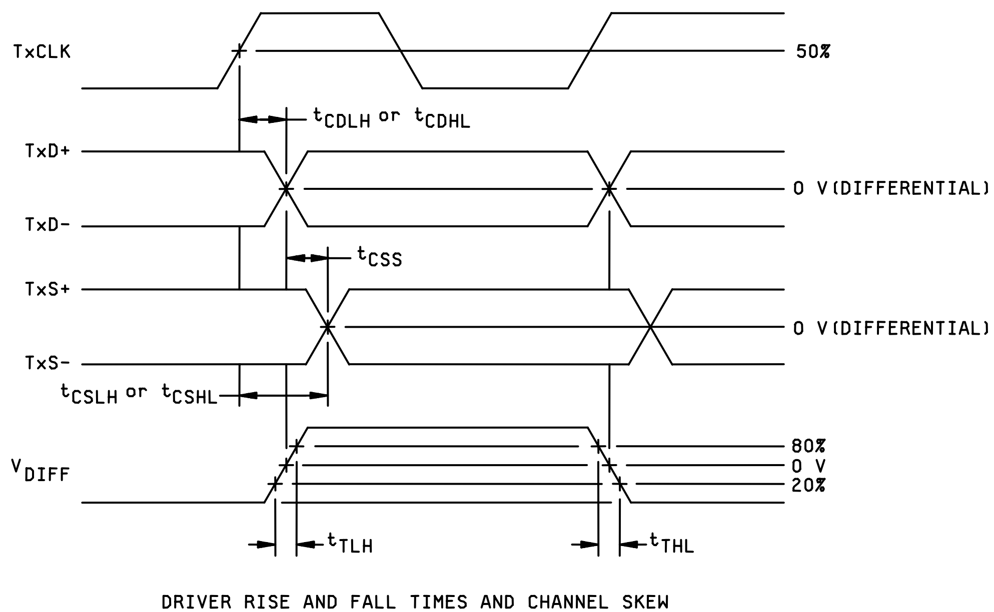


FIGURE 4. Functional block diagram.



NOTE: $V_{DIFF} = D_{OUT+} - D_{OUT-}$

FIGURE 5. Timing waveforms and test circuit.

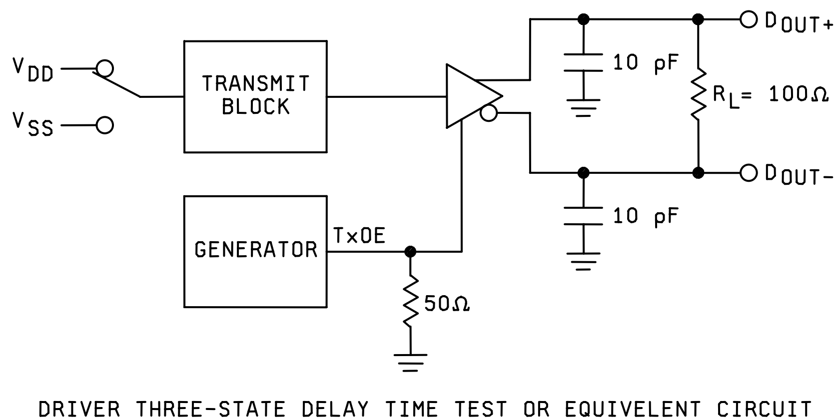


FIGURE 6. Timing waveforms and test circuit.

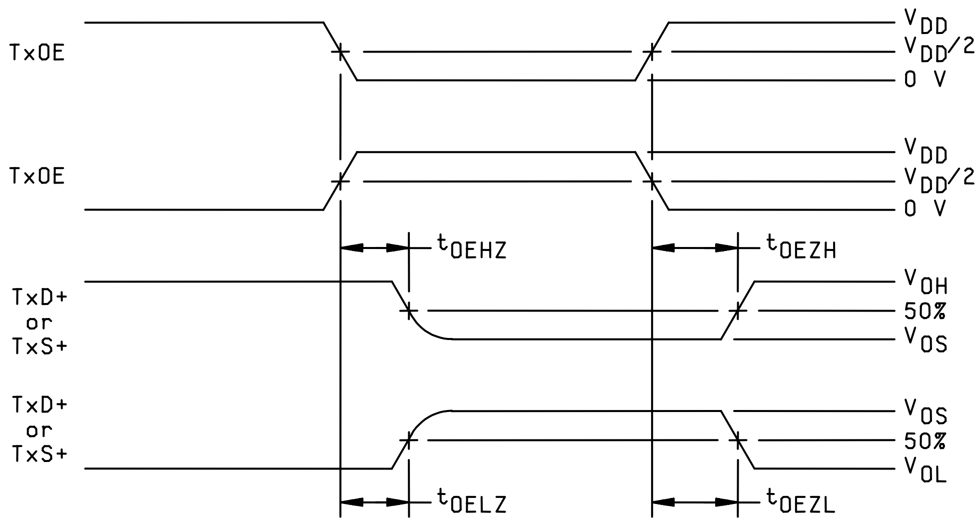


FIGURE 7. Timing waveforms and test circuit.

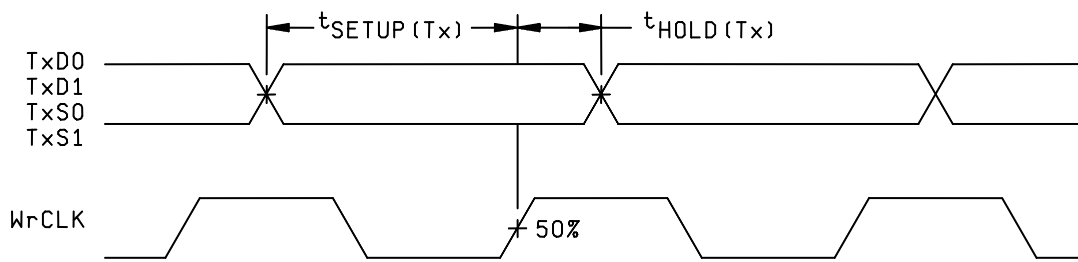


FIGURE 8. Timing waveforms and test circuit.

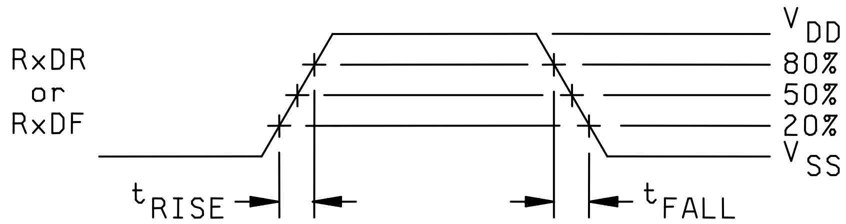


FIGURE 9. Timing waveforms and test circuit.

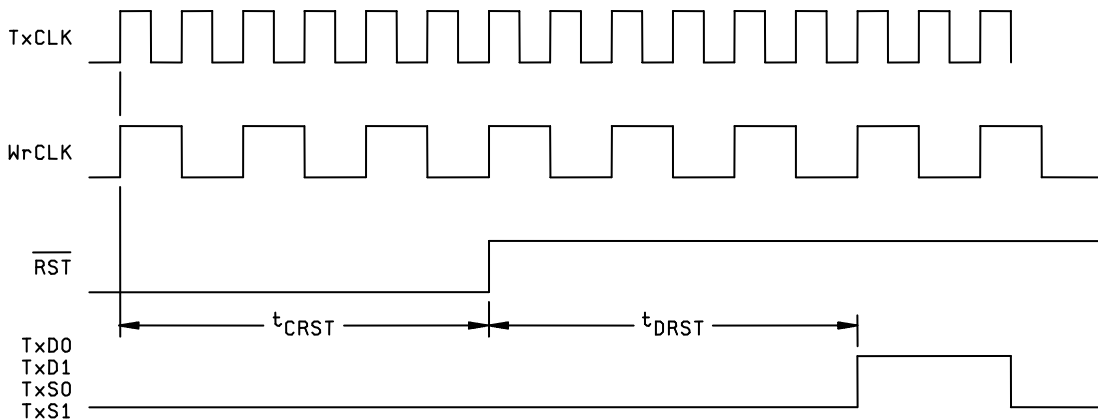


FIGURE 10. Timing waveforms and test circuit.

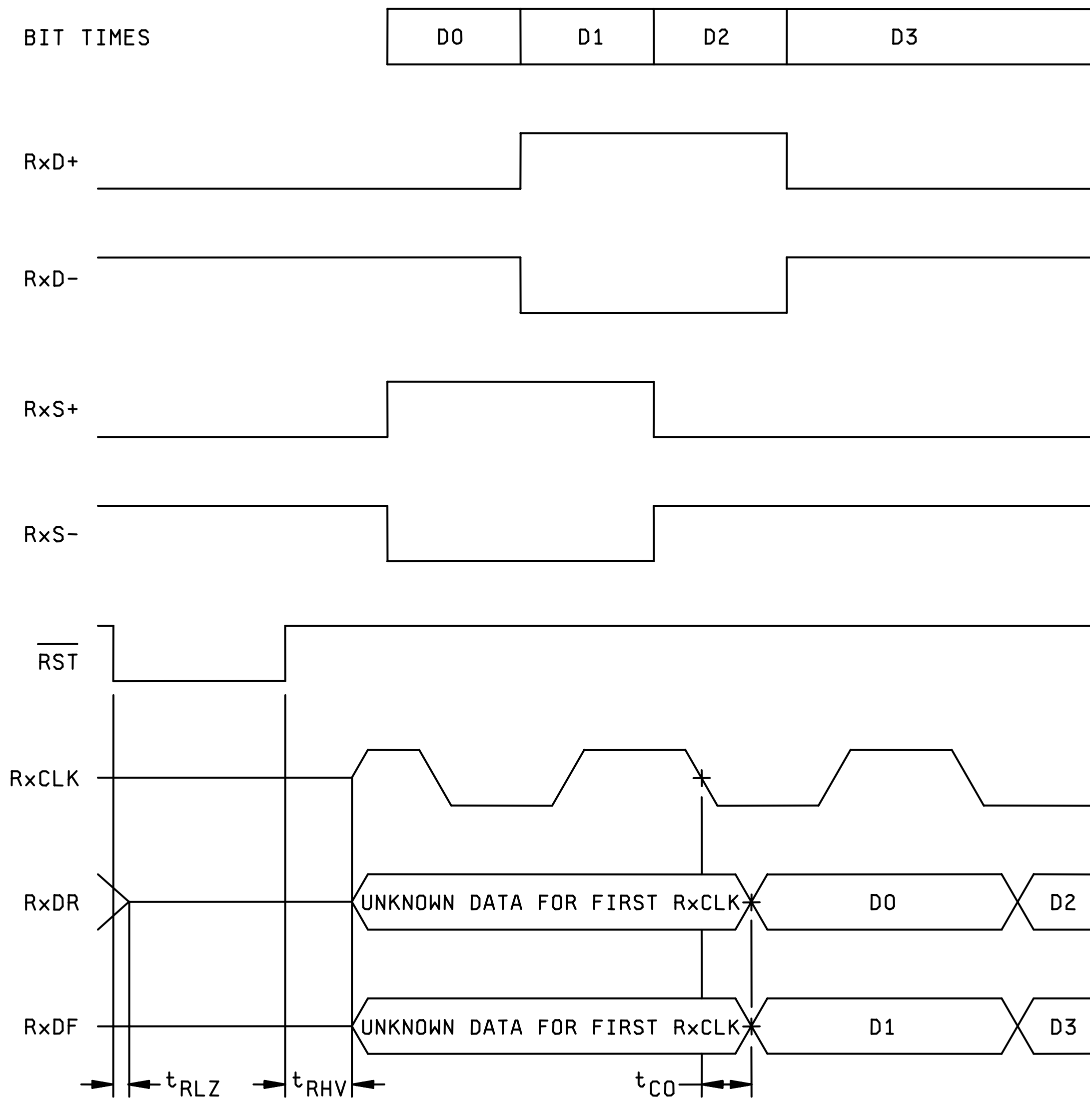


FIGURE 11. Timing waveforms and test circuit.

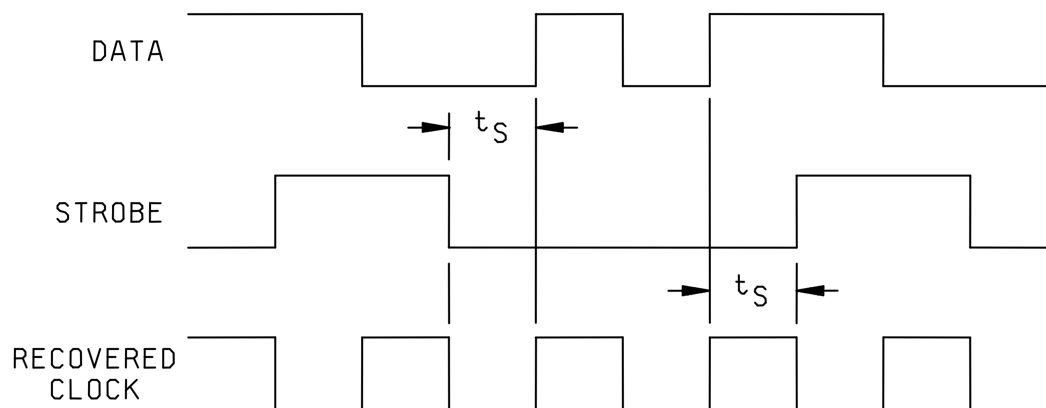


FIGURE 12. Timing waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 (C_{IN}, C_{OUT}, C_{INLVDS}, and $C_{OUTLVDS}$) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in table IIB herein, shall be required where specified, and the delta values shall be completed with reference to zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Test 1/	Symbol	Delta limits
Loaded supply current	I_{CCZ}	±10 % of measured value

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 (condition A) and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.5). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.5).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 11 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.5). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III as follows.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Terminal descriptions.

Terminal Name	Terminal Number	Terminal Type	Terminal Description
LclLBE	1	LVCMOS Input 1/	Local Loopback Enable 0: No loopback, received data comes from LVDS Rx inputs (RxD+, . . .). 1: Local loopback, received data comes from LVCMOS Tx inputs (TxD0, . . .).
RmtLBE	2	LVCMOS Input 1/	Remote Loopback Enable 0: No loopback, Transmit LVDS data comes from the LVCMOS Tx inputs (TxD0, . . .). 1: Remote loopback, Transmit LVDS data comes from LVDS Rx data.
RxD+	3	LVDS Input	LVDS Rx differential positive Data input.
RxD-	4	LVDS Input	LVDS Rx differential negative Data input.
RxS+	5	LVDS Input	LVDS Rx differential positive Strobe input.
RxS-	6	LVDS Input	LVDS Rx differential negative Strobe input.
V_{DD}	7, 22, 28		V_{DD} 3.3 V power supply.
GND	8, 14, 21, 27		V_{SS} 0 V
TxS+	9	LVDS Output	LVDS Tx differential positive Strobe output.
TxS-	10	LVDS Output	LVDS Tx differential negative Strobe output.
TxD+	11	LVDS Output	LVDS Tx differential positive Data output.
TxD-	12	LVDS Output	LVDS Tx differential negative Data output.
TxOE	13	LVCMOS Input 1/	TxOE = High: Enables LVDS transmit. TxOE = Low: Three-states LVDS transmit.
RxDR	26	LVCMOS Output	Receiver rising edge bit output.
RxDF	25	LVCMOS Output	Receiver falling edge bit output.
RxCLK	24	LVCMOS Output	Receiver clock output.
$\overline{RST}$	23	LVCMOS Input 1/	$\overline{RST}$ must remain low for 3 clock cycles before transitioning high, and must transition high 3 clock cycles before valid data.
TxCLK	20	LVCMOS Input 1/	Clock input to transmitter used to clock LVDS output. Any phase relationship is allowed between TxCLK and WrCLK but both must come from the same clock source and TxCLK must be twice the frequency of the WrCLK.
WrCLK	19	LVCMOS Input 1/	Transmitter input data Clock used to clock CMOS input to transmitter. Any phase relationship is allowed between TxCLK and WrCLK but both must come from the same clock source and WrCLK must be 1/2 of TxCLK.
TxS0	18	LVCMOS Input	First bit of 2-bit parallel strobe input to transmitter.
TxS1	17	LVCMOS Input	Second bit of 2-bit parallel strobe input to transmitter.
TxD0	16	LVCMOS Input	First bit of 2-bit parallel data input to transmitter.
TxD1	15	LVCMOS Input	Second bit of 2-bit parallel data input to transmitter.

1/ LVTTL compatible.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-07-06

Approved sources of supply for SMD 5962-06232 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R0623201QXA	65342	UT200SpWXCA
5962R0623201QXC	65342	UT200SpWXCC
5962R0623201VXA	65342	UT200SpWXCA
5962R0623201VXC	65342	UT200SpWXCC
5962R0623202QXA	65342	UT200SpWXWA
5962R0623202QXC	65342	UT200SpWXWC
5962R0623202VXA	65342	UT200SpWXWA
5962R0623202VXC	65342	UT200SpWXWC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.