Data Sheet
VSC850

1.6 Gb/s 16X32 Crosspoint Switch

Features

- 1.6 Gb/s Operation
- Non-blocking Architecture
- Duty-cycle Distortion: ≤ 100 pS
- ≤ 1.8 nS Propagation Delay for Data Path
- ≤ 200 pS Output to Output Skew in Broadcast Mode
- Power Supply: -2 V and 3.3 V
- ECL Differential Data Paths
- 3.3 V TTL Control Signals
- Low Power Dissipation
- Package: 208-pin PQFP

General Description

This VSC850 is a 16 x 32 crosspoint switch intended for high speed digital data communications applications. This product has 16 data inputs and 32 data outputs. Any input can be multiplexed to any, some, or all outputs. High speed digital data up to 1.25 Gb/s can be switched with less than 100 pS pulse width distortion. In broadcast mode, any two outputs will exhibit less than 200 pS of skew relative to one another. Signals in data paths are fully differential to minimize duty cycle distortion. The VSC850 requires both -2V and 3.3V power supplies.

The address signals that control traffic patterns for data paths are double buffered. *LSTROBE* signals load individual addresses for each output. A G*STROBE* signal is used to update addresses for all 32 outputs simultaneously. This method allows users to configure any, some or all switches independently without disrupting data flow of the data paths. A *CONFMODE* signal is provided to allow configuring the array either as a single 16 x 32 matrix or as two parallel 16 x 16 matrix's. Broadcast and flow through functionality are controlled via *BROADCAST* and *FLOWTHRU* inputs.

This product is ideal for high speed digital applications including data distribution for telecommunications, fiber channel networking, computer networking, multiprocessor switching, and test equipment. In a telecommunications SONET application, for example, the VSC850 can be used as an STS-12 protection switch.

The VSC850 is packaged in a 208 pin thermally enhanced PQFP package. This product is fabricated using Vitesse's E/D GaAs MESFET process which achieves high speed coupled with low power dissipation.

Functional Description

The VSC850 may be used to connect any one of 16 inputs to any one or combination of 32 output channels, according to a user defined bit pattern stored in each output channel's control latches (see Figure 1). For data path operation, signals flow transparently from inputs *I+/I-[0:15]* to output channels *Z+/Z-[0:31]* through thirty-two 16:1 multiplexers. The traffic pattern is controlled by data previously stored in thirty-two 4-bit control latches each corresponding to an output channel. Value of these 4-bit control latches is a binary numerical representation of the input channel selected (i.e., 0000 corresponds to *I[0]*, 0001 corresponds to *I[1]*, etc.).

Traffic information stored in control latches can be configured in either Single or Double Configuration mode by controlling *CONFMODE* input (see Table 1). If *CONFMODE* is high, the switch is configured in Single Configuration mode. In this mode, output addresses *A[4:0]* select one out of 32 banks of 4-bit holding registers. At rising edge of *LSTROBE[0]*, this bank of registers is updated by input addresses *D[3:0]* which describes a new path for that channel. The coding for these addresses is a binary numerical representation. *D[3:0]* = 0000 corresponds to *I[0]*, 0001 corresponds to *I[1]*, etc. Similarly, *A[4:0]* = 00000 selects path to output *Z[0]*, 00001 to *Z[1]*, etc. In this mode, values at *LSTROBE[1]*, *A[7:5]* and *D[7:4]* inputs are ignored. In Double Configura-

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tion mode, (*CONFMODE*=low), the switch matrix is divided into two 16x16 matrixes. Each of these two matrixes are configured independently with a set of 4 input addresses and 4 output addresses. Holding registers controlling paths to *Z+/Z-[0:15]* are selected with *A[3:0]* and updated by *D[3:0]* at the rising edge of *LSTROBE[0]*. Holding registers controlling paths to *Z+/Z-[16:31]* are selected with *A[7:4]* and updated by *D[7:4]* at the rising edge of *LSTROBE[1]*. Also, the coding of these addresses is binary numerical. In both methods, after some or all holding registers are programmed, a high pulse is applied to *GSTROBE* to transfer the information from holding registers into all control latches. By this method, the entire crosspoint switch can be reconfigured simultaneously.

The VSC850 can be configured in Broadcast Single Configuration mode or Broadcast Double Configuration mode. In Broadcast Single Configuration Mode, at the rising edge of *LSTROBE[0]*, all holding registers are updated by input addresses *D[3:0]*. In Broadcast Double Configuration Mode, holding registers controlling outputs *Z+/Z-[0:15]* are updated by *D[3:0]* at rising edge of *LSTROBE[0]*. Holding registers controlling *Z+/Z-[0:31]* are updated by *D[7:4]* at rising edge of *LSTROBE[1]*. If a high pulse is applied to *GSTROBE*, the entire crosspoint is configured and the selected data are broadcasted to all of the outputs. The output address values at *A[7:0]* are ignored in Broadcast Mode.

In FlowThru Single Configuration mode, at the rising edge of *LSTROBE[0]*, all holding registers are set to the numerical representation of the output which they control, (i.e., 0000 is loaded for output *Z[0]*& *Z[16]*, 0001 is loaded for output *Z[1]* & Z[17], etc.). The only difference in FlowThru Double Configuration mode is that the values of holding registers *Z+/Z-[0:15]* are updated by *LSTROBE[0]* and registers controlling outputs *Z+/Z-[16:31]* are updated by rising edge of *LSTROBE[1]*. If a high pulse is then applied to *GSTROBE*, these values are passed to the control latches. In this mode, data from *I[0]* is switched to *Z[0]* and *Z[16]*, data from *I[1]* is switched to *Z[1]* & *Z[17]*, etc. The input address values at *D[7:0]* and the output address values at *A[7:0]* are ignored in FlowThru Mode. All data input and output signals (*I+/I-[0:15]*, *Z+/Z-[0:31]*) are differential ECL levels. All other signals are TTL levels.

Table 1: Truth Table

BROADCAST	*FLOWTHRU*	*CONFMODE*	*MODES*
0	0	1	Single Configuration Mode
0	0	0	Double Configuration Mode
1	0	1	Broadcast Single Configuration Mode
1	0	0	Broadcast Double Configuration Mode
x	1	1	FlowThru Single Configuration Mode
x	1	0	FlowThru Double Configuration Mode

Note: *CONFMODE* signal asynchronously switches the two *LSTROBE* clocks during configuration process. In order to prevent glitching, values of the two *LSTROBE* clocks have to be the same at the time the *CONFMODE* signal changes states or the content of the holding registers during this period are not guaranteed

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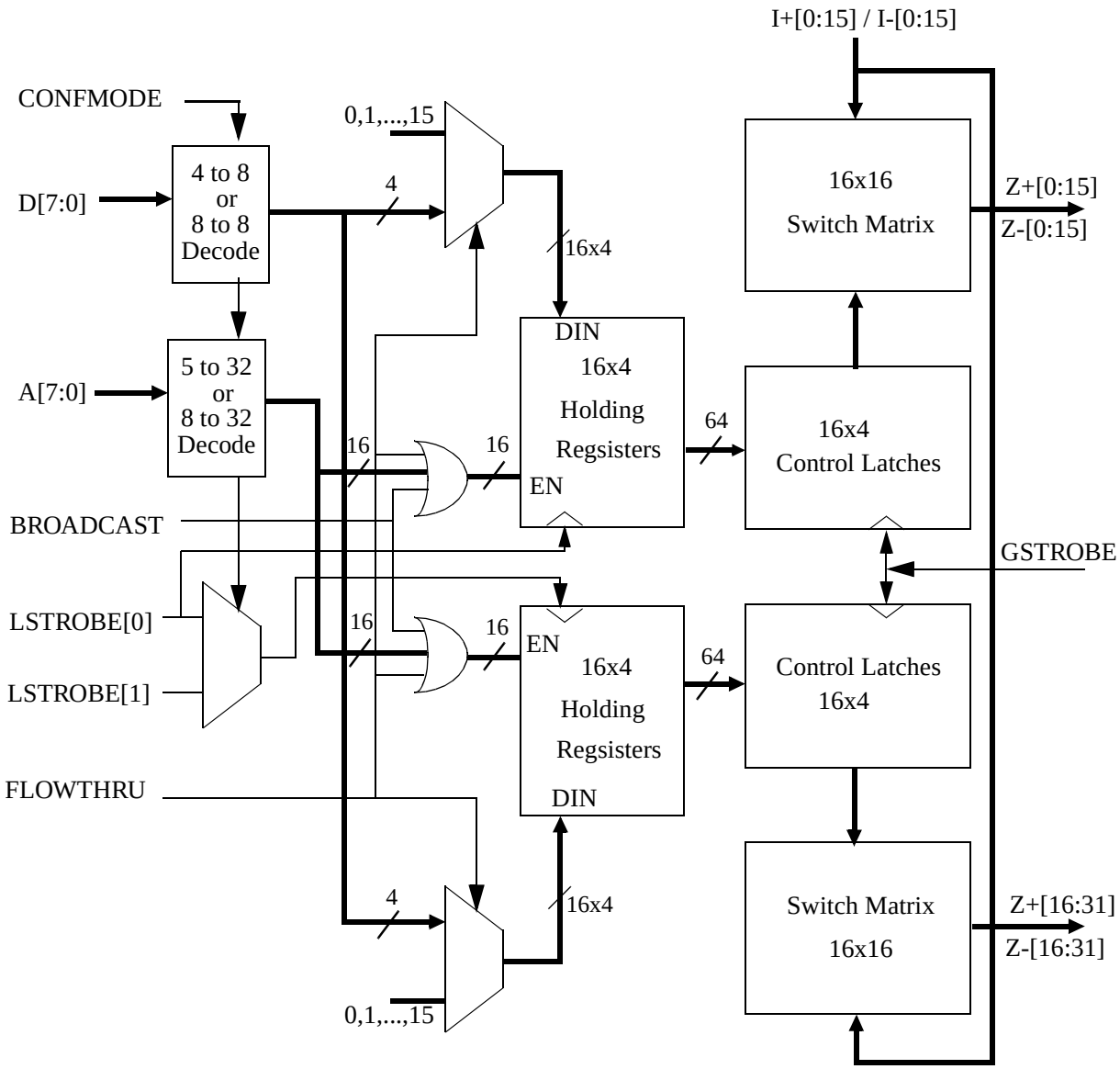
Figure 1: VSC850 Block Diagram



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Absolute Maximum Ratings (1)

ECL Power Supply Voltage , V_{TT} potential to GND ..... -2.5V to +0.5V
TTL Power Supply Voltage , V_{TTL} potential to GND ..... -0.5V to +4.3V
ECL input Voltage Applied, V_{ECLIN} ..... V_{TT}-0.5V to +0.5V
TTL input Voltage Applied, V_{TTLIN} ..... -0.5V to V_{TTL}+1.0V
Output Current, I_{OUT},(DC, output HI) ..... 50 mA
Case Temperature Under Bias, TC. ..... -55° to +125°C
Storage Temperature (ambient), TSTG. ..... -65°C to +150°C

Recommended Operating Conditions

ECL Supply Voltage, V_{TT}. ..... -2.0V ± 5%
TTL Supply Voltage, V_{TTL}. ..... 3.3V ± 5%
Commercial Operating Temperature Range, T(2). ..... 0° to 70°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) Lower limit of specification is ambient temperature and upper limit is case temperature.

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DC Characteristics *(Over recommended operating conditions. ECLOutput load 50Ω to V_{TT}.)*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{ODIF}	Differential ECL Output Voltage	600	—	1100	mV	50Ω to V_{TT}
V_{OCM}	Common Mode ECL Output Voltage	-1.5	—	-1.0	V	50Ω to V_{TT}
V_{IDIF}	Differential ECL Input Voltage	200	—	1200	mV	
V_{ICM}	Common Mode ECL Input Voltage	-1.5	—	-0.5	V	
I_{IHE}	Input HIGH ECL Current	—	—	+200	µA	V_{IN} = -0.7V
I_{ILE}	Input LOW ECL Current	-50	—	—	µA	V_{IN} = -2.0V
V_{IHT}	Input HIGH voltage (TTL)	2.0	—	4.3	V	
V_{ILT}	Input LOW voltage (TTL)	0	—	0.8	V	
I_{IHT}	Input HIGH current (TTL)	—	50	—	µA	2.0V < V_{IN} < 4.3V
I_{ILT}	Input LOW current (TTL)	-500	—	—	µA	-0.5V < V_{IN} < 0.8V
I_{VTTL}	VTTL Supply Current	—	—	20	mA	
I_{VTT}	VTT Supply Current	—	—	2850	mA	Outputs open
P_D	Power dissipation	—	—	5800	mW	

AC Characteristics *(Over recommended operating conditions. ECL Output load 50Ω to V_{TT}.)*

Table 2: Data Flow Mode.

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_{PW}	Minimum input pulse width	640	—	—	pS	Worst case 60/40 input duty cycle
T_{DLY}	Propagation delay	540	—	1800	pS	—
Tduty	Duty cycle distortion	—	—	100	pS	at 1.6 Gb/s Note(1)
Tskew	Output to output skew	—	—	200	pS	On a given part broadcast mode
Tpskew	Data path skew	—	—	500	pS	For any 2 paths from I+/I- to Z+/Z- on a given part

(1) Duty cycle distortion = duty cycle out - duty cycle in (pS) . With 8B/10B encoded data.

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AC Timing Waveforms

Figure 2: Normal Data Flow Timing

Minimum Input Pulse Width & Propagation Delay

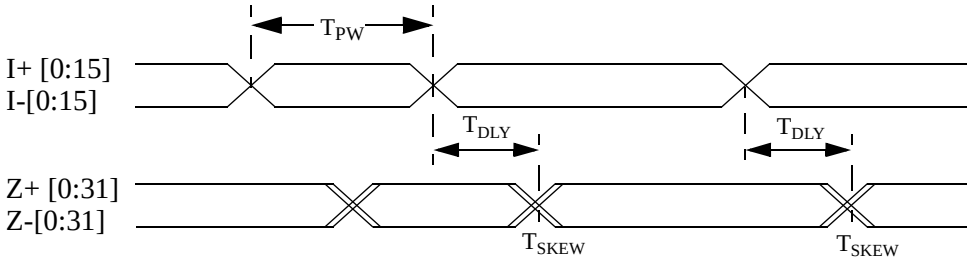

Table 3: Configuration, Broadcast, FlowThru Mode.

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_{LSW}	LSTROBE[0:1] pulse width	5	—	—	nS	—
T_{GSW}	GSTROBE pulse width	5	—	—	nS	—
T_{GSZ}	GSTROBE to Z+/Z- Outputs Delay	1.5	—	5000	nS	—
T_{LSZ}	LSTROBE[0:1] to Z+/Z- Outputs Delay	2	—	6000	nS	GSTROBE high
T_{ALSSU}	A[0:7] to LSTROBE setup time	3	—	—	nS	—
T_{ALSH}	A[0:7] to LSTROBE hold time	1	—	—	nS	—
T_{DLSSU}	D[0:7] to LSTROBE setup time	3	—	—	nS	—
T_{DLSH}	D[0:7] to LSTROBE hold time	1	—	—	nS	—
T_{GLSU}	GSTROBE to LSTROBE setup time	2	—	—	nS	—
T_{GLH}	GSTROBE to LSTROBE hold time	2	—	—	nS	—
T_{CLSSU}	CONFMODE to LSTROBE setup time	3.5	—	—	nS	—
T_{CLSH}	CONFMODE to LSTROBE hold time	1	—	—	nS	—
T_{BLSSU}	BROADCAST to LSTROBE setup time	3.5	—	—	nS	—
T_{BLSH}	BROADCAST to LSTROBE hold time	1	—	—	nS	—
T_{FLSSU}	FLOWTHRU to LSTROBE setup time	3.5	—	—	nS	—
T_{FLSH}	FLOWTHRU to LSTROBE hold time	1	—	—	nS	—

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Figure 3: Configuration Mode Timing

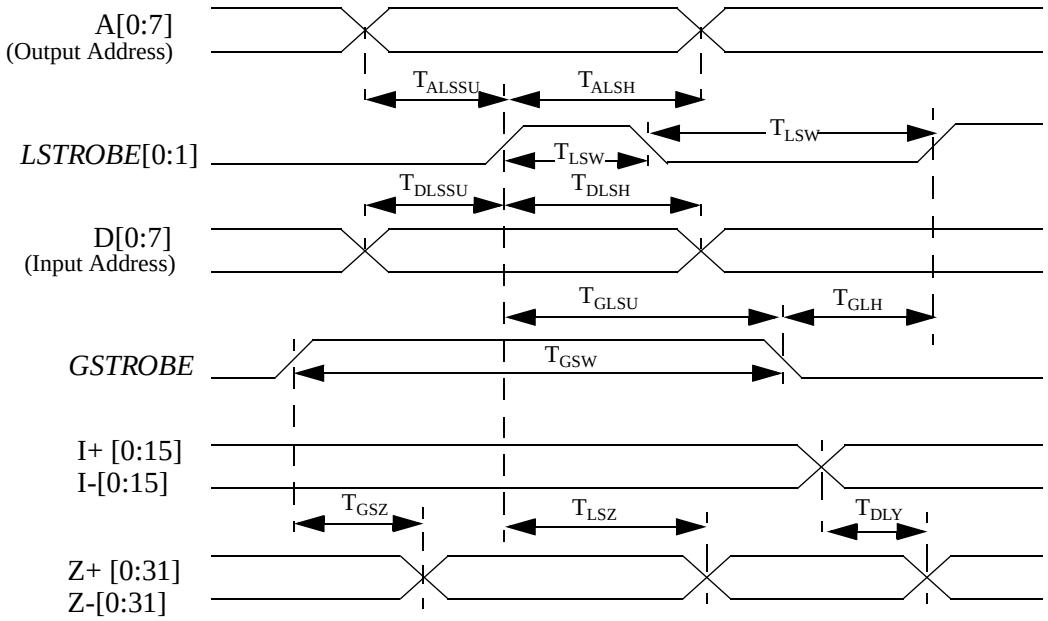

Figure 4: Broadcast and FlowThru Timing

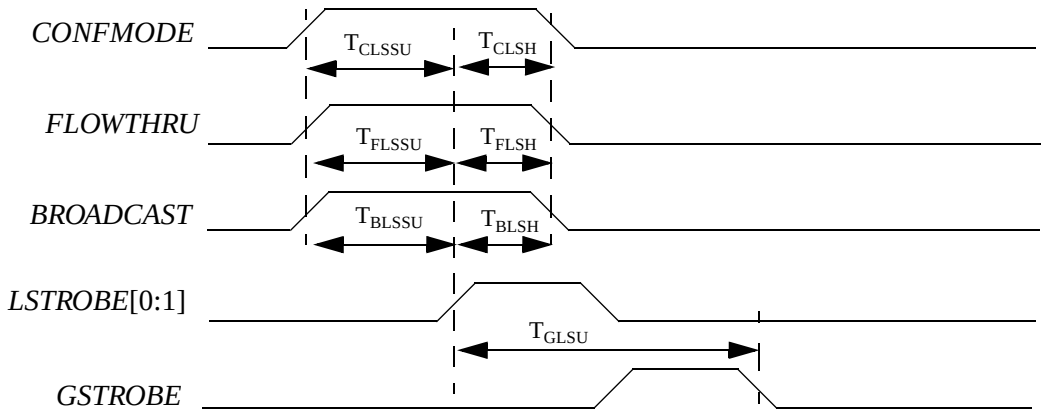

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Table 4: Pin Description

Name	*Pin #*	*I/O*	*Level*	*Description*
VTTL	1	PWR	+3.3V	+3.3V power supply
Z9	2	O	ECL	Serial data out
ZN9	3	O	ECL	Serial data out
VCC	4	PWR	GND	Ground
VCC	5	PWR	GND	Ground
Z8	6	O	ECL	Serial data out
ZN8	7	O	ECL	Serial data out
VCC	8	PWR	GND	Ground
Z7	9	O	ECL	Serial data out
ZN7	10	O	ECL	Serial data out
VTT	11	PWR	-2V	-2.0 power supply
Z6	12	O	ECL	Serial data out
ZN6	13	O	ECL	Serial data out
VTTL	14	PWR	+3.3V	+3.3V power supply
Z5	15	O	ECL	Serial data out
ZN5	16	O	ECL	Serial data out
VCC	17	PWR	GND	Ground
Z4	18	O	ECL	Serial data out
ZN4	19	O	ECL	Serial data out
VTT	20	PWR	-2V	-2.0V power supply
Z3	21	O	ECL	Serial data out
ZN3	22	O	ECL	Serial data out
VCC	23	PWR	GND	Ground
Z2	24	O	ECL	Serial data out
ZN2	25	O	ECL	Serial data out
VCC	26	PWR	GND	Ground
VCC	27	PWR	GND	Ground
Z1	28	O	ECL	Serial data out
ZN1	29	O	ECL	Serial data out
VCC	30	PWR	GND	Ground
Z0	31	O	ECL	Serial data out
ZN0	32	O	ECL	Serial data out
VTT	33	PWR	-2V	-2.0V power supply

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Name	*Pin #*	*I/O*	*Level*	*Description*
I0	34	I	ECL	Serial data in
IN0	35	I	ECL	Serial data in
VCC	36	PWR	GND	Ground
I1	37	I	ECL	Serial data in
IN1	38	I	ECL	Serial data in
VTTL	39	PWR	+3.3V	+3.3V power supply
I2	40	I	ECL	Serial data in
IN2	41	I	ECL	Serial data in
VTT	42	PWR	-2V	-2.0V power supply
I3	43	I	ECL	Serial data in
IN3	44	I	ECL	Serial data in
VCC	45	PWR	GND	Ground
I4	46	I	ECL	Serial data in
IN4	47	I	ECL	Serial data in
VCC	48	PWR	GND	Ground
VCC	49	PWR	GND	Ground
I5	50	I	ECL	Serial data in
IN5	51	I	ECL	Serial data in
VTTL	52	PWR	+3.3V	+3.3V power supply
N/C	53			No connection
N/C	54			No connection
N/C	55			No connection
N/C	56			No connection
N/C	57			No connection
N/C	58			No connection
VCC	59	PWR	GND	Ground
VSCIPNC	60	I	ECL	Test input (tie to -2V)
VSCOPNC	61	O	ECL	Test ouput (leave open)
VTT	62	PWR	-2V	-2.0V power supply
I6	63	I	ECL	Serial data in
IN6	64	I	ECL	Serial data in
VCC	65	PWR	GND	Ground
I7	66	I	ECL	Serial data in
IN7	67	I	ECL	Serial data in

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Name	*Pin #*	*I/O*	*Level*	*Description*
VCC	68	PWR	GND	Ground
VCC	69	PWR	GND	Ground
I8	70	I	ECL	Serial data in
IN8	71	I	ECL	Serial data in
VTT	72	PWR	-2V	-2.0V power supply
I9	73	I	ECL	Serial data in
IN9	74	I	ECL	Serial data in
VTTL	75	PWR	+3.3V	+3.3V power supply
I10	76	I	ECL	Serial data in
IN10	77	I	ECL	Serial data in
VCC	78	PWR	GND	Ground
VCC	79	PWR	GND	Ground
I11	80	I	ECL	Serial data in
IN11	81	I	ECL	Serial data in
VTTL	82	PWR	+3.3V	+3.3V power supply
I12	83	I	ECL	Serial data in
IN12	84	I	ECL	Serial data in
VTT	85	PWR	-2V	-2.0V power supply
I13	86	I	ECL	Serial data in
IN13	87	I	ECL	Serial data in
VCC	88	PWR	GND	Ground
VCC	89	PWR	GND	Ground
I14	90	I	ECL	Serial data in
IN14	91	I	ECL	Serial data in
VCC	92	PWR	GND	Ground
I15	93	I	ECL	Serial data in
IN15	94	I	ECL	Serial data in
VTT	95	PWR	-2V	-2.0V power supply
N/C	96			No connection
GSTROBE	97	I	TTL	Latch enable to transfer holding register data to control latches
VCC	98	PWR	GND	Ground
FLOWTHRU	99	I	TTL	Control signal to enable flow thru mode
BROADCAST	100	I	TTL	Control signal to enable broadcast mode
CONFMODE	101	I	TTL	Control signal to select configuration method

Name	*Pin #*	*I/O*	*Level*	*Description*
N/C	102			No connection
N/C	103			No connection
N/C	104			No connection
VTTL	105	PWR	+3.3V	+3.3V power supply
Z31	106	O	ECL	Serial data out
ZN31	107	O	ECL	Serial data out
VCC	108	PWR	GND	Ground
VCC	109	PWR	GND	Ground
Z30	110	O	ECL	Serial data out
ZN30	111	O	ECL	Serial data out
VCC	112	PWR	GND	Ground
Z29	113	O	ECL	Serial data out
ZN29	114	O	ECL	Serial data out
VTT	115	PWR	-2V	-2.0V power supply
Z28	116	O	ECL	Serial data out
ZN28	117	O	ECL	Serial data out
VTTL	118	PWR	+3.3V	+3.3V power supply
Z27	119	O	ECL	Serial data out
ZN27	120	O	ECL	Serial data out
VCC	121	PWR	GND	Ground
Z26	122	O	ECL	Serial data out
ZN26	123	O	ECL	Serial data out
VTT	124	PWR	-2V	-2.0V power supply
Z25	125	O	ECL	Serial data out
ZN25	126	O	ECL	Serial data out
VCC	127	PWR	GND	Ground
Z24	128	O	ECL	Serial data out
ZN24	129	O	ECL	Serial data out
VCC	130	PWR	GND	Ground
VCC	131	PWR	GND	Ground
Z23	132	O	ECL	Serial data out
ZN23	133	O	ECL	Serial data out
VCC	134	PWR	GND	Ground
Z22	135	O	ECL	Serial data out

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Name	*Pin #*	*I/O*	*Level*	*Description*
ZN22	136	O	ECL	Serial data out
VTT	137	PWR	-2V	-2.0V power supply
Z21	138	O	ECL	Serial data out
ZN21	139	O	ECL	Serial data out
VCC	140	PWR	GND	Ground
Z20	141	O	ECL	Serial data out
ZN20	142	O	ECL	Serial data out
VTTL	143	PWR	+3.3V	+3.3V power supply
Z19	144	O	ECL	Serial data out
ZN19	145	O	ECL	Serial data out
VTT	146	PWR	-2V	-2.0V power supply
Z18	147	O	ECL	Serial data out
ZN18	148	O	ECL	Serial data out
VCC	149	PWR	GND	Ground
Z17	150	O	ECL	Serial data out
ZN17	151	O	ECL	Serial data out
VCC	152	PWR	GND	Ground
VCC	153	PWR	GND	Ground
Z16	154	O	ECL	Serial data out
ZN16	155	O	ECL	Serial data out
VTTL	156	PWR	+3.3V	+3.3V power supply
D0	157	I	TTL	Input address
D1	158	I	TTL	Input address
D2	159	I	TTL	Input address
D3	160	I	TTL	Input address
D4	161	I	TTL	Input address
D5	162	I	TTL	Input address
VCC	163	PWR	GND	Ground
D6	164	I	TTL	Input address
N/C	165			No connection
VTT	166	PWR	-2V	-2.0V power supply
N/C	167			No connection
N/C	168			No connection
VCC	169	PWR	GND	Ground

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Name	*Pin #*	*I/O*	*Level*	*Description*
Z15	170	O	ECL	Serial data out
ZN15	171	O	ECL	Serial data out
VCC	172	PWR	GND	Ground
VCC	173	PWR	GND	Ground
Z14	174	O	ECL	Serial data out
ZN14	175	O	ECL	Serial data out
VTT	176	PWR	-2V	-2.0V power supply
Z13	177	O	ECL	Serial data out
ZN13	178	O	ECL	Serial data out
VTTL	179	PWR	+3.3V	+3.3V power supply
D7	180	I	TTL	Input address
A0	181	I	TTL	Output address
VCC	182	PWR	GND	Ground
VCC	183	PWR	GND	Ground
LSTROBE0	184	I	TTL	Load addresses into holding registers
LSTROBE1	185	I	TTL	Load addresses into holding registers
VTTL	186	PWR	+3.3V	+3.3V power supply
VSCTE	187	I	-2V	Test enable (tie to -2V)
N/C	188			No connection
VTT	189	PWR	-2V	-2.0V power supply
Z12	190	O	ECL	Serial data out
ZN12	191	O	ECL	Serial data out
VCC	192	PWR	GND	Ground
VCC	193	PWR	GND	Ground
Z11	194	O	ECL	Serial data out
ZN11	195	O	ECL	Serial data out
VCC	196	PWR	GND	Ground
Z10	197	O	ECL	Serial data out
ZN10	198	O	ECL	Serial data out
VTT	199	PWR	-2V	-2.0V power supply
N/C	200			No connection
A1	201	I	TTL	Output address
VCC	202	PWR	GND	Ground
A2	203	I	TTL	Output address

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Name	Pin #	I/O	Level	Description
A3	204	I	TTL	Output address
A4	205	I	TTL	Output address
A5	206	I	TTL	Output address
A6	207	I	TTL	Output address
A7	208	I	TTL	Output address

Parametric NOR Chain

The VSC850 supports boundary scan in the form of asynchronous NOR chain at I/O ring. This feature provides the ability to test the connection for external TTL input pins to the chip. To invoke the test, drive VSCTE input to 0V and assert all TTL inputs high. Toggle VSCIPNC input pin. Output pin VSCOPNC will toggle accordingly. Pin VSCIPNC is held low and the first input pin, A[7], is toggled. Observe that VSCOPNC output toggles. Similarly, assert A[7] low and toggle A[6] ... following the order of the scan chain. Note that all differential ECL pins I+[0:15]/I-[0:15] and Z+[0:31]/Z-[0:31] are excluded from this test.

Scan Chain Order :

VSCIPNC, A[7:1], LSTROBE[1:0], A[0], D[7:0], CONFMODE, BROADCAST, FLOWTHRU, GSTROBE, VSCOPNC.

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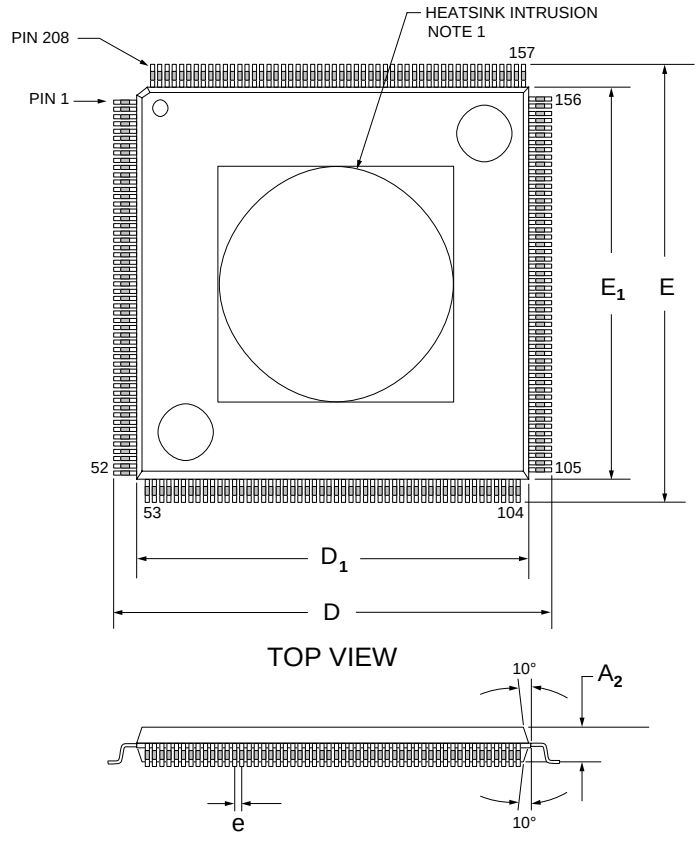
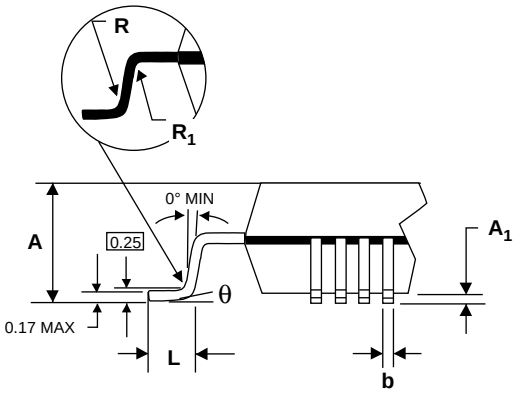
Package Information

208 PQFP Package Dimensions





Key	*mm*	*Tolerances*
A	4.07	MAX
A_1	0.25	MIN
A_2	3.49	±.10
D	30.60	±.4
D_1	28.00	±.10
E	30.60	±.4
E_1	28.00	±.10
L	0.60	+.15/-.10
e	0.50	BASIC
b	0.22	±.05
θ	0° - 10°	
R_1	.15	TYP
R	.25	MAX

NOTES:
(1) Exposed Heatspreader will be either 20.32 ±.50 round or 12.0 ± .50 square
(2) Drawing not to scale.
Package #: 101-228-6, Issue #:1

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Ordering Information

VSC850-QG

Device Type:

VSC850: 16x32 Crosspoint Switch

Package Type

QG: 208 Plastic Quad Flat Pack (PQFP)

Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products, specifications or other information at any time without prior notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to placing any orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

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