S19FL032P MirrorBit® ROM

32-Mbit CMOS 3.0 Volt MirrorBit ROM with 104-MHz SPI (Serial Peripheral Interface) Multi I/O Bus

Data Sheet *(Preliminary)*

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Publication Number S19FL032P_00 **Revision** 02 **Issue Date** August 5, 2009

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S19FL032P MirrorBit® ROM

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***Data Sheet** (Preliminary)*

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - Full voltage range: 2.7 to 3.6V
- **Device ID**
  - JEDEC standard two-byte electronic signature
  - RES command one-byte electronic signature for backward compatibility
- **Process technology**
  - Manufactured on 0.09 µm MirrorBit® process technology
- **Package option**
  - Industry Standard Pinouts
  - 8-pin SO package (208 mils)
  - 16-pin SO package (300 mils)

Performance Characteristics

- **Speed**
  - Normal READ (Serial): 40 MHz clock rate
  - FAST_READ (Serial): 104 MHz clock rate (maximum)
  - DUAL I/O FAST_READ: 80 MHz clock rate or 20 MB/s effective data rate
  - QUAD I/O FAST_READ: 80 MHz clock rate or 40 MB/s effective data rate
- **Power saving standby mode**
  - Standby Mode 80 µA (typical)
  - Deep Power-Down Mode 3 µA (typical)
- **Data retention**
  - 20 years typical

General Description

The S19FL032P is a 3.0 Volt (2.7V to 3.6V), single-power-supply Serial Peripheral Interface (SPI) read-only memory device. The S19FL032P device is fully backward compatible with the S19FL032A device.

The S19FL032P device adds the following high-performance features using 4 new instructions:

- Dual Output Read using both SI and SO pins as output pins at a clock rate of up to 80 MHz
- Quad Output Read using SI, SO, IO2 and HOLD# pins as output pins at a clock rate of up to 80 MHz
- Dual I/O High Performance Read using both SI and SO pins as input and output pins at a clock rate of up to 80 MHz
- Quad I/O High Performance Read using SI, SO, IO2 and HOLD# pins as input and output pins at a clock rate of up to 80 MHz

Each device requires only a 3.0-volt power supply (2.7V to 3.6V) for read functions.

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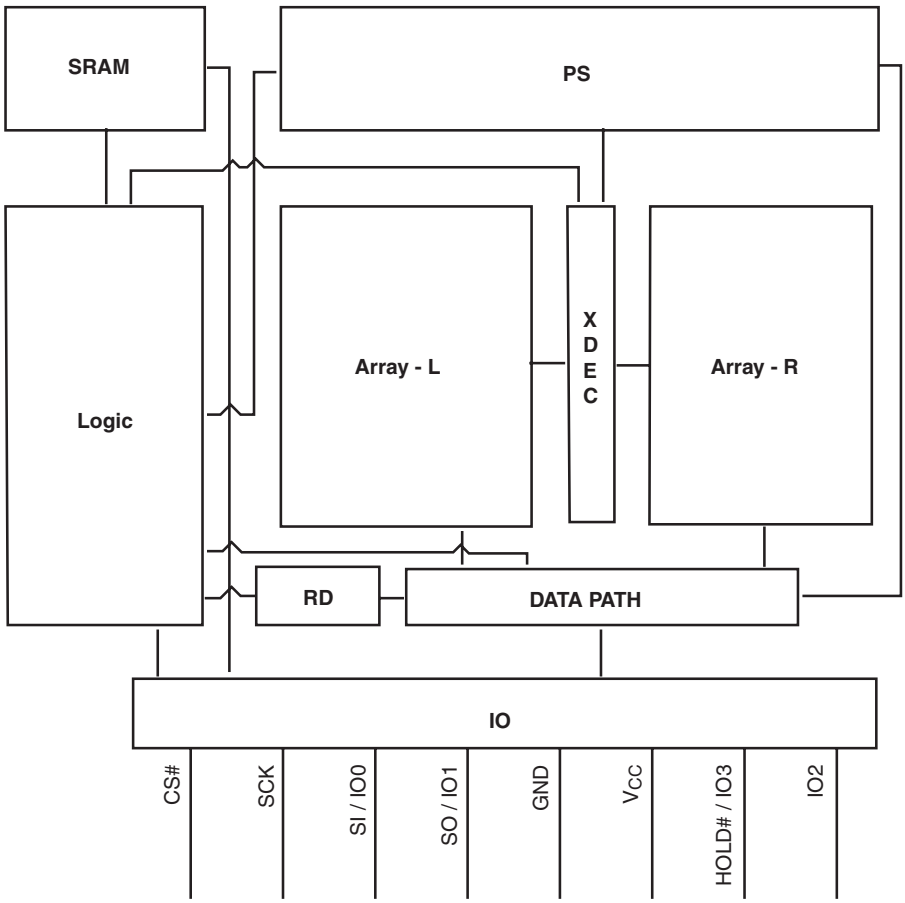
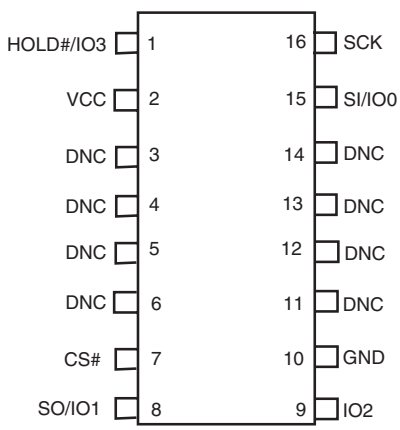


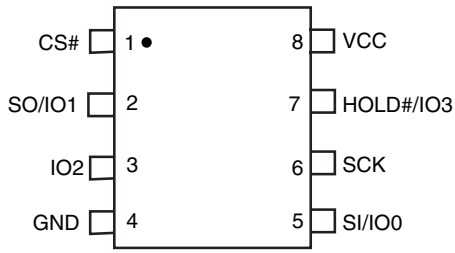
2. Connection Diagrams

Figure 2.1 16-pin Plastic Small Outline Package (SO)



Note
DNC = Do Not Connect (Reserved for future use)
IO2 = NC on Single I/O use

Figure 2.2 8-pin Plastic Small Outline Package (SO)

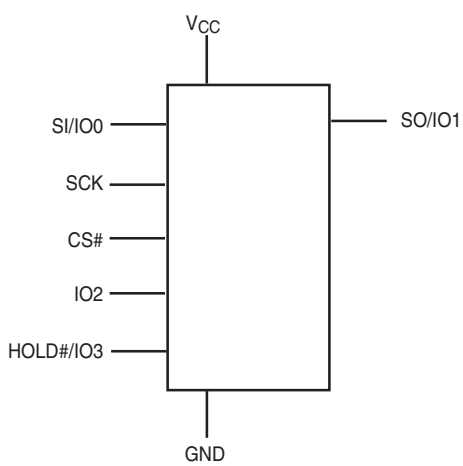


Note
IO2 = NC on Single I/O

3. Input/Output Descriptions

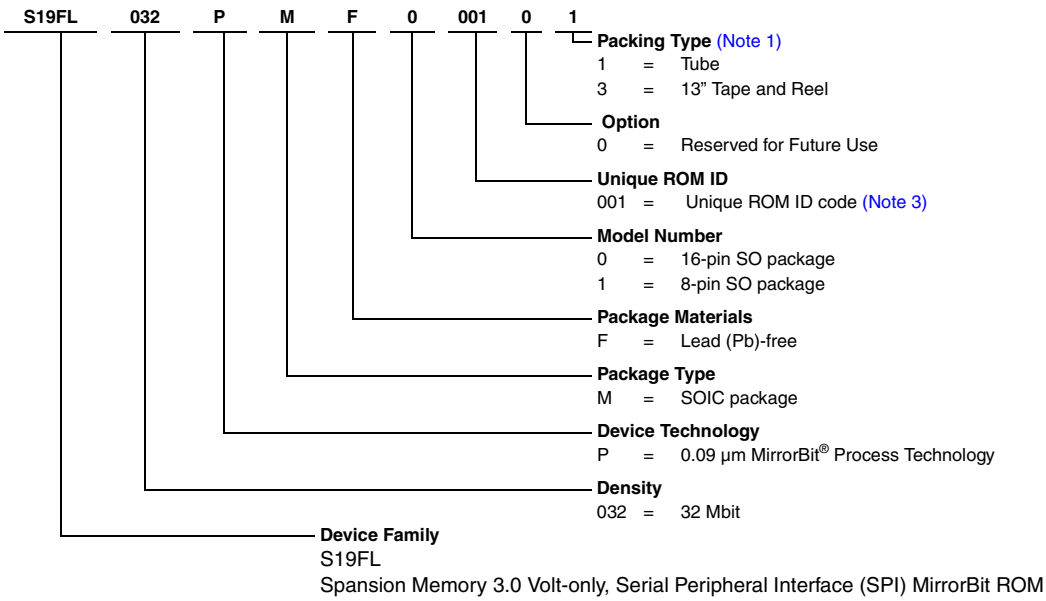
Signal	I/O	Description
SO/IO1	I/O	**Serial Data Output**: Transfers data serially out of the device on the falling edge of SCK. Functions as an input pin in Dual and Quad I/O modes.
SI/IO0	I/O	**Serial Data Input**: Transfers instructions and addresses serially into the device. Device latches commands, addresses on SI on the rising edge of SCK. Functions as an output pin in Dual and Quad I/O mode.
SCK	Input	**Serial Clock**: Provides serial interface timing. Latches commands, addresses, and data on SI on rising edge of SCK. Triggers output on SO after the falling edge of SCK.
CS#	Input	**Chip Select**: Places device in active power mode when driven low. Deselects device and places SO at high impedance when high. After power-up, device requires a falling edge on CS# before any command is written.
HOLD#/IO3	I/O	**Hold**: Pauses any serial communication with the device without deselecting it. When driven low, SO is at high impedance, and all input at SI and SCK are ignored. Requires that CS# also be driven low. Functions as an output pin in Quad I/O mode.
IO2	I/O	**IO2**: NC on Single I/O mode. Functions as an output pin in Quad I/O mode.
V_{CC}	Input	**Supply Voltage**
GND	Input	**Ground**

4. Logic Symbol



5. Ordering Information

The ordering part number is formed by a valid combination of the following:



Note

All S19FL-P devices are offered over the industrial temperature (-40°C to 85°C) range and 104 MHz (serial), 80 MHz (dual/quad) maximum clock rate.

5.1 Valid Combinations

Table 5.1 lists the valid combinations configurations planned to be supported in volume for this device.

Table 5.1 S19FL032P Valid Combinations Table

S19FL-P Valid Combinations					
Base Ordering Part Number	**Package & Material**	**Model Number**	**Unique ROM ID**	**Option**	**Packing Type**
S19FL032P	MF	0, 1 (Note 2)	XXX (Note 3)	0	1, 3 (Note 1)

Note

1. *Type 1 is standard. Specify other options as required.*
2. *Contact your local sales office for availability.*
3. *Unique ROM ID is assigned by the factory.*

6. Spansion SPI Modes

A microcontroller can use either of its two SPI modes to control Spansion SPI ROM devices:

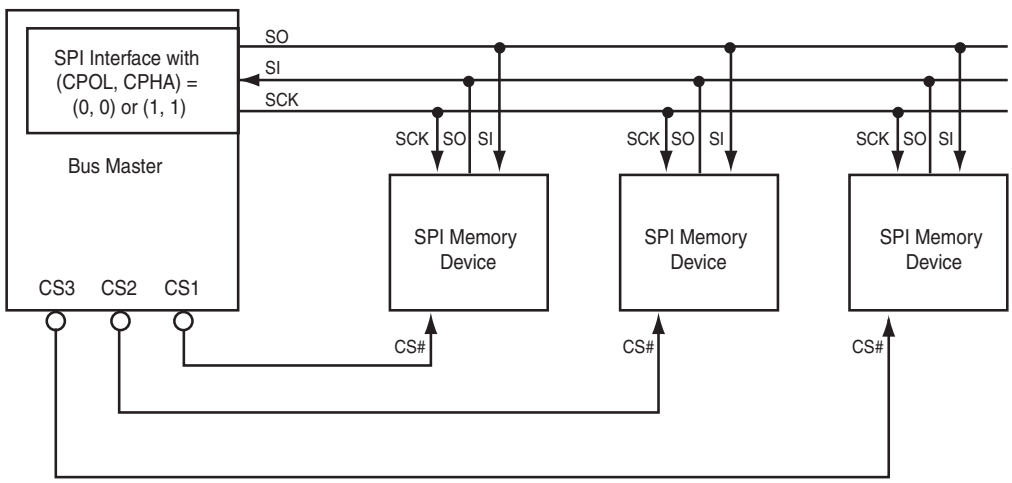
- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When the bus master is in standby mode, SCK is as shown in Figure 6.2 for each of the two modes:

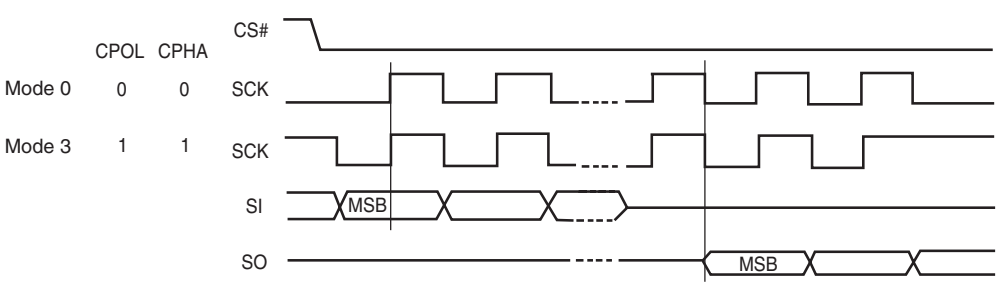
- SCK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

Figure 6.1 Bus Master and Memory Devices on the SPI Bus



Note
The Hold (HOLD#) signal should be driven high (logic level 1) or low (logic level 0) as appropriate.

Figure 6.2 SPI Modes Supported



7. Device Operations

All Spansion SPI devices accept and output data in bytes (8 bits at a time). The SPI device is a slave device that supports an inactive clock while CS# is held low.

7.1 Dual and Quad I/O Mode

The S19FL032P device supports Dual and Quad I/O operation when using the Dual/Quad Output Read Mode and the Dual/Quad I/O High Performance Mode instructions. Using the Dual or Quad I/O instructions allows data to be transferred to or from the device at two to four times the rate of standard SPI devices. When operating in the Dual or Quad I/O High Performance Mode (BBh or EBh instructions), data can be read at fast speed using two or four data bits at a time, and the 3-byte address can be input two or four address bits at a time.

7.2 Active Power and Standby Power Modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is Low. When CS# is high. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}. The Deep Power-Down (DP) command provides additional data protection against inadvertent signals. After writing the DP command the device reduces its power consumption to I_{DP}.

7.3 Configuration Register

The Configuration Register contains the control bits that can be read or set by specific commands.

- The QUAD bit is non-volatile and sets the pin out of the device to Quad mode; that is HOLD# becomes IO3. The instructions for Serial, Dual Output, and Dual I/O reads will function as normal. The HOLD# functionality will not work when the device is set in Quad mode.

Table 7.1 Configuration Register Table

Bit	Bit Name	Bit Function	Description
7	NA	-	Not Used
6	NA	-	Not Used
5	NA	-	Not Used
4	NA	-	Not Used
3	NA	-	Not Used
2	NA	-	Not Used
1	QUAD	Puts the device into Quad I/O mode	1 = Quad I/O 0 = Dual or Serial I/O (Default)
0	NA	-	Not Used

Note

(Default) indicates the value of each Configuration Register bit set upon initial factory shipment.

7.4 Hold Mode (HOLD#)

The Hold input (HOLD#) stops any serial communication with the device.

The Hold mode starts on the falling edge of HOLD# if SCK is also low (see Figure 7.1, standard use). If the falling edge of HOLD# does not occur while SCK is low, the Hold mode begins after the next falling edge of SCK (non-standard use).

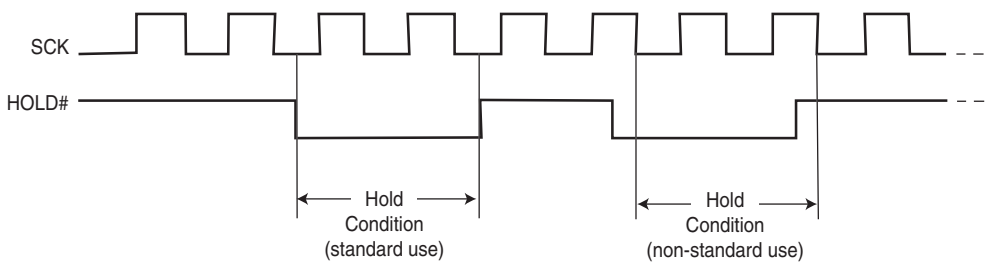
The Hold mode ends on the rising edge of HOLD# signal (standard use) if SCK is also low. If the rising edge of HOLD# does not occur while SCK is low, the Hold mode ends on the next falling edge of CLK (non-standard use) See Figure 7.1.

The SO output is high impedance, and the SI and SCK inputs are ignored (don't care) for the duration of the Hold mode.

CS# must remain low for the entire duration of the Hold mode to ensure that the device internal logic remains unchanged. If CS# goes high while the device is in the Hold mode, the internal logic is reset. To prevent the device from reverting to the Hold mode when device communication is resumed, HOLD# must be held high, followed by driving CS# low.

Note: The HOLD Mode feature is disabled during Quad I/O Mode.

Figure 7.1 Hold Mode Operation



8. Command Definitions

The host system must shift all commands, addresses, and data in and out of the device, beginning with the most significant bit. On the first rising edge of SCK after CS# is driven low, the device accepts the one-byte command on SI (all commands are one byte long), most significant bit first. Each successive bit is latched on the rising edge of SCK. Table 8.1 lists the complete set of commands.

Every command sequence begins with a one-byte command code. The command may be followed by address, data, both, or nothing, depending on the command. CS# must be driven high after the last bit of the command sequence has been written.

The Read Data Bytes (READ), Read Data Bytes at Higher Speed (FAST_READ), Dual Output Read (DOR), Quad Output Read (QOR), Dual I/O High Performance Read (DIOR), Quad I/O High Performance Read (QIOR), Read Status Register (RDSR), Read Configuration Register (RCR), Read Manufacturer and Device ID (READ_ID), Read Identification (RDID) and Release from Deep Power-Down and Read Electronic Signature (RES) command sequences are followed by a data output sequence on SO. CS# can be driven high after any bit of the sequence is output to terminate the operation.

The instruction set is listed in Table 8.1.

Table 8.1 Instruction Set

Operation	Command	One byte Command Code	Description	Address Byte Cycle	Mode Bit Cycle	Dummy Byte Cycle	Data Byte Cycle
Read	READ	(03h) 0000 0011	Read Data bytes	3	0	0	1 to ∞
	FAST_READ	(0Bh) 0000 1011	Read Data bytes at Fast Speed	3	0	1	1 to ∞
	DOR	(3Bh) 0011 1011	Dual Output Read	3	0	1	1 to ∞
	QOR	(6Bh) 0110 1011	Quad Output Read	3	0	1	1 to ∞
	DIOR	(BBh) 1011 1011	Dual I/O High Performance Read	3	1	0	1 to ∞
	QIOR	(EBh) 1110 1111	Quad I/O High Performance Read	3	1	2	1 to ∞
	RDID	(9Fh) 1001 1111	Read Identification	0	0	0	1 to 81
	READ_ID	(90h) 1001 0000	Read Manufacturer and Device Identification	3	0	0	1 to ∞
Configuration Register	RCR	(35h) 0011 0101	Read Configuration Register (CFG)	0	0	0	1 to ∞
Power Saving	DP	(B9h) 1011 1001	Deep Power-Down	0	0	0	0
	RES	(ABh) 1010 1011	Release from Deep Power-Down Mode	0	0	0	0
		(ABh) 1010 1011	Release from Deep Power-Down and Read Electronic Signature	0	0	3	1 to ∞

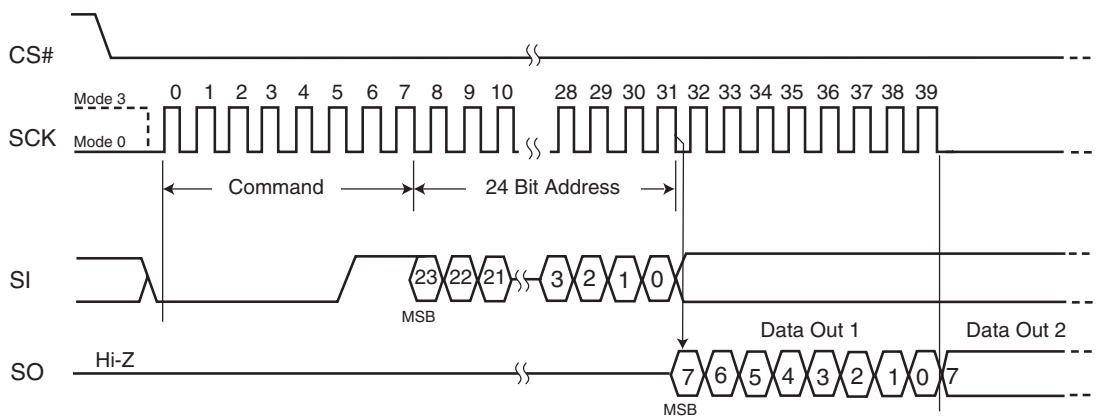
8.1 Read Data Bytes (READ)

The Read Data Bytes (READ) command reads data from the memory array at the frequency (f_{SCK}) presented at the SCK input, with a maximum speed of 40 MHz. The host system must first select the device by driving CS# low. The READ command is then written to SI, followed by a 3 byte address (A23-A0). Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_{SCK}, on the falling edge of SCK.

Figure 8.1 and Table 8.1 on page 13 detail the READ command sequence. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single READ command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The READ command is terminated by driving CS# high at any time during data output.

Figure 8.1 Read Data Bytes (READ) Command Sequence



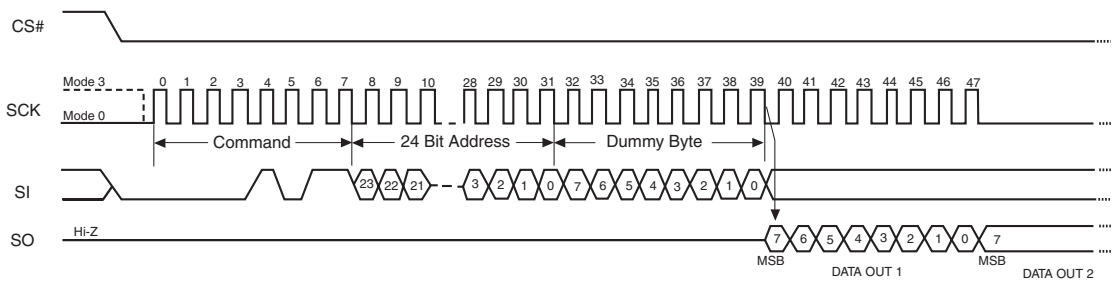
8.2 Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ command reads data from the memory array at the frequency (f_{SCK}) presented at the SCK input, with a maximum speed of 104 MHz. The host system must first select the device by driving CS# low. The FAST_READ command is then written to SI, followed by a 3 byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_{SCK}, on the falling edge of SCK.

The FAST_READ command sequence is shown in Figure 8.2 and Table 8.1 on page 13. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single FAST_READ command. When the highest address is reached, the address counter reverts to 000000h, allowing the read sequence to continue indefinitely.

The FAST_READ command is terminated by driving CS# high at any time during data output.

Figure 8.2 Read Data Bytes at Higher Speed (FAST_READ) Command Sequence



8.3 Dual Output Read Mode (DOR)

The Dual Output Read instruction is similar to the FAST_READ instruction, except that the data is shifted out 2 bits at a time using 2 pins (SI/IO0 and SO/IO1) instead of 1 bit, at a maximum frequency of 80 MHz. The Dual Output Read mode effectively doubles the data transfer rate compared to the FAST_READ instruction.

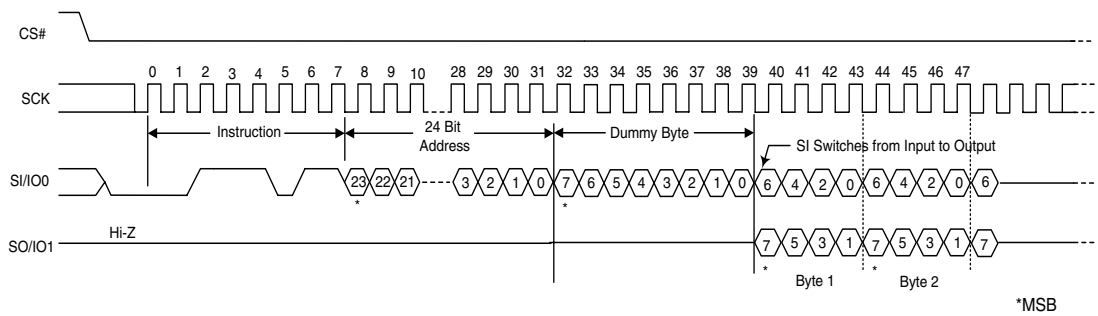
The host system must first select the device by driving CS# low. The Dual Output Read command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. Then the memory contents, at the address that is given, are shifted out two bits at a time through the IO0 (SI) & IO1 (SO) pins at a frequency f_{SCK} on the falling edge of SCK.

The Dual Output Read command sequence is shown in Figure 8.3 and Table 8.1 on page 13. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Dual Output Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The Dual Output Read command is terminated by driving CS# high at any time during data output.

Figure 8.3 Dual Output Read Instruction Sequence



8.4 Quad Output Read Mode (QOR)

The Quad Output Read instruction is similar to the FAST_READ instruction, except that the data is shifted out 4 bits at a time using 4 pins (SI/IO0, SO/IO1, IO2 and HOLD#/IO3) instead of 1 bit, at a maximum frequency of 80 MHz. The Quad Output Read mode effectively doubles the data transfer rate compared to the Dual Output Read instruction, and is four times the data transfer rate of the FAST_READ instruction.

The host system must first select the device by driving CS# low. The Quad Output Read command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. Then the memory contents, at the address that are given, are shifted out four bits at a time through IO0 (SI), IO1 (SO), IO2, and IO3 (HOLD#) pins at a frequency f_{SCK} on the falling edge of SCK.

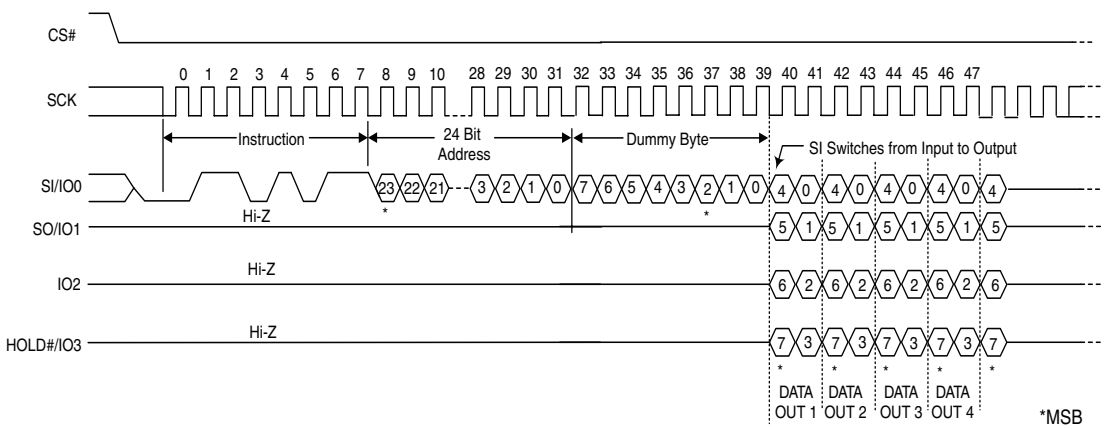
The Quad Output Read command sequence is shown in Figure 8.4 and Table 8.1 on page 13. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Quad Output Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The Quad Output Read command is terminated by driving CS# high at any time during data output.

The Quad bit of Configuration Register must be set (CR Bit1 = 1) to enable the Quad mode capability of the S19FL device.

Figure 8.4 Quad Output Read Instruction Sequence



8.5 DUAL I/O High Performance Read Mode (DIOR)

The Dual I/O High Performance Read instruction is similar to the Dual Output Read instruction, except that it improves throughput by allowing input of the address bits (A23-A0) using 2 bits per SCK via two input pins (SI/IO2 and SO/IO1), at a maximum frequency of 80 MHz.

The host system must first select the device by driving CS# low. The Dual I/O High Performance Read command is then written to SI, followed by a 3-byte address (A23-A0) and a 1-byte Mode instruction, with two bits latched on the rising edge of SCK. Then the memory contents, at the address that is given, are shifted out two bits at a time through IO0 (SI) and IO1 (SO).

The DUAL I/O High Performance Read command sequence is shown in Figure 8.5 and Table 8.1 on page 13. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single DUAL I/O High Performance Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

In addition, address jumps can be done without exiting the Dual I/O High Performance Mode through the setting of the Mode bits (after the Address (A23-0) sequence, as shown in Figure 8.5). This added feature removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7-4) of the Mode bits control the length of the next Dual I/O High Performance instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3-0) of the Mode bits are DON'T CARE ("x"). If the Mode bits equal Axh, then the device remains in Dual I/O High Performance Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without requiring the BBh instruction opcode, as shown in Figure 8.6, thus eliminating eight cycles for the instruction sequence. However, if the Mode bits are any value other than Axh, then the next instruction (after CS# is raised high and then asserted low) requires the instruction sequence, which is normal operation. The following sequences will release the device from Dual I/O High Performance Read mode; after which, the device can accept standard SPI instructions:

1. During the Dual I/O High Performance Instruction Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised high and then asserted low, the device will be released from Dual I/O High Performance Read mode.
2. Furthermore, during any operation, if CS# toggles high to low to high for eight cycles (or less) **and** data input (IO0 & IO1) are not set for a valid instruction sequence, then the device will be released from Dual I/O High Performance Read mode.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The read instruction can be terminated by driving the CS# pin to the logic high state. The CS# pin can be driven high at any time during data output to terminate a read operation.

Figure 8.5 DUAL I/O High Performance Read Instruction Sequence

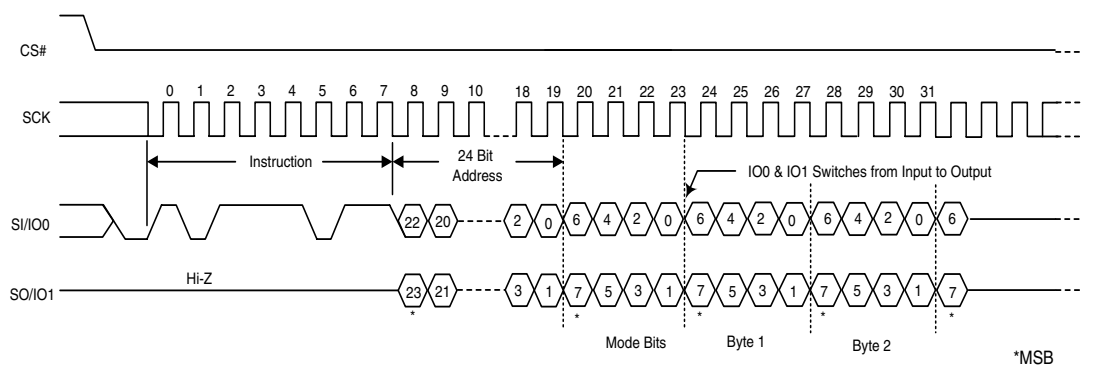
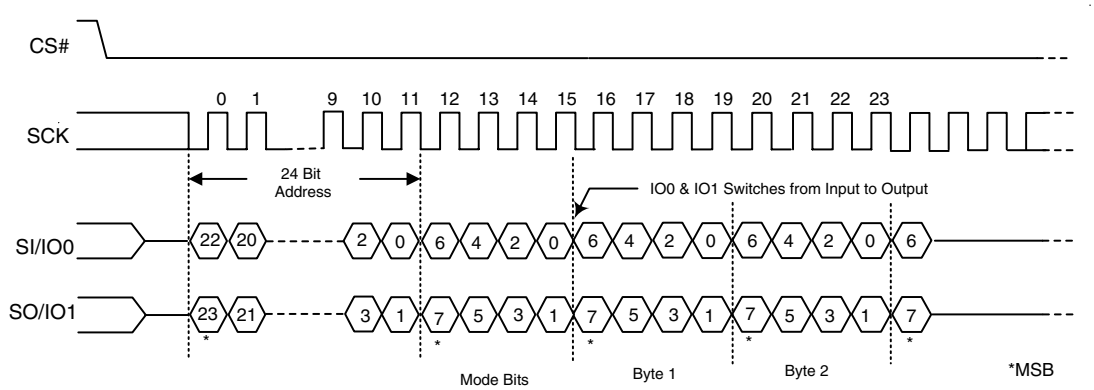


Figure 8.6 Continuous Dual I/O High Performance Read Instruction Sequence



8.6 Quad I/O High Performance Read Mode (QIOR)

The Quad I/O High Performance Read instruction is similar to the Quad Output Read instruction, except that it further improves throughput by allowing input of the address bits (A23-A0) using 4 bits per SCK via four input pins (SI/IO0, SO/IO1, IO2 and HOLD#/IO3), at a maximum frequency of 80 MHz.

The host system must first select the device by driving CS# low. The Quad I/O High Performance Read command is then written to SI, followed by a 3-byte address (A23-A0) and a 1-byte Mode instruction, with four bits latched on the rising edge of SCK. Note that four dummy clocks are required prior to the data input. Then the memory contents, at the address that is given, are shifted out four bits at a time through IO0 (SI), IO1 (SO), IO2, and IO3 (HOLD#).

The Quad I/O High Performance Read command sequence is shown in Figure 8.7 and Table 8.1 on page 13. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Quad I/O High Performance Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

In addition, address jumps can be done without exiting the Quad I/O High Performance Mode through the setting of the Mode bits (after the Address (A23-0) sequence, as shown in Figure 8.7). This added feature the removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7-4) of the Mode bits control the length of the next Quad I/O High Performance instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3-0) of the Mode bits are DON'T CARE (“x”). If the Mode bits equal Axh, then the device remains in Quad I/O High Performance Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without requiring the EBh instruction opcode, as shown in Figure 8.8, thus eliminating eight cycles for the instruction sequence. The following sequences will release the device from Quad I/O High Performance Read mode; after which, the device can accept standard SPI instructions:

1. During the Quad I/O High Performance Instruction Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised high and then asserted low the device will be released from Quad I/O High Performance Read mode.
2. Furthermore, during any operation, if CS# toggles high to low to high for eight cycles (or less) **and** data input (IO0, IO1, IO2, & IO3) are not set for a valid instruction sequence, then the device will be released from Quad I/O High Performance Read mode.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The read instruction can be terminated by driving the CS# pin to the logic high state. The CS# pin can be driven high at any time during data output to terminate a read operation.

Figure 8.7 QUAD I/O High Performance Instruction Sequence

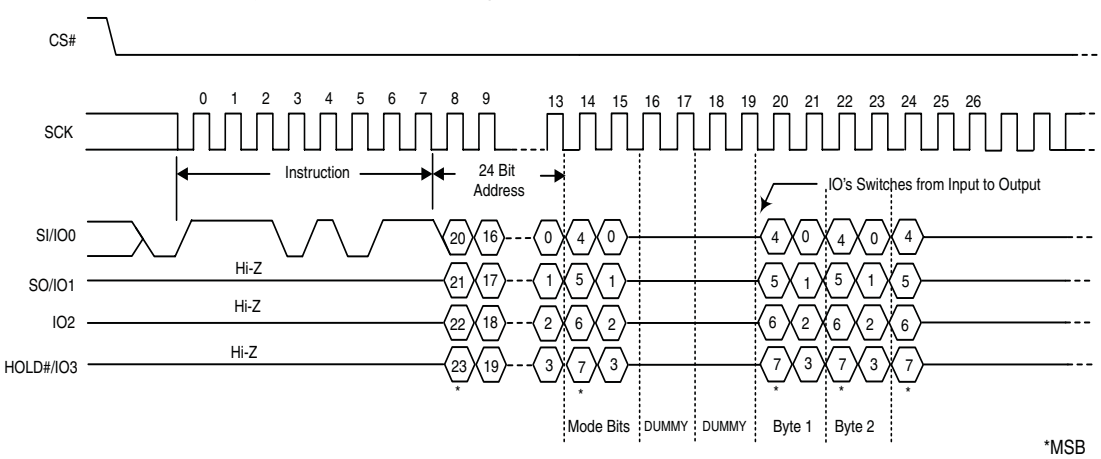
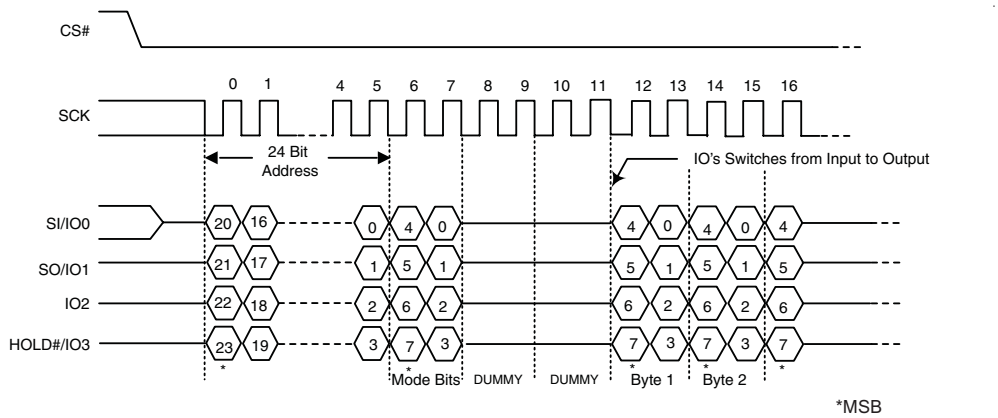


Figure 8.8 Continuous QUAD I/O High Performance Instruction Sequence



8.7 Read Identification (RDID)

The Read Identification (RDID) command outputs the one-byte manufacturer identification, followed by the two-byte device identification. The manufacturer identification is assigned by JEDEC; for Spansion devices, it is 01h. The device identification (2 bytes) is assigned by the device manufacturer.

See Table 8.2 on page 22 for device ID data.

The host system must first select the device by driving CS# low. The RDID command is then written to SI, and each bit is latched on the rising edge of SCK. The 3-byte device identification data is output from the memory array on SO at a frequency f_{SCK}, on the falling edge of SCK.

The RDID command sequence is shown in Figure 8.9 and Table 8.1 on page 13.

Driving CS# high after the device identification data has been read at least once terminates the RDID command. Driving CS# high at any time during data output.

Figure 8.9 Read Identification (RDID) Command Sequence and Data-Out Sequence

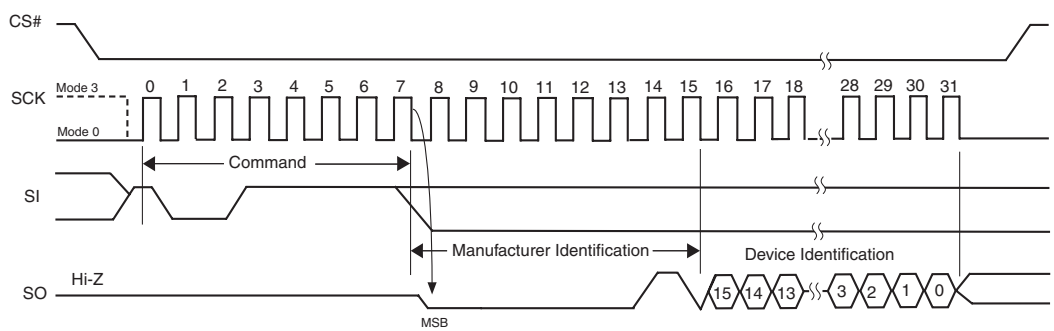


Table 8.2 Manufacturer & Device ID - RDID (JEDEC 9Fh):

Device	Manuf. ID	Device Id		# Extended bytes
	Byte 0	Byte 1	Byte 2	Byte 3
S19FL032P SPI ROM	01h	02h	15h	4Dh

Notes

1. *Byte 0 is Manufacturer ID of Spansion.*
2. *Byte 1 & 2 is Device Id.*
3. *Byte 3 is Extended Device Information String Length, to indicate how many Extended Device Information bytes will follow.*
4. *Bytes 4, 5 and 6 are Spansion reserved (do not use).*
5. *For Bytes 07h-0Fh and 3Dh-3Fh, the data will be read as 0xFF.*
6. *Bytes 10h-50h are factory programmed per JEDEC standard.*

8.8 Read-ID (READ_ID)

The READ_ID instruction provides the S19FL032P manufacturer and device information and is provided as an alternative to the Release from Deep Power-Down and Read Electronic Signature (RES), and the JEDEC Read Identification (RDID) commands.

The instruction is initiated by driving the CS# pin low and shifting in (via the SI input pin) the instruction code “90h” followed by a 24-bit address (which is either 00000h or 00001h). Following this, the Manufacturer ID and the Device ID are shifted out on the SO output pin starting after the falling edge of the SCK serial clock input signal. If the 24-bit address is set to 000000h, the Manufacturer ID is read out first followed by the Device ID. If the 24-bit address is set to 000001h, then the Device ID is read out first followed by the Manufacturer ID. The Manufacturer ID and the Device ID are always shifted out on the SO output pin with the MSB first, as shown in Figure 10-14. Once the device is in Read-ID mode, the Manufacturer ID and Device ID output data toggles between address 000000H and 000001H until terminated by a low to high transition on the CS# input pin. The maximum clock frequency for the Read-ID (90h) command is at 104 MHz (FAST_READ). The Manufacturer ID & Device ID is output continuously until terminated by a low to high transition on CS# chip select input pin.

Figure 8.10 Read-ID (RDID) Command Timing Diagram

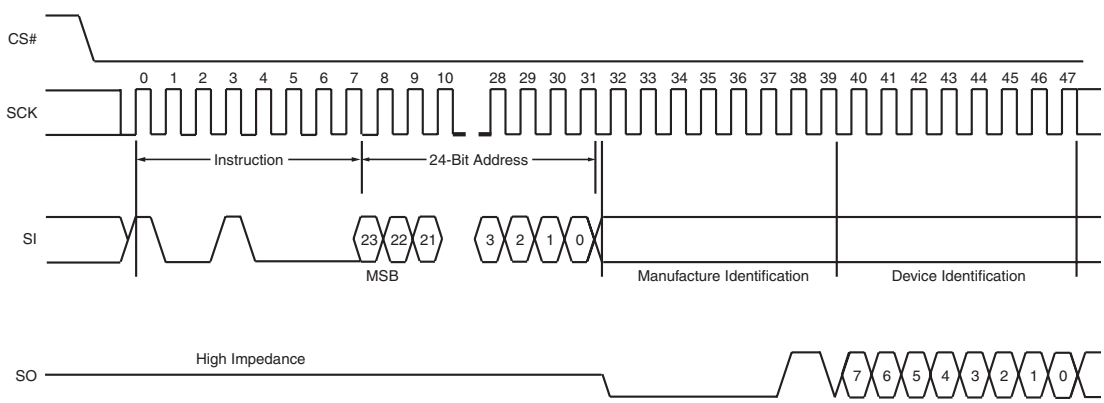


Table 8.3 READ_ID Data-Out Sequence

	Address	Uniform
Manufacturer Identification	00000h	01h
Device Identification	00001h	15h

8.9 Deep Power-Down (DP)

The Deep Power-Down (DP) command provides the lowest power consumption mode of the device. It is intended for periods when the device is not in active use, and ignores all commands except for the Release from Deep Power-Down (RES) command. The standard standby mode, which the device goes into automatically when CS# is high (and all operations in progress are complete), should generally be used for the lowest power consumption when the quickest return to device activity is required.

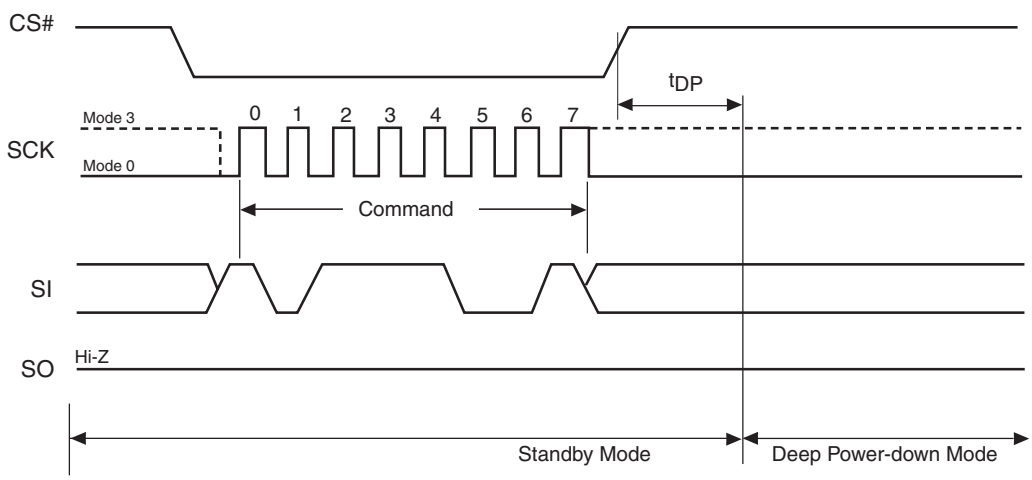
The host system must drive CS# low, and then write the DP command on SI. CS# must be driven low for the entire duration of the DP sequence. The command sequence is shown in Figure 8.11 and Table 8.1 on page 13.

The host system must drive CS# high after the device has latched the 8th bit of the DP command, otherwise the device does not execute the command. After a delay of t_{DP}, the device enters the DP mode and current reduces from I_{SB} to I_{DP} (see Table 13.1 on page 29).

Once the device has entered the DP mode, all commands are ignored except the RES command (which releases the device from the DP mode). The RES command also provides the Electronic Signature of the device to be output on SO, if desired (see Section 8.10 and 8.10.1).

DP mode automatically terminates when power is removed, and the device always powers up in the standard standby mode.

Figure 8.11 Deep Power-Down (DP) Command Sequence



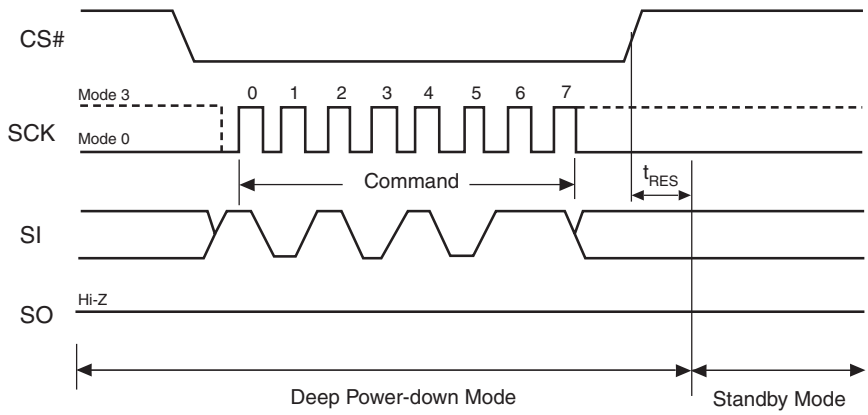
8.10 Release from Deep Power-Down (RES)

The device requires the Release from Deep Power-Down (RES) command to exit the Deep Power-Down mode. When the device is in the Deep Power-Down mode, all commands except RES are ignored.

The host system must drive CS# low and write the RES command to SI. CS# must be driven low for the entire duration of the sequence. The command sequence is shown in Figure 8.12 and Table 8.1 on page 13.

The host system must drive CS# high $t_{RES(max)}$ after the 8-bit RES command byte. The device transitions from DP mode to the standby mode after a delay of t_{RES} (see Figure 15.1). In the standby mode, the device can execute any read command.

Figure 8.12 Release from Deep Power-Down (RES) Command Sequence



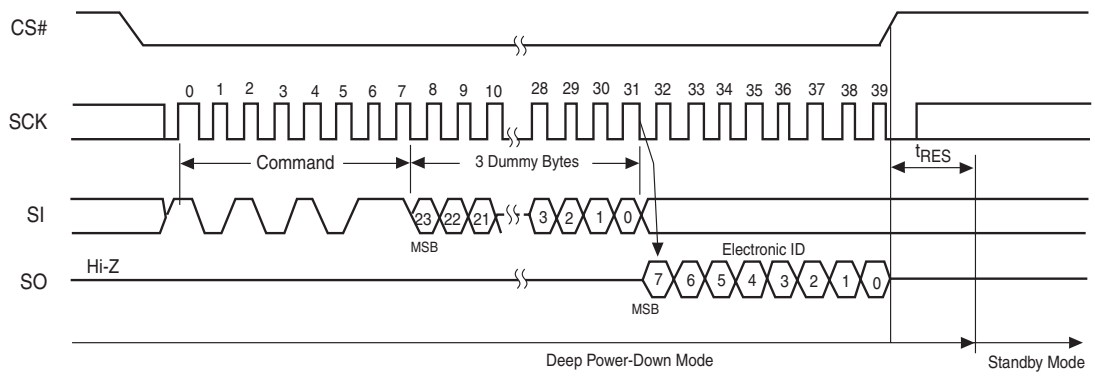
8.10.1 Release from Deep Power-Down and Read Electronic Signature (RES)

The device features an 8-bit Electronic Signature, which can be read using the RES command. See Figure 8.13 and Table 8.1 on page 13 for the command sequence and signature value. The Electronic Signature is not to be confused with the identification data obtained using the RDID command. The device offers the Electronic Signature so that it can be used with previous devices that offered it; however, the Electronic Signature should not be used for new designs, which should read the RDID data instead.

After the host system drives CS# low, it must write the RES command followed by 3 dummy bytes to SI (each bit is latched on SI during the rising edge of SCK). The Electronic Signature is then output on SO; each bit is shifted out on the falling edge of SCK. The RES operation is terminated by driving CS# high after the Electronic Signature is read at least once. Additional clock cycles on SCK with CS# low cause the device to output the Electronic Signature repeatedly.

When CS# is driven high, the device transitions from DP mode to the standby mode after a delay of t_{RES}, as previously described. The RES command always provides access to the Electronic Signature of the device and can be applied even if DP mode has not been entered.

Figure 8.13 Release from Deep Power-Down and RES Command Sequence



9. Power-up and Power-down

During power-up and power-down, certain conditions must be observed. CS# must follow the voltage applied on V_{CC}, and must not be driven low to select the device until V_{CC} reaches the allowable values as follows (see Figure 9.1 and Table 9.1 on page 27):

- At power-up, V_{CC} (min.) plus a period of t_{PU}
- At power-down, GND

A pull-up resistor on Chip Select (CS#) typically meets proper power-up and power-down requirements.

At power-up, the device is in standby mode (not Deep Power-Down mode) and the WEL bit is reset (0).

Each device in the host system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins (this capacitor is generally of the order of 0.1 µF), as a precaution to stabilizing the V_{CC} feed.

When V_{CC} drops from the operating voltage to below the minimum V_{CC} threshold at power-down, all operations are disabled and the device does not respond to any commands.

Figure 9.1 Power-Up Timing Diagram

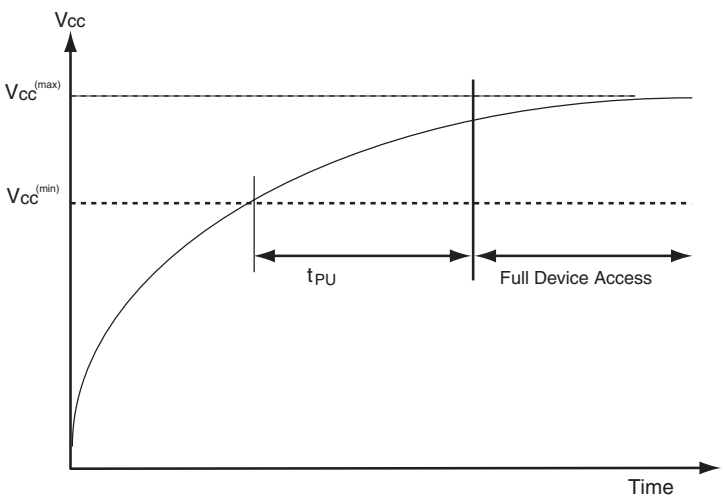


Figure 9.2 Power-down and Voltage Drop

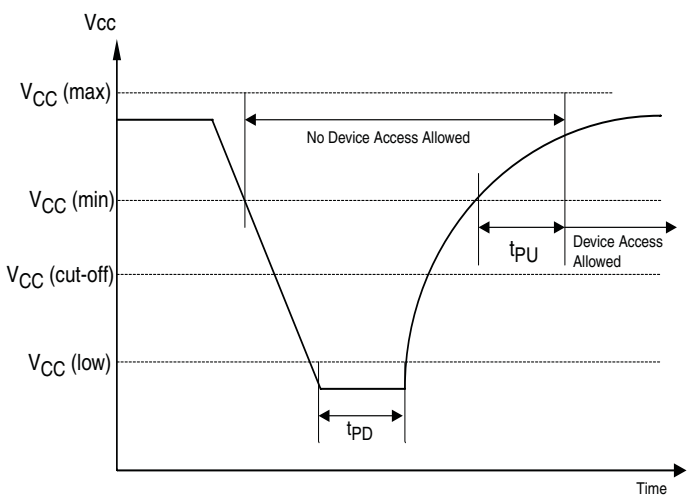


Table 9.1 Power-Up / Power-Down Voltage and Timing

Symbol	Parameter	Min	Max	Unit
$V_{CC(min)}$	V_{CC} (minimum operation voltage)	2.7		V
V_{CC}(cut-off)	V_{CC} (Cut off where re-initialization is needed)	2.4		V
V_{CC}(low)	V_{CC} (Low voltage for initialization to occur at read/standby) V_{CC} (Low voltage for initialization to occur at embedded)	0.2 2.3		V
t_{PU}	V_{CC}(min.) to device operation	300		µs
t_{PD}	V_{CC} (low duration time)	1.0		µs

10. Initial Delivery State

The Configuration Register contains 00h (all bits are set to 0).

11. Electrical Specifications

11.1 Absolute Maximum Ratings

Description	Rating
Ambient Storage Temperature	-65°C to +150°C
Voltage with Respect to Ground: All Inputs and I/Os	-0.5V to V_{CC}+0.5V
Output Short Circuit Current (Note 2)	200 mA

Note

1. *Minimum DC voltage on input or I/Os is -0.5V. During voltage transitions, inputs or I/Os may undershoot GND to -2.0V for periods of up to 20 ns. See Figure 11.1. Maximum DC voltage on input or I/Os is V_{CC} + 0.5V. During voltage transitions inputs or I/Os may overshoot to V_{CC} + 2.0V for periods up to 20 ns. See Figure 11.2.*
2. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
3. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

Figure 11.1 Maximum Negative Overshoot Waveform

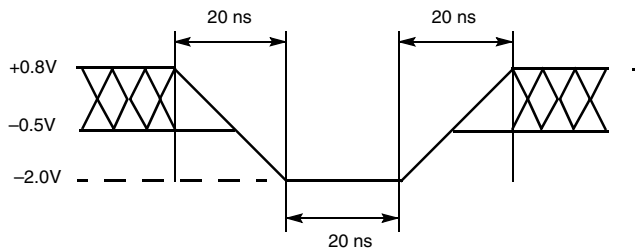
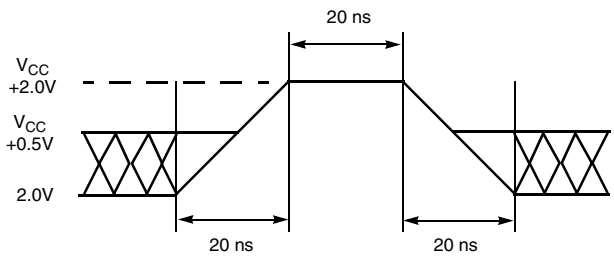


Figure 11.2 Maximum Positive Overshoot Waveform



12. Operating Ranges

Table 12.1 Operating Ranges

Description		Rating
Ambient Operating Temperature (T_A)	Industrial	–40°C to +85°C
Positive Power Supply	Voltage Range	2.7V to 3.6V

Note

Operating ranges define those limits between which functionality of the device is guaranteed.

13. DC Characteristics

This section summarizes the DC Characteristics of the device. Designers should check that the operating conditions in their circuit match the measurement conditions specified in the Test Specifications in Table 14.1 on page 30, when relying on the quoted parameters.

Table 13.1 DC Characteristics (CMOS Compatible)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ*	Max	
V_{CC}	Supply Voltage		2.7		3.6	V
V_{IL}	Input Low Voltage		-0.3		0.3 x V_{CC}	V
V_{IH}	Input High Voltage		0.7 x V_{CC}		V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = V_{CC} min.			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.1 mA	V_{CC}-0.6			V
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND			±2	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or GND			±2	µA
I_{CC1}	Active Power Supply Current - READ (SO = Open)	At 80 MHz (Dual or Quad)			38	mA
		At 104 MHz (Serial)			25	
		At 40 MHz (Serial)			12	
I_{SB1}	Standby Current	CS# = V_{CC}; SO + V_{IN} = GND or V_{CC}		80	200	µA
I_{PD}	Deep Power-down Current	CS# = V_{CC}; SO + V_{IN} = GND or V_{CC}		3	10	µA

*Typical values are at T_{AI} = 25°C and V_{CC} = 3V

14. Test Conditions

Figure 14.1 AC Measurements I/O Waveform

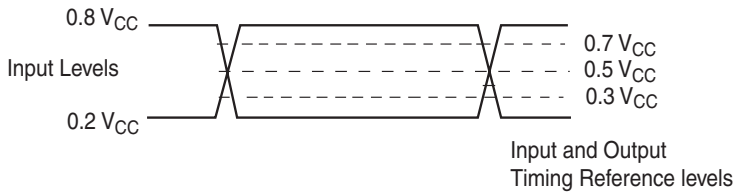


Table 14.1 Test Specifications

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltage	0.2 V_{CC} to 0.8 V_{CC}		V
	Input Timing Reference Voltage	0.3 V_{CC} to 0.7 V_{CC}		V
	Output Timing Reference Voltage	0.5 V_{CC}		V

15. AC Characteristics

Figure 15.1 AC Characteristics (Sheet 1 of 2)

Symbol (Notes)	Parameter (Notes)	Min. (Notes)	Typ (Notes)	Max (Notes)	Unit
f_R	SCK Clock Frequency for RDID and READ command	DC		40	
f_C	SCK Clock Frequency for all others: FAST_READ, DP, RES, READ_ID	DC		104 (serial) 80 (dual/quad)	MHz
t_{WH}, t_{CH}	Clock High Time (4)	4.5			ns
t_{WL}, t_{CL}	Clock Low Time (4)	4.5			ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1			V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1			V/ns
t_{CS}	CS# High Time (Read Instructions)	10			ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3			ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3			ns
$t_{SU:DAT}$	Data in Setup Time	3			ns
$t_{HD:DAT}$	Data in Hold Time	2			ns
t_V	Clock Low to Output Valid	0		8 (Serial)Δ 9.5 (Dual/Quad)Δ 6.5 (Serial)∞ 8 (Dual/Quad)∞ 7 (Dual/Quad)Ω	ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			8	ns
t_{HLCH}	HOLD# Active Setup Time (relative to SCK)	3			ns
t_{CHHH}	HOLD# Active Hold Time (relative to SCK)	3			ns
t_{HHCH}	HOLD# Non Active Setup Time (relative to SCK)	3			ns
t_{CHHL}	HOLD# Non Active Hold Time (relative to SCK)	3			ns
t_{HZ}	HOLD# enable to Output Invalid			8	ns

Figure 15.1 AC Characteristics (Sheet 2 of 2)

Symbol (Notes)	Parameter (Notes)	Min. (Notes)	Typ (Notes)	Max (Notes)	Unit
t_{LZ}	HOLD# disable to Output Valid			8	ns
t_{RES}	Deep Power-down to Standby Mode			30	µs
t_{DP}	Time to enter Deep Power-down Mode			10	µs

Notes

1. *∆ Full Vcc range (2.7 – 3.6V) & CL = 30 pF*
2. *∞ Regulated Vcc range (3.0 – 3.6V) & CL = 30 pF*
3. *Ω Regulated Vcc range (3.0 – 3.6V) & CL = 15 pF*
4. *t_{WH} + t_{WL} must be less than or equal to $1/f_C$.*

15.1 Capacitance

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance (applies to SCK, PO7-PO0, SI, CS#)	V_{OUT} = 0V		6	pF
C_{OUT}	Output Capacitance (applies to PO7-PO0, SO)	V_{IN} = 0V		8	pF

Figure 15.2 SPI Mode 0 (0,0) Input Timing

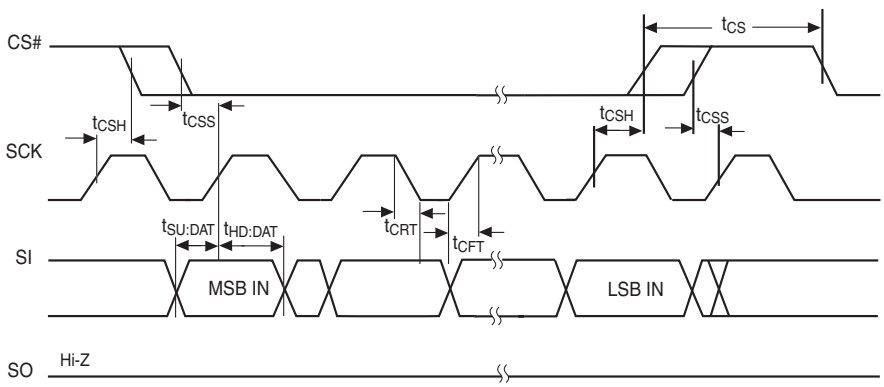


Figure 15.3 SPI Mode 0 (0,0) Output Timing

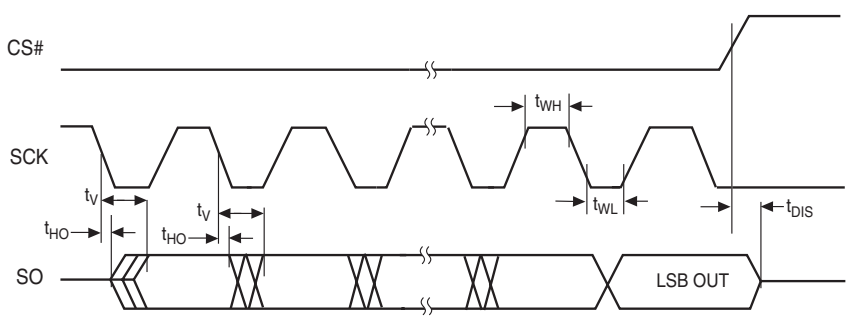
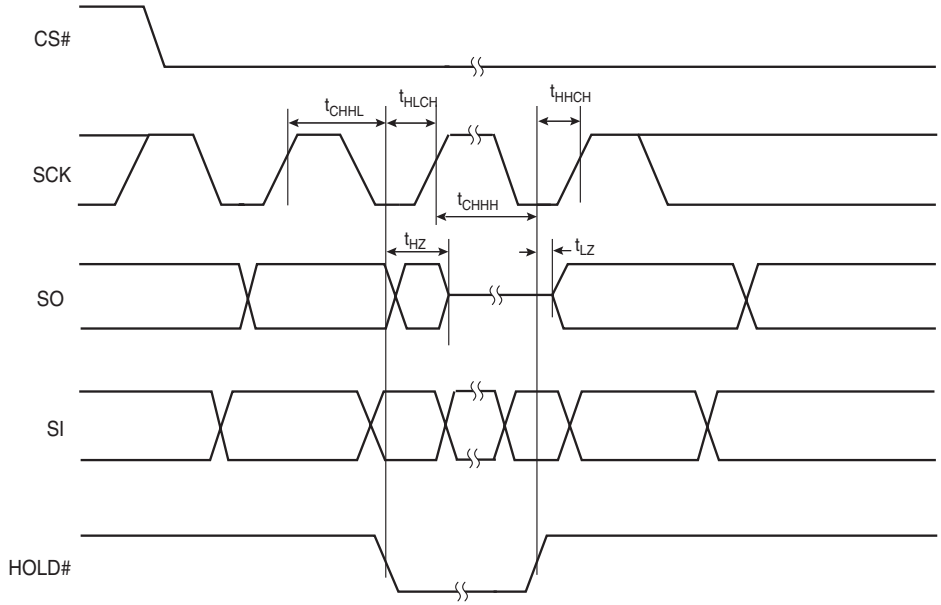
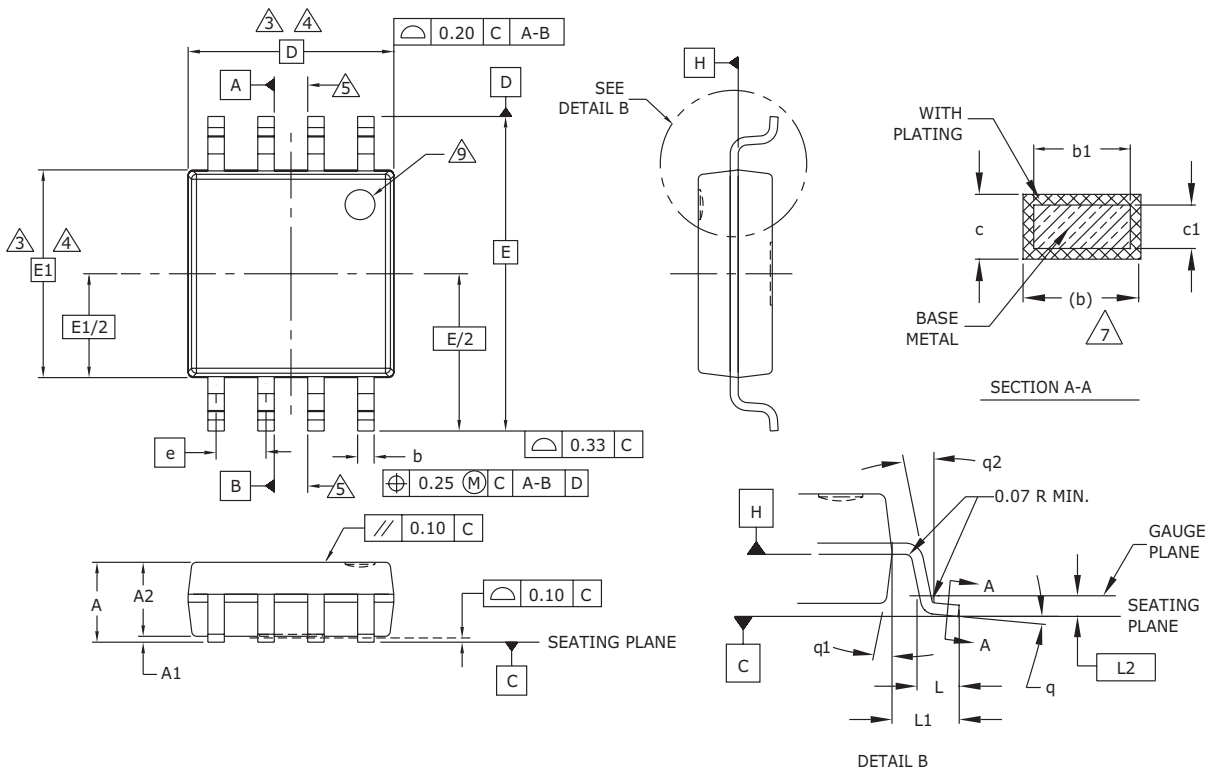


Figure 15.4 HOLD# Timing



16. Physical Dimensions

16.1 SOC008 wide — 8-pin Plastic Small Outline Package (208-mils Body Width)



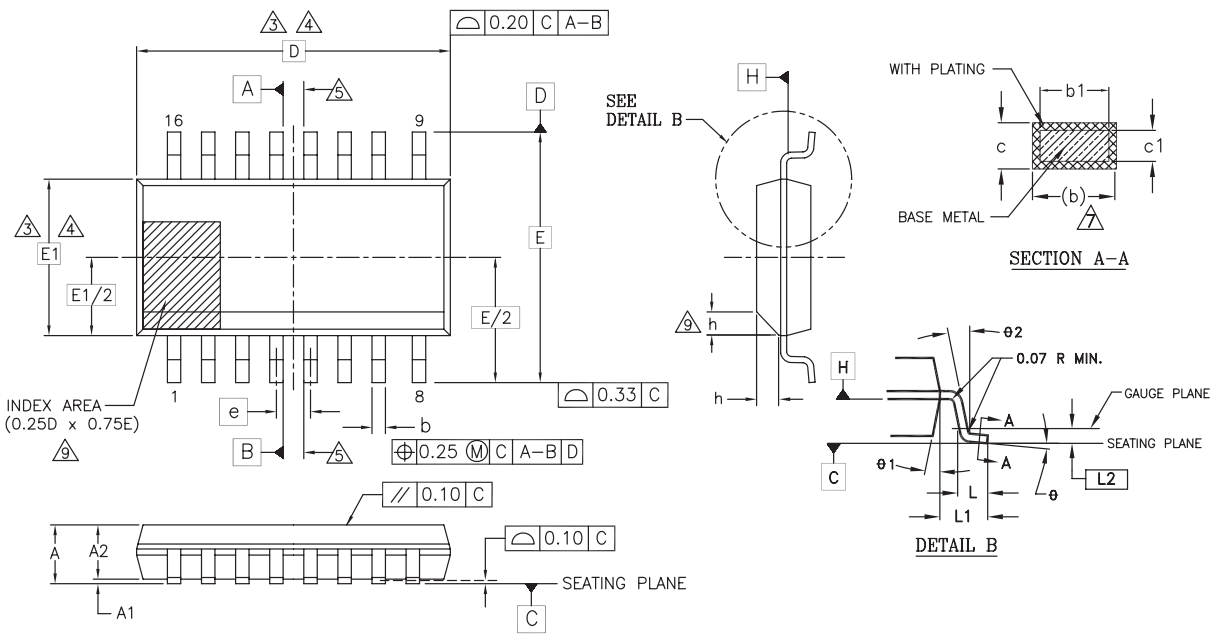
PACKAGE	SOC 008 (inches)		SOC 008 (mm)	
JEDEC				
SYMBOL	MIN	MAX	MIN	MAX
A	0.069	0.085	1.753	2.159
A1	0.002	0.0098	0.051	0.249
A2	0.067	0.075	1.70	1.91
b	0.014	0.019	0.356	0.483
b1	0.013	0.018	0.330	0.457
c	0.0075	0.0095	0.191	0.241
c1	0.006	0.008	0.152	0.203
D	0.208 BSC		5.283 BSC	
E	0.315 BSC		8.001 BSC	
E1	0.208 BSC		5.283 BSC	
e	.050 BSC		1.27 BSC	
L	0.020	0.030	0.508	0.762
L1	.055 REF		1.40 REF	
L2	.010 BSC		0.25 BSC	
N	8		8	
θ	0°	8°	0°	8°
θ1	5°	15°	5°	15°
θ2	0°		0°	

NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

3432 \ 16-038.03 \ 10.28.04

16.2 SO3 016 — 16-pin Wide Plastic Small Outline Package (300-mil Body Width)



PACKAGE	SO3 016 (inches)		SO3 016 (mm)	
JEDEC	MS-013(D)AA		MS-013(D)AA	
SYMBOL	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.081	0.104	2.05	2.55
b	0.012	0.020	0.31	0.51
b1	0.011	0.019	0.27	0.48
c	0.008	0.013	0.20	0.33
c1	0.008	0.012	0.20	0.30
D	0.406 BSC		10.30 BSC	
E	0.406 BSC		10.30 BSC	
E1	0.295 BSC		7.50 BSC	
e	.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
L1	.055 REF		1.40 REF	
L2	.010 BSC		0.25 BSC	
N	16		16	
h	0.10	0.30	0.25	0.75
θ	0°	8°	0°	8°
θ1	5°	15°	5°	15°
θ2	0°		0°	

NOTES:

1. ALL DIMENSIONS ARE IN BOTH INCHES AND MILLMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH. BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

3601 \ 16-038.03 \ 8.31.6

17. Revision History

Section	Description
Revision 01 (July 16, 2009)	
	Initial release.
Revision 02 (August 5, 2009)	
Distinctive Characteristics	Corrected description of Single power supply operation
Read Identification (RDID)	Corrected description
Deep Power-Down	Corrected description
AC Characteristics	Corrected Table for SCK Clock Frequency for RDID command

Colophon

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