Standard Products

UT54ALVC2525 RadHard Clock Driver
1 to 8 Minimum Skew

Advanced Data Sheet
September 7, 2006

AEROFLEX
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FEATURES

- 2.0V to 3.6V Power supply operation
- Output-output skew <100 ps
- Guaranteed pin-to-pin and part-to-part skew
- Eight LVTTL outputs with high drive strength
- Radiation performance
  - Total-dose tolerance: 100 to 300 krad(Si,) or 1 Mrad(Si)
  - SEL Immune to a LET of 109 MeV-cm^2/mg
- Military temperature range: -55^{o}C to +125^{o}C
- Packaging options:
  - 14-Lead Ceramic Flatpack
- Standard Microcircuit Drawing: 5962-06233
  - QML-Q and QML-V compliant part

INTRODUCTION

The UT54ALVC2525 is a low-voltage, minimum skew, one-to-eight clock driver. The UT54ALVC2525 distributes a single clock to eight, high-drive, outputs with low skew across all outputs during both the t_{PLH} and t_{PHL} transitions making it ideal for signal generation and clock distribution. The output pins act as a single entity and will follow the state of the CLK pin.

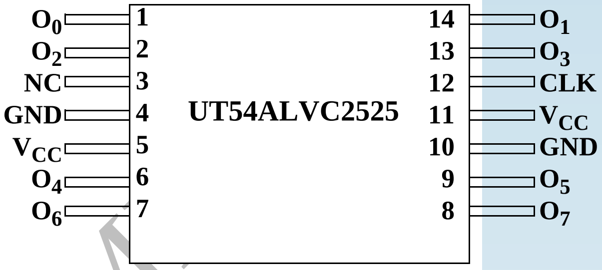


Figure 2. 14-Lead Ceramic Flatpack Pinouts

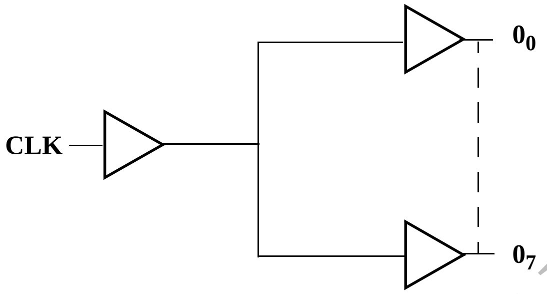


Figure 1: UT54ALVC2525 Block Diagram

PIN DESCRIPTION

Flatpack Pin No.	Name	I/O	Type	Description
12	CLK	I	LVTTL	Primary reference clock input. This pin must be driven by an LVTTL or LVCMOS clock source.
3	N/C	--	--	No connect.
1, 2, 6, 7, 8, 9, 13, 14	O_n	O	LVTTL	Eight output clocks.
5, 11	V_{DD}	PWR	Power	Power supply for internal circuitry and output buffers.
4, 10	V_{SS}	PWR	Power	Ground

RADIATION HARDNESS

The UT54ALVC2525 incorporates special design, layout, and process features which allows operation in a limited radiation environment.

Parameter	Limit	Units
Total Ionizing Dose (TID)	>1E6	rads(Si)
Single Event Latchup (SEL) [1, 2]	>109	MeV-cm^2/mg
Onset Single Event Upset (SEU) LET Threshold [3, 4]	>109	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2
Dose Rate Upset	TBD	rads(Si)/sec
Dose Rate Survivability	TBD	rads(Si)/sec

Notes:

1. The UT54ALVC2525 is latchup immune to particle LETs >109 MeV-cm^2/mg.
2. SEL temperature and voltage conditions of T_C = +125°C, V_{DD} = 3.6V.
3. SEU worst case temperature and voltage conditions of T_C = +25°C, V_{DD} = 3.0V.
4. For the UT54ALVC2525 SET performance at select operating frequency data ranges, please contact the factory.

ABSOLUTE MAXIMUM RATINGS:[1]

(Referenced to V_{SS})

Symbol	Description	Limits	Units
V_{DD}	Core Power Supply Voltage	-0.3 to 4.0	V
V_{IN}	Voltage Any Clock Input	-0.3 to V_{DD} + 0.3	V
V_{OUT}	Voltage Any Clock Output	-0.3 to V_{DD} + 0.3	V
I_I	DC Input Current	±10	mA
P_D	Maximum Power Dissipation	TBD	W
T_{STG}	Storage Temperature	-65 to +150	°C
T_J	Maximum Junction Temperature [2]	+150	°C
Θ_{JC}	Thermal Resistance, Junction to Case	20	°C/W
ESD_{HBM}	ESD Protection (Human Body Model) - Class II	>3000	V

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.

RECOMMENDED OPERATING CONDITIONS:

Symbol	Description	Limits	Units
V_{DD}	Core Operating Voltage	2.0 to 3.6	V
V_{IN}	Voltage Clock Input	0 to V_{DD}	V
V_{OUT}	Voltage Any Clock Output	0 to V_{DD}	V
T_C	Case Operating Temperature	-55 to +125	°C

DC OUTPUT ELECTRICAL CHARACTERISTICS (Pre- and Post-Radiation)*
(V_{DD} = 2.0V to 3.6V; T_C = -55°C to +125°C)

Symbol	Description	Conditions	V_{DD}	Min.	Max.	Units
V_{IH}[1]	High level input voltage		2.0V 2.75V 3.0V 3.6V	1.25 1.5 1.75 2.0		V
V_{IL}[1]	Low level input voltage		2.0V 2.75V 3.0V 3.6V		0.7 0.8 0.8 0.8	V
V_{OL}	Low level output voltage	I_{OL} = 12mA I_{OL} = 12mA I_{OL} = 12mA I_{OL} = 12mA	2.0V 2.75V 3.0V 3.6V		0.4 0.4 0.4 0.4	V
V_{OH}	High level output voltage	I_{OH} = -12mA I_{OH} = -12mA I_{OH} = -12mA I_{OH} = -12mA	2.0V 2.75V 3.0V 3.6V	1.6 2.2 2.4 3.0		V
I_{OS}[2]	Short-circuit output current	V_{OUT} = V_{DD} and V_{SS}	2.0V 3.6V	-300 -600	300 600	mA
I_{IL}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	3.6V	-1	1	µA
I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}				
	Pre-Rad 25°C		2.0V	2.0	mA	mW/MHz
	Pre-Rad -55°C to +125°C			TBD	mA	mW/MHz
	Post-Rad 25°C			TBD	mA	mW/MHz
	Pre-Rad 25°C		3.6V	4.0	mA	mW/MHz
	Pre-Rad -55°C to +125°C			TBD	mA	mW/MHz
	Post-Rad 25°C			TBD	mA	mW/MHz
P_{TOTAL}	Total power dissipation	C_L = 50pF	2.0V 2.75V 3.0V 3.6V		1 2 2.5 3.75	mW/MHz
C_{IN}[4]	Input capacitance	f = 1MHz	0V		15	pF
C_{OUT}[4]	Output capacitance	f = 1MHz	0V		15	pF

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to a TID level of 1.0E6 rad(Si).
1. Functional tests are conducted in accordance with MIL-STD-883 with the following test conditions: V_{IH}=V_{IH}(min) +20%, -0% V_{IL}=V_{IL}(max)+0%, -50%, as specified herein for the LVTTL and LVCMOS inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min), V_{IL} (max).
2. Supplied as a design limit. Neither guaranteed nor tested.
3. When measuring the dynamic supply current, all outputs are loaded in accordance with the equivalent test load defined in figure 3.
4. Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and the VSS at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.

AC OUTPUT ELECTRICAL CHARACTERISTICS (Pre- and Post-Radiation)*

(V_{DD} = 2.0V to 3.6V; T_C = -55°C to +125°C) **(Note 1, 2)**

Description	Condition	V_{DD}	Mi		
Input rise/fall time	V_{IH} (min) - V_{IL} (max)	3.6V			
Propagation delay: CLK to On, high-to-low transition	Measured as transition time between $V_{IN} = V_{DD}÷2$ to $V_{OUT} = V_{DD}÷2$	2.0V 2.75V 3.0V 3.6V	3. 3. 2.7 2.2		
Propagation delay: CLK to On, low-to-high transition	Measured as transition time between $V_{IN} = V_{DD}÷2$ to $V_{OUT} = V_{DD}÷2$	2.0V 2.75V 3.0V 3.6V	3.2 2.7 2. 2.		
Maximum skew: common edge, output-to-output, low-to-high transition		2.0V 2.75V 3.0V 3.6V		0.7 0.55 0.55 0.5	ns
Maximum skew: common edge, output-to-output, high-to-low transition		2.0V 2.75V 3.0V 3.6V		0.7 0.55 0.55 0.5	ns
Output rise/fall time	Measured as transition time between 20% * V_{DD} and 80% * V_{DD}	2.0V 3.6V	1.0 0.75	2.0 1.5	ns
Part-part skew	Skew between the outputs of any two devices under identical settings and conditions (V_{DD}, temp, air flow, frequency, etc).	2.0V 3.6V		0.75 0.50	ns
Propagation delay balance: difference between same output, low-to-high and high-to-low transitions	Measured as transition time between $V_{IN} = V_{DD}÷2$ to $V_{OUT} = V_{DD}÷2$	2.0V 2.75V 3.0V 3.6V		0.75 0.5 0.35 0.3	ns
Maximum skew: opposite edge, output-to-output variation	Measured as transition time between $V_{IN} = V_{DD}÷2$ to $V_{OUT} = V_{DD}÷2$	2.0V 2.75V 3.0V 3.6V		0.5 0.25 0.18 0.1	ns

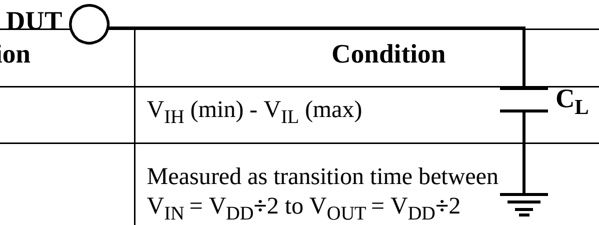


Figure 3.
Output Test Load Circuit Dynamic Power Supply Current Measurements

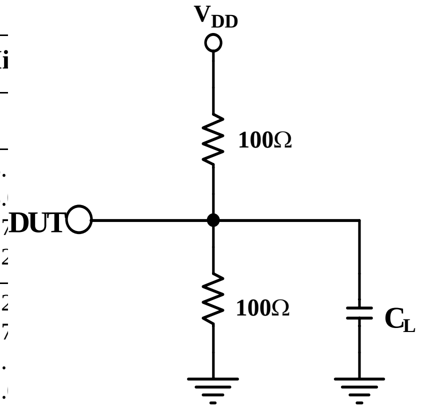


Figure 4.
Clock Output AC Test Load Circuit

Note: This is not the recommended termination for normal user operation.

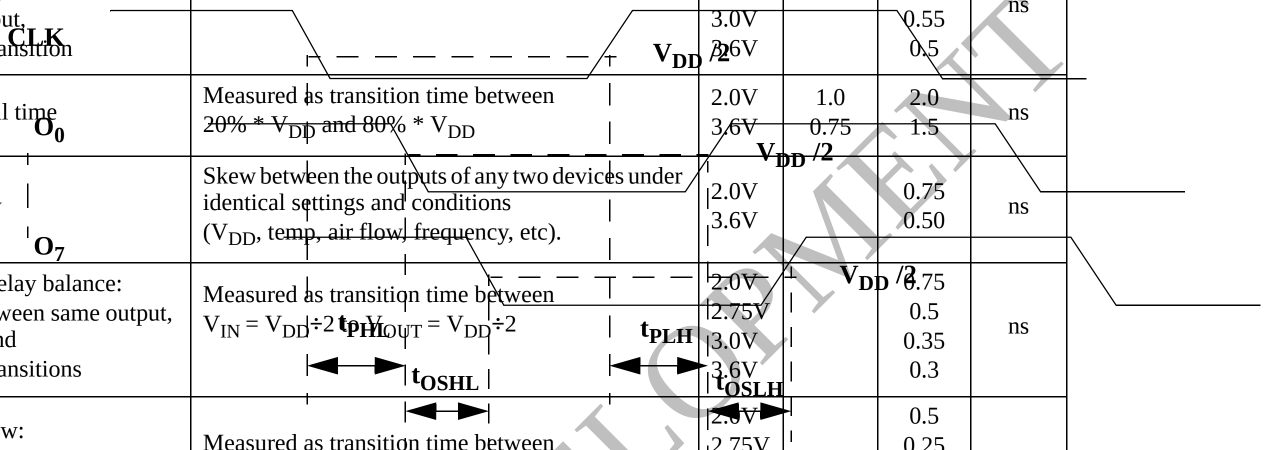
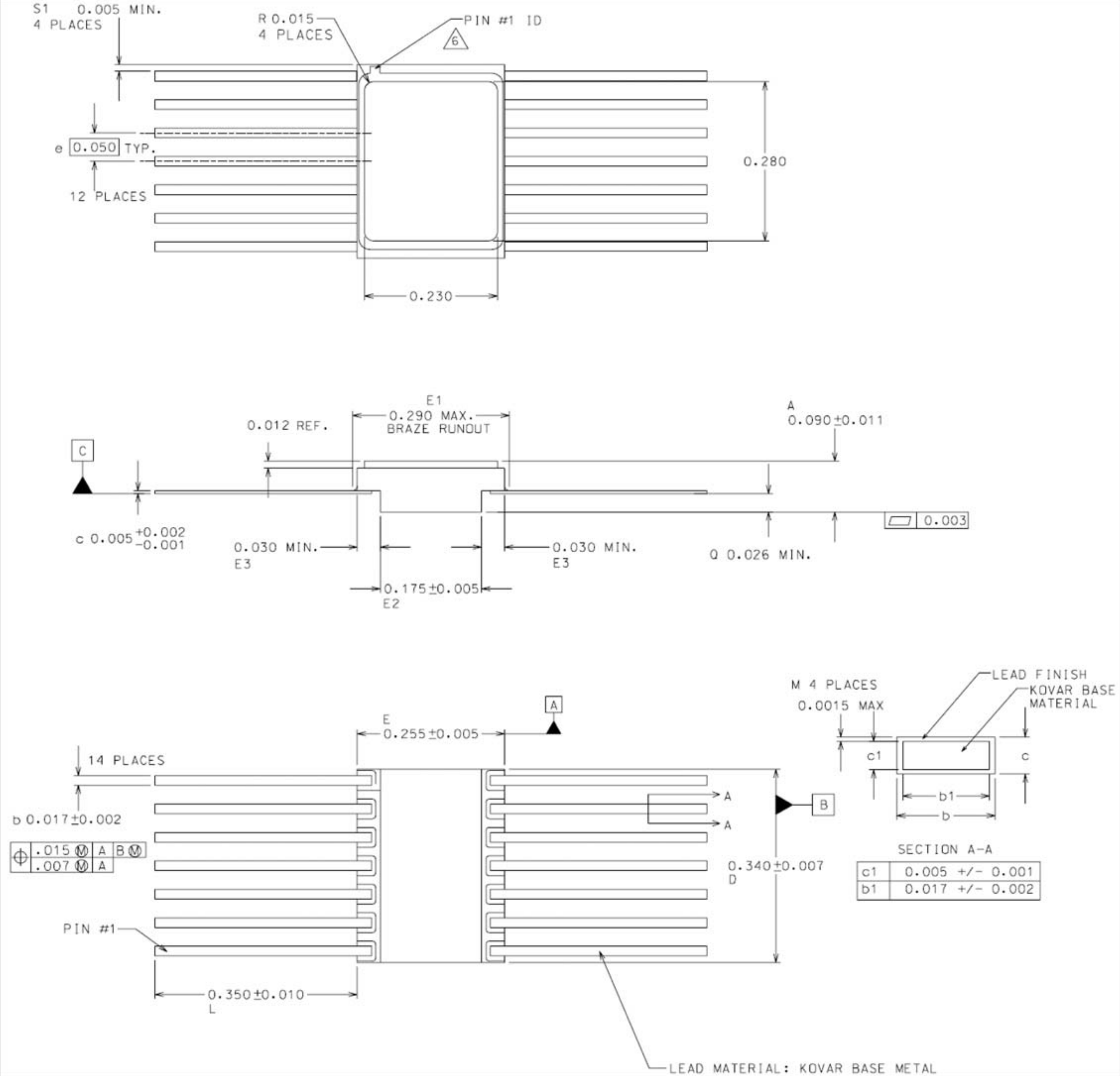


Figure 5. AC Timing Diagram

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to a TID level of 1.0E6 rad(Si).
1. Test load = 40pF, terminated to $V_{DD}÷2$. All outputs are equally loaded. Reference figure 4 for clock output loading that is equivalent to the load circuit used for all AC testing.
2. Reference Figures 5 and 6 for AC timing diagrams.
3. Supplied only as a design guideline, neither tested nor guaranteed.
4. Guaranteed by characterization, but not tested.

PACKAGING



1. All exposed metallized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbol is in accordance with MIL-PRF-38533.
5. Lead position and colanarity are not measured.
6. ID mark symbol is vendor option.

Figure 6. 14-Pin Flatpack Package

ORDERING INFORMATION

UT54ALVC2525:

UT54ALVC2525 - * * *

Lead Finish (Notes 1 & 2):
(A) = Hot solder dipped
(C) = Gold
(X) = Factory option (gold or solder)

Screening (Notes 3,4,5)
(C) = Military Temperature Range flow (-55°C to +125°C)
(P) = Prototype flow

Package Type:
(U) = 14-Lead Ceramic Flatpack

Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an “X” is specified when ordering, then the part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Prototype flow per Aeroflex Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.
5. Extended Industrial Temperature Range Flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -40°C, room temp, and +125°C. Radiation is neither tested nor guaranteed.

UT54ALVC2525: SMD

5962 * 06233 ** * * *

Lead Finish (Notes 1 & 2):
(A) = Hot solder dipped
(C) = Gold
(X) = Factory Option (gold or solder)

Case Outline:
(X) = 14-Lead Ceramic Flatpack

Class Designator:
(Q) = QML Class Q
(V) = QML Class V

Device Type:
(01) = UT54ALVC2525

Drawing Number:
06233

Total Dose: (Note 3)
(-) = No Radiation Guarantee
(R) = 1E5 rads(Si)
(F) = 3E5 rads(Si)
(G) = 5E5 rads(Si)
(H) = 1E6 rads(Si)

Federal Stock Class Designator: No options

Notes:
1.Lead finish (A,C, or X) must be specified.
2.If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3.Total dose radiation must be specified when ordering. QML Q and QML V are not available without radiation hardening.

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