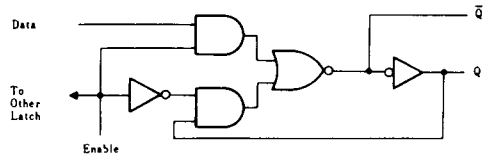
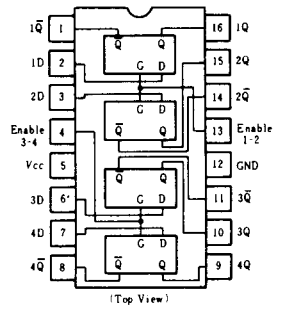
HD74LS75 ●Quadruple Bistable Latches

The HD74LS75 is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data(D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high. This device features complementary Q and $\overline{Q}$ outputs from a 4-bit latch.

■BLOCK DIAGRAM(¼)



■PIN ARRANGEMENT



■FUNCTION TABLE

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
×	L	Q_0	$\overline{Q}_0$

Notes) H; high level, L; low level, X; irrelevant
Q_0; level of Q before the indicated steady-state input conditions were established.
$\overline{Q}_0$; complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established.

■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Pulse width	t_w	20	–	–	ns
Setup time	t_{su}	15	–	–	ns
Hold time	t_h	5	–	–	ns

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	–	–	0.4	V
			$I_{OL}=8mA$	–	–	0.5	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$	D input	–	–	20	μA
			G input	–	–	80	
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$	D input	–	–	−0.4	mA
			G input	–	–	−1.6	
	I_I	$V_{CC}=5.25V$, $V_I=7V$	D input	–	–	0.1	mA
			G input	–	–	0.4	
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current **	I_{CC}	$V_{CC}=5.25V$		–	6.3	12	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

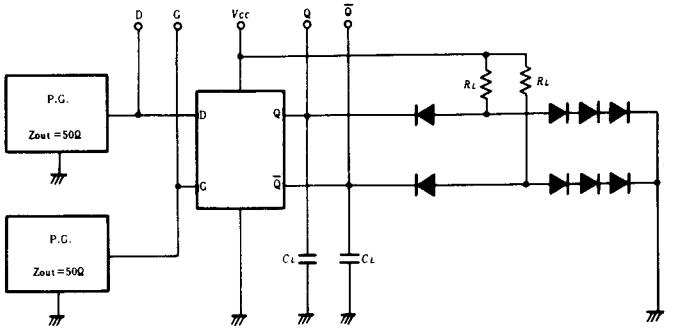
* $V_{CC}=5V$, $Ta=25°C$
** I_{CC} is measured with all outputs open and all inputs grounded.

■SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃)

Item	Symbol	Input	Output	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	D	Q	C_L=15pF, R_L=2kΩ	–	15	27	ns
	t_{PHL}				–	9	17	
	t_{PLH}	D	$\overline{Q}$		–	12	20	ns
	t_{PHL}				–	7	15	
	t_{PLH}	G	Q		–	15	27	ns
	t_{PHL}				–	14	25	
	t_{PLH}	G	$\overline{Q}$		–	16	30	ns
	t_{PHL}				–	7	15	

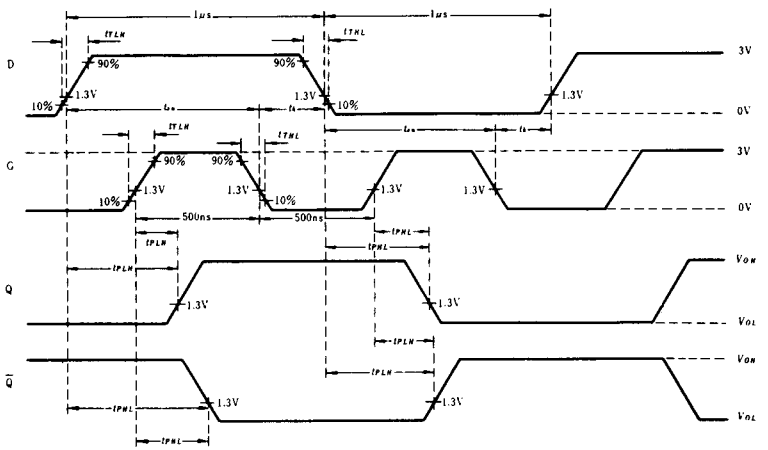
■TESTING METHOD

1) Test Circuit



Notes) 1. Test is put into the each latch
2. All diodes are 1S2074 Ⓗ.
3. C_L includes probe and jig capacitance.

Waveform



Notes) 1. Input pulse; D input; PRR=500kHz, G input; PRR=1MHz, $t_{THL} \leqq 10$ns, $t_{TLH} \leqq 10$ns.
2. When measuring propagation delay times from the D input, the corresponding G input must be held high.

PACKAGING INFORMATIONS

T-90-20

Factory orders for circuits described in this databook should include a three-part type number as explained in the following example.

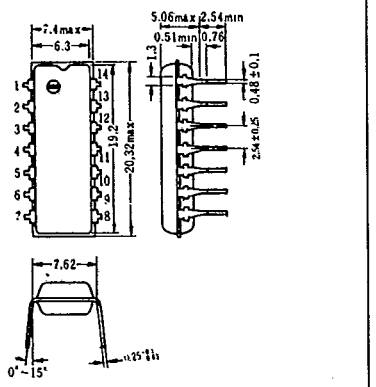
HD 74LS00 P

- Package ; Plastic DIP ; letters P
  Cerdip ; non-letters
- Circuit description
- Prefix : HD ; Hitachi Digital IC

■Plastic DIP

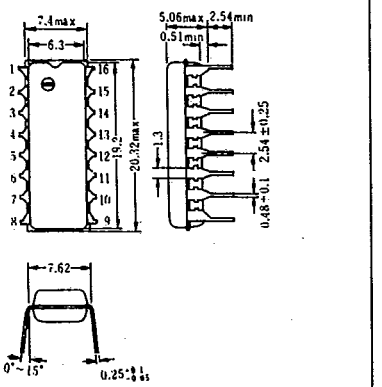
●14 Pin

DP-14



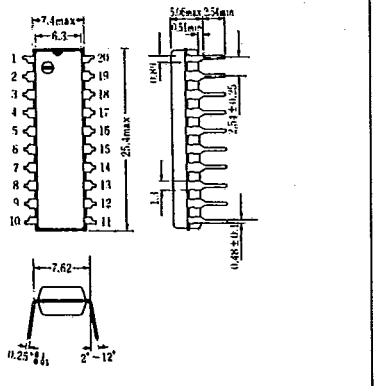
●16 Pin

DP-16



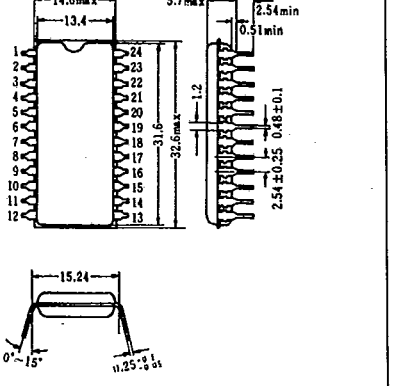
●20 Pin

DP-20



●24 Pin

DP-24

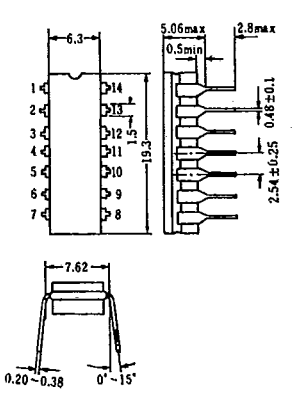


PACKAGING INFORMATIONS

■Cerdip

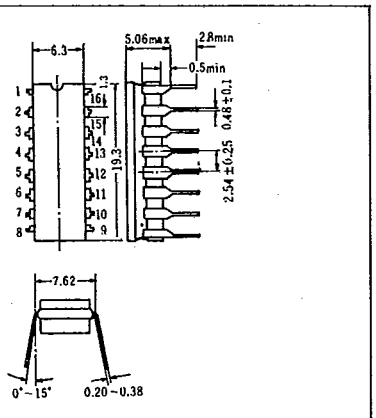
●14 Pin

DG-14



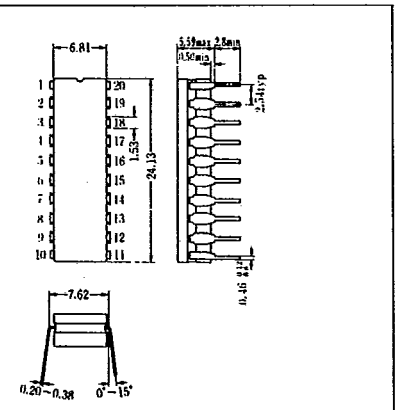
●16 Pin

DG-16



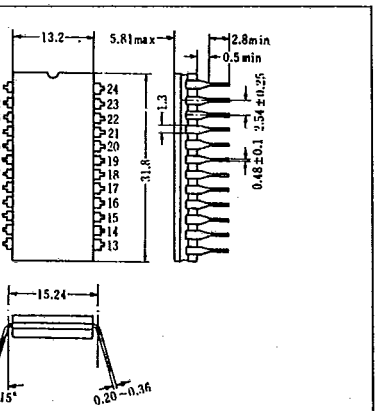
●20 Pin

DG-20



●24 Pin

DG-24



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