SIERRA SEMICONDUCTOR

SQ3265
V.32bis, Modem Sound Combo with AccuSound™ SpeakerPhone Chip Set

SQ3265 V.32bis, Modem Sound Combo with AccuSound™ SpeakerPhone Chip Set

FEATURES

Compatibility

- Sound Blaster 16™, Sound Blaster Pro™, Sound Blaster™ software compatible
- Windows™ Sound System 2.0
- MPU401 MIDI (UART mode)
- Windows COM port driver
- Windows OLE

Concurrency

- Complete interoperability of Sound Blaster (Pro, 16), Speakerphone, MIDI, .WAV, Data, Fax

Sound

- 8/16 bit, mono/stereo recording and playback of digital audio
- Stereo FM synthesis (OPL3)
- Stereo Wave Table Synthesis (OPL4)
- 5 kHz to 45 kHz sampling rates
- Mixes CD, SoundBlaster, FM modem audio, microphone and line inputs
- 32-level volume control for master, digital, FM audio
- Bass and treble tone control
- Direct headphone drive

Speakerphone/Voice

- AccuSound™ Full-Duplex Speakerphone with DSP echo cancellation
- Voice-Data protocol—Radish™ VoiceView™
- Voice Mail mode with compression down to 14.4k bit/s
- Voice sampling rates of 4.8, 7.2, 8, 9.6, and 11k samples/s.
- Sierra 2.3x Voice Commands
- Integrated DMA interface for Voice Mail and MCI wave interface
- Distinctive ring detection
- Caller ID
- Record speakerphone mode
- Music on hold

Plug and Play Autoconfiguration

- Plug and Play (PnP) ISA revision 1.0a compatible
- PnP Legacy systems ready
- PnP BIOS systems ready
- Windows 95 ready

I/O

- MIDI, MPU-401 (UART mode)
- Joystick, Software configurable fast or slow
- Enhanced IDE CD-ROM interface
- Integrated 16C550 UART direct PC bus interface

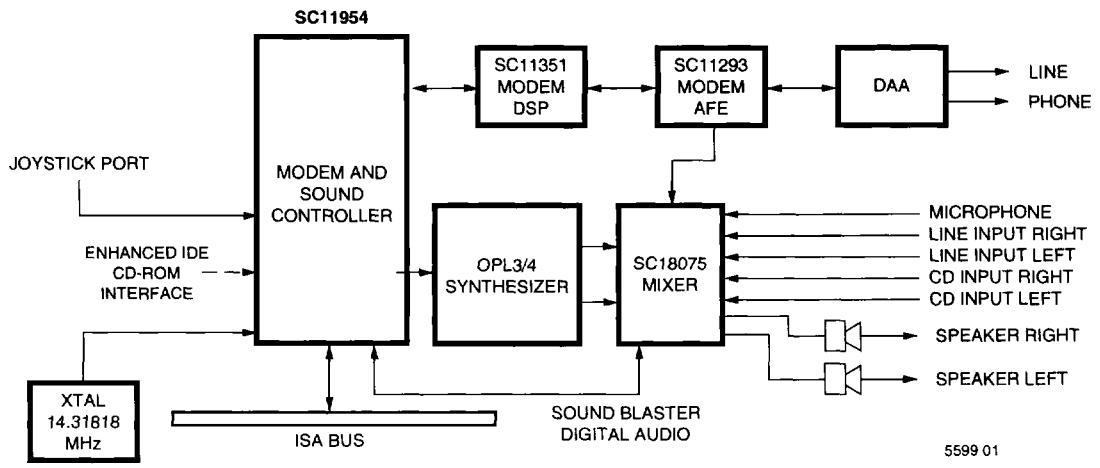
DATA

- Data Modes: ITU-T (formerly CCITT) V.32bis, V.32, V.22bis, V.22, V.21, V.23 Bell 212A and 103
- Data Rates: 57,600 to 300 bit/s
- "AT" Command set
- Error Control: MNP 2-4 and V.42
- Data Compression: MNP 5 and V.42bis
- T.I.E.S. (Time Independent Escape Sequence)

FAX

- Fax Modes: ITU-T V.17, V.33, V.29, V.27ter., V.21 (Channel 2)
- Class 1 and 2 Fax Interface
- 14,400 to 2400 bit/s
- 5 volt CMOS technology

BLOCK DIAGRAM



GENERAL DESCRIPTION

The Sierra SQ3265 V.32bis chipset is a highly integrated multimedia modem design. Sound Blaster software compatibility, FM, and wave table synthesis are combined with Accusound Speakerphone and Modem capabilties. This design allows modem manufacturers to build a high performance, fully featured Sound Blaster software compatible, Speaker-Phone, Fax, Data and Voice Mail modem with differentiation, and a minimum design effort for their customers.

The SQ3265 offers the end user complete SB-16, MIDI, .WAV, speakerphone, data, and fax concurrency—all the hottest features in a single integrated system.

The chip set also provides full Plug & Play support, allowing jumperless configuration of interrupts, DMA, COM port & I/O space requirements for both modem and sound functions. The chip set is compatible with the Plug & Play ISA specification revision 1.0A.

The SQ3265 is a modem chip set that will operate over General Switched Telephone Network (GSTN) two-wire full duplex lines. It supports all commonly used ITU-T (International Telecommunications Unit-Telecommunications (formerly CCITT)) and Bell data modes from 14,400 bits/s to 300 bit/s. It also supports the ITU-T V.42bis compression protocol that can deliver data at speeds up to 57,600 bits/s. V.17 Group III facsimile supports data at 14,400, 12,000, 9,600, 7,200, 4,800 and 2,400 bits/s.

The Full-Duplex SpeakerPhone uses AccuSound technology Acoustic Echo Cancellation (AEC) and Electrical Echo Cancellation (EEC) to allow a conference quality (non-speakerphone sounding) conversation. Flash-hook, hold transfer, mute, programmable speaker volume and microphone gain, AGC, redial, and memory dial are all supported. Music-on-hold and conversation record options are available through the mixer.

The SQ3265 Chip Set also supports multiple voice-mail modes. Voice can be compressed down to 14.4 Kbps using Sierra's CVSD voice compression. Linear and Mu-Law voice modes are also supported. The linear voice mode allows .WAV files to be played through the modem without any compression/decompression required. Mu-Law mode will compress 12 bit samples into 8 bits, retaining 12 bit voice quality. Extensive support for multiple sampling rates is provided (4.8, 7.2, 8, 9.6, 11k samples/s). The lower sampling rates provide an alternative to compression for reducing disk space/channel bandwidth requirements. 8k s/s gives access to industry standard voice compression, speech to text, and speech recognition technology. 11k s/s is available for the commonly used Business Audio format .WAV files.

The SQ3265 Chip Set is supported with Sierra's extensive "AT" command set that now includes the Sierra 2.3x Voice commands. Controller firmware is available in compilable form allowing memory size to be matched to the feature set.

The SQ3265 consists of the SC11954 (208 pin PQFP) advanced modem and sound controller, the SC18075 (68 pin PLCC) mixer, the SC11293 (44 pin PQFP) Analog Front End, and the SC11351 (80 pin PQFP) Digital Signal Processor. All parts have a TQFP option.

SC11954 SOUND CONTROLLER

The SC11954 is a modem and sound controller which enables multimedia modem platforms based on Sierra's V.32bis chip. The chip sets Sound Blaster™ software compatibility and FM and wave table synthesis are combined with speakerphone, voice mail, fax, data, and business audio with minimal component and cost addition. The SC11954 also provides full Plug & Play support, allowing jumperless configuration of interrupts, DMA, COM port & I/O space requirements for both modem and sound functions. The chip fully supports the Plug & Play ISO specification revision 1.0A.

Pin Descriptions

Pin #	Pin Name	Pin Type	Input Class	Output Drive	PU/PD	Description
			External RAM/ROM Peripheral Interface			
42	$\overline{\text{CSRAM}}$	DO		4mA		Chip select for external RAM (Address from 0300H to 7FFFH)
41	$\overline{\text{CSROM}}$	DO		4mA		Chip select for external ROM (Address from 8000H to FFFFH)
111	MA0	DO		4mA		Address bus for external program/data access (bit 0)
109	MA1	DO		4mA		Address bit 1
107	MA2	DO		4mA		Address bit 2
105	MA3	DO		4mA		Address bit 3
104	MA4	DO		4mA		Address bit 4
102	MA5	DO		4mA		Address bit 5
100	MA6	DO		4mA		Address bit 6

Pin Descriptions (continued)

Pin #	Pin Name	Pin Type	Input Class	Output Drive	PU/PD	Description
99	MA7	DO		4mA		Address bit 7
97	MA8	DO		4mA		Address bit 8
96	MA9	DO		4mA		Address bit 9
95	MA10	DO		4mA		Address bit 10
94	MA11	DO		4mA		Address bit 11
93	MA12	DO		4mA		Address bit 12
92	MA13	DO		4mA		Address bit 13
91	MA14	DO		4mA		Address bit 14
90	MA15	DO		4mA		Address bit 15
89	MA16	DO		4mA		Address bit 16
120	AD0	DIO	CMOS	4mA	PU	Bidirectional data bus (8-bit) bit
119	AD1	DIO	CMOS	4mA	PU	Bidirectional data bus (8-bit) bit
118	AD2	DIO	CMOS	4mA	PU	Bidirectional data bus (8-bit) bit
117	AD3	DIO	CMOS	4mA	PU	Bidirectional data bus (8-bit) bit
116	AD4	DIO	CMOS	4mA	PU	Bidirectional data bus (8-bit) bit
115	AD5	DIO	CMOS	4mA	PU	Bidirectional data bus (8-bit) bit
114	AD6	DIO	CMOS	4mA	PU	Bidirectional data bus (8-bit) bit
113	AD7	DIO	CMOS	4mA	PU	Bidirectional data bus (8-bit) bit
39	$\overline{\text{DSPCS}}$	DO		4mA		DSP chip select (Address 200H to 25FH)
33	$\overline{\text{RD}}$	DO		4mA		Peripheral read select (Active low, data valid on rising edge of pulse)
43	$\overline{\text{WR}}$	DO		4mA		Peripheral write select (Active low, data valid on rising edge of pulse)
			Modem Analog Processor Interface			
70	RX	DI	TTL		PU	Serial data received from modem
69	TDOUT	DO		4mA		Serial data to be transmitted by modem
71	SOUT	DO		4mA		Serial data to be transmitted to modem
72	SIN	DI	CMOS			Serial data received from DTE
79	INTTST	DI	TTL			Modem external input interrupt (Detected on low to high transition)
				Clocks		
17	XTAL1	DI				14.31818 MHz crystal oscillator input
18	XTAL2	DO				14.31818 MHz crystal oscillator output
29	DSPCLK	DO		4mA		Buffered clock output for modem DSP
14	FMCLK	DO		2mA ‡		Buffered XTAL output for OPL3
78	$\overline{\text{CLKPD}}$	DI	CMOS		PU	Clock oscillator & PLL power down
			Relay, DAA, and Modem Control			
75	KDV	DO		4mA		Data/voice relay control (High signal indicates voice relay is closed and modem is in voice mode)
74	OH	DO		4mA		Off-hook control (High signal indicates that DAA should go off-hook)
76	$\overline{\text{RI}}$	DI	CMOS Schmitt			Ring indicator (Low signal indicates that modem is receiving a ringing signal)
77	$\overline{\text{RLSD}}$	DO		12mA		Carrier detect output
15	$\overline{\text{MDMPD}}$	DO		8mA		Modem power-down mode (active low, open drain)
			General Purpose I/O			
88	IO0	DIO	TTL	4mA	PU	General purpose I/O port bit 0
87	IO1	DIO	TTL	4mA	PU	General purpose I/O port bit 1
86	IO2	DIO	TTL	4mA	PU	General purpose I/O port bit 2
85	IO3	DIO	TTL	4mA	PU	General purpose I/O port bit 3
84	IO4	DIO	TTL	4mA	PU	General purpose I/O port bit 4
83	IO5	DIO	TTL	4mA	PU	General purpose I/O port bit 5
82	IO6	DIO	TTL	4mA	PU	General purpose I/O port bit 6
81	IO7	DIO	TTL	4mA	PU	General purpose I/O port bit 7
			ISA Bus Interface			
170	PCA0	DI	TTL			PC address bus bit 0
171	PCA1	DI	TTL			PC address bus bit 1
172	PCA2	DI	TTL			PC address bus bit 2
173	PCA3	DI	TTL			PC address bus bit 3
174	PCA4	DI	TTL			PC address bus bit 4
175	PCA5	DI	TTL			PC address bus bit 5
177	PCA6	DI	TTL			PC address bus bit 6
178	PCA7	DI	TTL			PC address bus bit 7
179	PCA8	DI	TTL			PC address bus bit 8
180	PCA9	DI	TTL			PC address bus bit 9
181	PCA10	DI	TTL			PC address bus bit 10
182	PCA11	DI	TTL			PC address bus bit 11
135	IRQ15	DO		12mA		PC Interrupt 15
136	IRQ12	DO		12mA		PC Interrupt 12

Pin Descriptions (continued)

Pin #	Pin Name	Pin Type	Input Class	Output Drive	PU/PD	Description
137	IRQ11	DO		12mA		PC Interrupt 11
138	IRQ10	DO		12mA		PC Interrupt 10
140	IRQ7	DO		12mA		PC Interrupt 7
141	IRQ5	DO		12mA		PC Interrupt 5
142	IRQ4	DO		12mA		PC Interrupt 4
143	IRQ3	DO		12mA		PC Interrupt 3
144	IRQ2	DO		12mA		PC Interrupt 2
128	DREQ0	DO		12mA		PC DMA Request 0 (8-bit DMA)
121	$\overline{\text{DACK0}}$	DI	TTL			PC DMA Acknowledge 0 (8-bit DMA)
129	DREQ1	DO		12mA		PC DMA Request 1 (8-bit DMA)
122	$\overline{\text{DACK1}}$	DI	TTL			PC DMA Acknowledge 1 (8-bit DMA)
130	DREQ3	DO		12mA		PC DMA Request 3 (8-bit DMA)
123	$\overline{\text{DACK3}}$	DI	TTL			PC DMA Acknowledge 3 (8-bit DMA)
131	DREQ5	DO		12mA		PC DMA Request 5 (16-bit DMA)
124	$\overline{\text{DACK5}}$	DI	TTL			PC DMA Acknowledge 5 (16-bit DMA)
132	DREQ6	DO		12mA		PC DMA Request 6 (16-bit DMA)
125	$\overline{\text{DACK6}}$	DI	TTL			PC DMA Acknowledge 6 (16-bit DMA)
133	DREQ7	DO		12mA		PC DMA Request 7 (16-bit DMA)
127	$\overline{\text{DACK7}}$	DI	TTL			PC DMA Acknowledge 7
67	PCD0	DIO	Schmitt	24mA ‡		PC data bus bit 0
66	PCD1	DIO	Schmitt	24mA ‡		PC data bus bit 1
65	PCD2	DIO	Schmitt	24mA ‡		PC data bus bit 2
64	PCD3	DIO	Schmitt	24mA ‡		PC data bus bit 3
63	PCD4	DIO	Schmitt	24mA ‡		PC data bus bit 4
62	PCD5	DIO	Schmitt	24mA ‡		PC data bus bit 5
61	PCD6	DIO	Schmitt	24mA ‡		PC data bus bit 6
60	PCD7	DIO	Schmitt	24mA ‡		PC data bus bit 7
59	PCD8	DIO	Schmitt	24mA ‡		PC data bus bit 8
55	PCD9	DIO	Schmitt	24mA ‡		PC data bus bit 9
53	PCD10	DIO	Schmitt	24mA ‡		PC data bus bit 10
52	PCD11	DIO	Schmitt	24mA ‡		PC data bus bit 11
50	PCD12	DIO	Schmitt	24mA ‡		PC data bus bit 12
48	PCD13	DIO	Schmitt	24mA ‡		PC data bus bit 13
46	PCD14	DIO	Schmitt	24mA ‡		PC data bus bit 14
44	PCD15	DIO	Schmitt	24mA ‡		PC data bus bit 15
37	$\overline{\text{PCIOR}}$	DI	Schmitt			PC I/O read strobe (Active low)
38	$\overline{\text{PCIOW}}$	DI	Schmitt			PC I/O write strobe (Active low)
183	PCAEN	DI	TTL			PC address enable
188	PCTC	DI	TTL			PC DMA Terminal Count
			SC18075 Mixer Interface			
169	MIXLR	DO		4mA		Mixer L/R clock
164	DACCLK	DO		4mA		Mixer DAC data clock
163	DACDATA	DO		4mA		Mixer DAC serial data
165	ADCCLK	DO		4mA		Mixer ADC data clock
167	ADCDATA	DI	CMOS			Mixer ADC serial data
162	MIXFCLK	DO		4mA		Mixer filter clock (10.584 MHz)
146	$\overline{\text{MIXWR}}$	DO		4mA		Mixer write strobe
148	MIXRS	DO		4mA		Mixer register/data select
147	$\overline{\text{MIXCS}}$	DO		4mA		Mixer chip select
149	MIXD0	DO		4mA	PU	Mixer data bus bit 0
150	MIXD1	DO		4mA	PU	Mixer data bus bit 1
151	MIXD2	DO		4mA	PU	Mixer data bus bit 2
152	MIXD3	DO		4mA	PU	Mixer data bus bit 3
156	MIXD4	DO		4mA	PU	Mixer data bus bit 4
157	MIXD5	DO		4mA	PU	Mixer data bus bit 5
159	MIXD6	DO		4mA	PU	Mixer data bus bit 6
161	MIXD7	DO		4mA	PU	Mixer data bus bit 7
			MIDI Interface			
30	MIDIN	DI	TTL		PU	MIDI data input
31	MIDOUT	DO		4mA		MIDI data output
			PnP E²PROM Interface			
7	EECS	DO		4mA		PnP E²PROM chip select
5	EECLK	DO		4mA		PnP E²PROM serial clock
1	EEDI	DI	CMOS		PU	PnP E²PROM serial data in
3	EEDO	DO		4mA		PnP E²PROM serial data out
			Enhanced IDE Interface			
203	$\overline{\text{IDECSA}}$	DO		12mA		IDE chip select A
202	$\overline{\text{IDECSB}}$	DO		12mA		IDE chip select B
206	$\overline{\text{IDEWR}}$	DO		12mA		Buffered ISA I/O write strobe
204	$\overline{\text{IDERD}}$	DO		12mA		Buffered ISA I/O read strobe

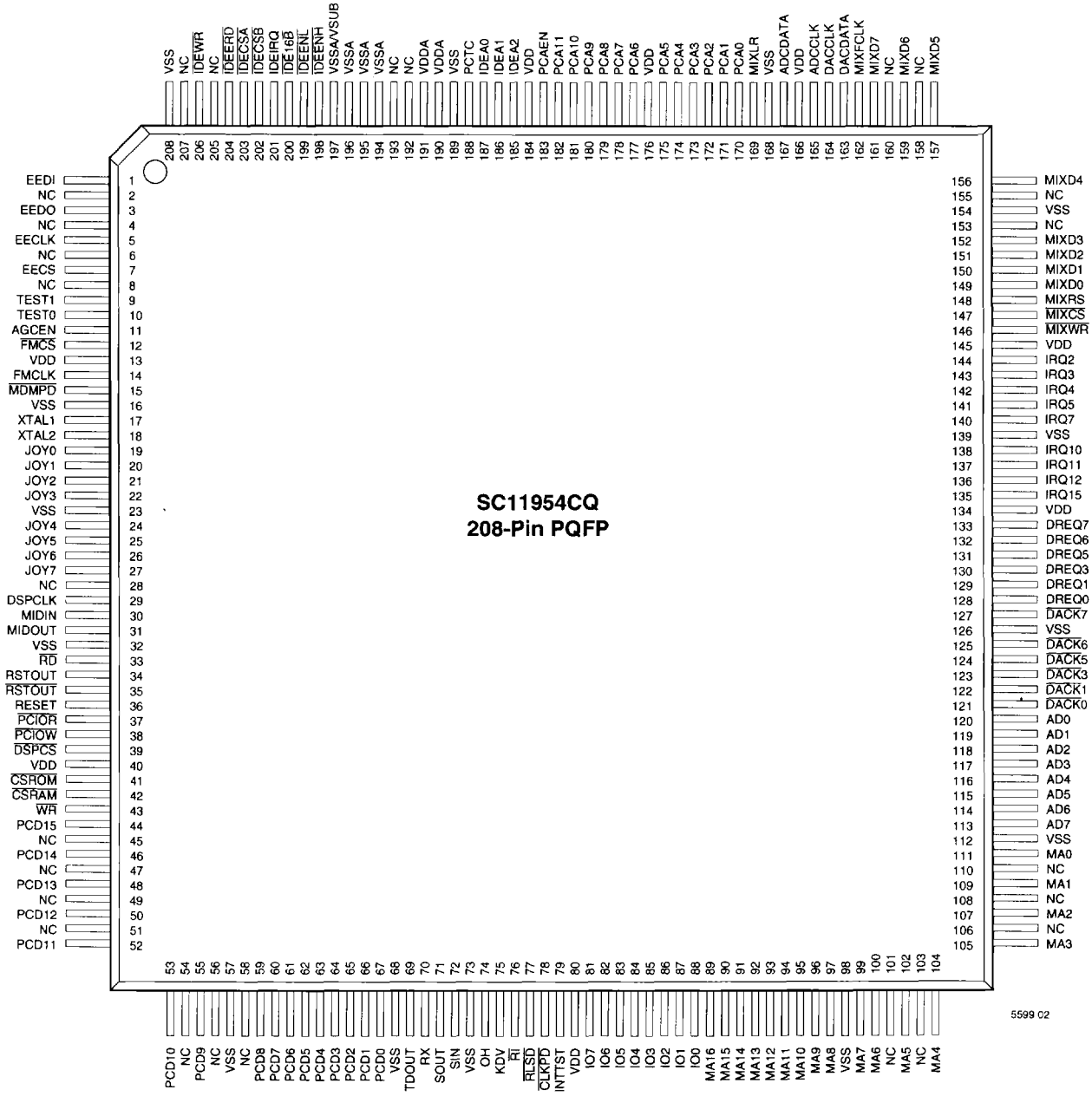
Pin Descriptions (continued)

Pin #	Pin Name	Pin Type	Input Class	Output Drive	PU/PD	Description
187	IDEA0	DO		12mA		Buffered ISA Address bit 0
186	IDEA1	DO		12mA		Buffered ISA Address bit 1
185	IDEA2	DO		12mA		Buffered ISA Address bit 2
201	IDEIRQ	DI	Schmitt		PD	IDE interrupt
200	$\overline{\text{IDE16B}}$	DI	Schmitt		PU	IDE 16 bit enable
199	$\overline{\text{IDEENL}}$	DO		8mA		IDE low byte external buffer enable
198	$\overline{\text{IDEENH}}$	DO		8mA		IDE high byte external buffer enable
			Joystick Interface			
19	JOY0	AI	Analog			Joystick position input #1
20	JOY1	AI	Analog			Joystick position input #2
21	JOY2	AI	Analog			Joystick position input #3
22	JOY3	AI	Analog			Joystick position input #4
24	JOY4	AI	TTL		PU (5K)	Joystick button input #1
25	JOY5	AI	TTL		PU (5K)	Joystick button input #2
26	JOY6	AI	TTL		PU (5K)	Joystick button input #3
27	JOY7	AI	TTL		PU (5K)	Joystick button input #4
			Other Pins			
36	RESET	DI	TTL			Chip reset
34	RSTOUT	DO		4mA		Buffered reset output
35	$\overline{\text{RSTOUT}}$	DO		12mA		Buffered inverted reset output
12	$\overline{\text{FMCS}}$	DO		4mA		OPL3/4 chip select
11	AGCEN	DO		4mA		AGC enable (0=ON, 1=OFF)
			No Connect, Power, Ground			
2	NC					No Connect
4	NC					No Connect
6	NC					No Connect
8	NC					No Connect
28	NC					No Connect
45	NC					No Connect
47	NC					No Connect
49	NC					No Connect
51	NC					No Connect
54	NC					No Connect
56	NC					No Connect
58	NC					No Connect
101	NC					No Connect
103	NC					No Connect
106	NC					No Connect
108	NC					No Connect
110	NC					No Connect
153	NC					No Connect
155	NC					No Connect
158	NC					No Connect
160	NC					No Connect
192	NC					No Connect
193	NC					No Connect
205	NC					No Connect
207	NC					No Connect
13	VDD	PWR				Digital power
40	VDD	PWR				Digital power
80	VDD	PWR				Digital power
134	VDD	PWR				Digital power
145	VDD	PWR				Digital power
166	VDD	PWR				Digital power
176	VDD	PWR				Digital power
184	VDD	PWR				Digital power
9	VSS	GND				Digital ground
10	VSS	GND				Digital ground
16	VSS	GND				Digital ground
23	VSS	GND				Digital ground
32	VSS	GND				Digital ground
57	VSS	GND				Digital ground
68	VSS	GND				Digital ground
73	VSS	GND				Digital ground
98	VSS	GND				Digital ground
112	VSS	GND				Digital ground
126	VSS	GND				Digital ground
139	VSS	GND				Digital ground
154	VSS	GND				Digital ground
168	VSS	GND				Digital ground

Pin Descriptions (continued)

Pin #	Pin Name	Pin Type	Input Class	Output Drive	PU/PD	Description
189	VSS	GND				Digital ground
208	VSS	GND				Digital ground
190	VDDA	PWR				Analog power
191	VDDA	PWR				Analog power
194	VSSA	GND				Analog ground
195	VSSA	GND				Analog ground
196	VSSA	GND				Analog ground
197	VSSA/VSUB	GND				Analog ground

Connection Diagram



NOTE: Pinout subject to change without notice.

GENERAL CHIP DESCRIPTION SC11954 SOUND CONTROLLER

The SC11954 controller will provide address decoding, data buffering and a DMA channel for the modem. It provides Sound Blaster 16 command interpretation for the sound functions and an interface to the SC18075 mixer/ADC/DAC. In addition, the SC11954 provides Plug and Play auto-configuration feature which eliminates the necessity for jumpers and DIP switches.

The SC11954 controller consists of 7 blocks:

- Modem Controller and UART
- PC ISA Bus Interface
- Sound Blaster 16 Emulation
- Mixer/ADC/DAC Interface
- Clock Synthesizer
- Plug and Play Auto-configuration
- Enhanced IDE Interface

MODEM CONTROLLER AND UART

Internal Processor

The CPU contains a processor which executes a subset of the Intel 8096 instruction set. The processor consists of a microcontrol PLA and a 16-bit registered arithmetic/logic unit (RALU). The microcontrol PLA accepts as input 8096 instruction opcodes and generates the control sequences necessary to implement the instructions. The RALU is a bit=slice processor that performs instruction execution, operand address calculation, jump address calculation, program sequencing, and stack control. The program counter (PC) and stack pointer (SP) are contained within the RALU. The 16-bit output of the RALU goes onto either an 8-bit data bus or a 16-bit address bus.

Interrupts

The CPU contains a 16-input vectored interrupt structure. For each interrupt input, there is an enable bit and a pending bit. When a vectored interrupt occurs, the internal processor will respond to the interrupt with the highest priority, and jump to its corresponding vector address. The hardware will automatically reset the pending bit. After the interrupt is serviced, the internal processor will respond to the next highest interrupt, and so on. If the user does not wish to use vectored interrupts, the user can poll the pending bits, or poll the sources that generates the interrupts directly.

Registers

The CPU contains a 384-byte RAM. The stack is contained inside the RAM, which the PLA initializes the stack pointer to 140H (320D). The first page of the RAM (000H-0FFH) can be accessed through direct or indirect addressing mode. The second page of RAM (100H-17FH) must use indirect addressing mode.

There are hardware registers in the CPU, UART Interface, and UART blocks. These registers are all 8-bit registers and must be accessed via indirect addressing mode. For complete information on SC11954 internal modem registers, please refer to the SC11951 data sheet.

External Memory Interface

The external memory interface consists of a 16-bit address bus (MA16-MA0), 8-bit data bus (AD7-AD0), select lines (/CSROM, /CSRAMB, or /DSPCS), read line (/RD), and write line (/WR). The default memory access is 3-cycle and can be switched to 2-cycle by setting GCR1.1, which is the FASTMEM bit. The entire external memory space is writeable and instructions can be executed from anywhere inside the external memory space.

The external ROM space is 32K (8000H-FFFFH). MA16 (GCR1.7) and MA15 (GCR1.6) are used to create 4 banks of 32K ROM spaces for a total of 128K ROM space.

The external RAM space is 31.25K (0300H-7FFFH). When the RAM32K downbond is grounded, the RAM space is restricted to 16K (4000H-7FFFH).

The external peripheral space is 256 bytes (0200H-02FFH).

Clock Generation

The modem controller operates at 39.3216 MHz or 49.1520 MHz. The default XTAL setting is 39.3216 MHz and can be switched to 49.1520 MHz by setting GCR1.0, the FREQSEL bit. This bit ensures that the timer operates at 9.8304 MHz and the base clock of the baud rate generator operates at 1.8432 MHz. CLKOUT is a buffered version of the crystal frequency (X1). The internal system clock (CP) operates at half the crystal frequency (X1/2).

UART Interface

General Features

The SC11954 contains FIFOs to facilitate high data throughput for the CPU. The FIFOs are 4 bytes deep, one holds send data for the UART, the other holds receive data from the UART. The FIFOs are incorporated in order to decrease the interrupt rate to the CPU. The data flow in parallel mode is opposite that of the serial mode. In order to minimize the differences between serial and parallel mode controller code, the UART can be configured to present a consistent send/receive interface to the controller.

Send FIFO Operation

The SFIFO holds up to 4 bytes of data that the CPU is sending to the host. The data is serialized at a rate controlled by the UART MCR and routed to either the UART Receive Shift Register (RSR) or the UART serial output. The SFIFO has the following features:

- The depth of the SFIFO ensures that as many as 4 characters can be transferred when the CPU services the SFIFO_empty interrupt. This effectively buffers the CPU transfer rate from the serial data rate.
- The SFIFO depth allows the CPU to load 4 characters each time it switches context to the service routine. This reduces the impact of the CPU time lost in context switching.

Receive FIFO Operation

The RFIFO holds up to 4 bytes of data that has been received from the host. The data is received from either the UART Tx FIFO or the UART RSR. The RFIFO has the following features:

- The depth of the RFIFO ensures that as many as 4 characters will be ready to transfer when the CPU services the RFIFO_threshold interrupt.
- The program can select the number of bytes required in the RFIFO (1, 2, 3, or 4) before the UART_interface issues an interrupt. This allows the software to modify the interrupt trigger levels depending on its current task or loading. It also ensures that the CPU doesn't continually waste time switching context for only a few characters.
- The RFIFO will hold 4 bytes regardless of which trigger level the CPU selects. This makes allowances for a variety of CPU latency times, as the FIFO continues to fill after the interrupt is issued.

Direct UART Interface / UART Shadow Interface

All communication between the UART and CPU is supposed to be through the send and read FIFO, but a hardware interface exists which enables the CPU to directly communicate with the '550 UART registers through the '550 UART data bus. Also, a "shadow" data bus exists to provide read and write access to some of the '550 UART registers without having to disturb the '550 UART data bus.

UART

General Features

The SC11954 contains a 16C550-compatible UART, which includes FIFOs, to facilitate high data throughput for the external host. The UART is dual-ported, as the CPU can access it through a direct UART interface and the host can access it through the PC bus interface. The FIFOs are 16 bytes deep – one holds data for the transmitter, the other for the receiver. The FIFOs are incorporated in order to decrease the interrupt rate to the host. The FIFOs differ in their customization for either transmitter or receiver functions. Each has support circuitry to minimize software overhead when handling interrupts. The receiver optimizes the CPI/UART data transaction via the following features:

- The depth of the receiver (Rx) FIFO ensures that as many as 16 characters will be ready to transfer when the CPU services the Rx interrupt. Therefore, the CPU transfer rate is effectively buffered from the serial data rate.
- The program can select the number of bytes required in the Rx FIFO (1, 4, 8, or 14) before the UART issues and interrupt. This allows the software to modify the interrupt trigger levels depending on its current task or loading. It also ensures that the CPU doesn't continually waste time switching context for only a few characters.
- The Rx FIFO will hold 16 bytes regardless of which trigger level the CPU selects. This makes allowances for a variety of CPU latency times, as the FIFO continues to fill after the interrupt is issued.

  The transmitter optimizes the CPU/UART data transaction via the following features:

- The depth of the transmitter (Tx) FIFO ensures that as many as 16 characters can transferred when the CPU services the Tx interrupt. Once again, this effectively buffers the CPU transfer rate from the serial data rate.
- The transmitter (Tx) FIFO depth allows the CPU to load 16 characters each time it switches context to the service routine. This reduces the impact of the CPU time lost in context switching.
- Since a time lag in servicing an asynchronous transmitter usually has no penalty, CPU latency time is of no concern to transmitter operation.

Tx FIFO Operation

The Tx portion of the UART transmits data through SOUT as soon as the CPU loads a byte into the Tx FIFO. The UART will prevent loads to the Tx FIFO if it currently holds 16 characters. Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The SC11954 issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO, the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this

byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UARTs interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. Therefore, after the first byte has been loaded into the FIFO, the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt.

This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx FIFO Operation

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time, if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the overrun error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having an Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. To prevent the software from having to check for this situation, the SC11954 incorporates a timeout interrupt.

The timeout interrupt is activated when there is at least one byte in the Rx FIFO and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

AUTOBAUD Operation

The autobaud circuitry enables the UART to automatically detect and set the incoming baud rate up to 115.2 kbaud.

Modem Voice DMA

NOTE: The two registers 0x27E and 0x27F do not repeat in the range 278H to 27DH.

Reserved registers (278 - 27D)

Voice DMA Control register (27E)

This register is the control/status register for voice mode DMA operation. This register allows the modem controller to initiate a DMA request and monitor DMA busy status. All bits in the register are set to zero by chip RESET. Following bits are defined –

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	EODMA	IRQEN	REQEN	BUSY	DREQ

DREQ Modem controller sets this read/write bit to 1 to initiate a DMA cycle. It is reset by SC11954 on the leading edge of DACK signal from PC.

BUSY This read-only bit is set to 1 when the DREQ or DACK signal is active. The modem controller can monitor this bit to decide when the DMA cycle is complete.

REQEN The modem controller sets this read/write bit to 1 to enable the the DREQ output driver. 0 places it in Hi Z state.

IRQEN The modem controller sets this read/write bit to 1 to enable the DMA IRQ output driver. 0 places it in Hi Z state.

EODMA This read/write bit is set to 1 when the TC signal from the PC signals end of DMA block. This bit remains set until cleared by the modem controller (by writing 0 to it).

Voice DMA Data register (27F)

This register is used for sending or receiving voice mode DMA data to and from the PC.

Memory

The external ROM space is 32K (8000H-FFFFH). Pins MA16 (GCR1.7) and MA15 (GCR1.6) can be used to create 4 banks of 32K ROM spaces for a total of 128K addressable ROM space.

The SC11954 memory map is shown below:

Internal RAM	(384Bytes)	0000 017F
Register	(128 Bytes)	0180 01FF
Peripheral	(256 Bytes)	0200 02FF
External RAM	(31.25K Bytes)	0300 7FFF
External ROM	(32K Bytes)	8000 FFFF

The Peripheral address space maps to the /DSPCS pin.

The External RAM address space maps to the /CSRAM pin.

The External ROM address space maps to the /CSROM pin.

Low Power Mode

The modem controller also has a low power mode. This mode runs the modem controller on an internal RC oscillator at a rate of roughly 2 MHz while exerting the open drain active low output MDMPD.

PC INTERFACE

The PC Interface is designed to provide a glueless interface between the modem/Sound Blaster and the PC. The functions are defined below.

PC Data Transceiver

The PC data transceiver provides isolation between the PC data bus and the internal PC data bus used in the SC11954. Direction of the transceiver is controlled by IOR/ signal from the PC. When IOR/ is high, transceiver becomes an input port passing data from the PC bus to SC11954. When IOR/ is active low signifying a PC data read cycle, the transceiver becomes an output port and passes SC11954 data to the PC bus provided its driver is enabled. The driver outputs are in a Hi Z state if it is disabled. It is enabled when the UART, Sound Blaster,Joystick or configuration registers are accessed by the PC.

UART IRQ Router

The INTO output of the MAC UART is a three state signal and is routed to the appropriate IRQ line selected by the UART IRQ configuration register. When OUT2 bit in the MAC UART MCR register is reset or when IRQ is disabled by the configuration register, IRQ output must be forced to Hi Z state. The bit is decoded at Modem base address+4, bit 3.

Voice DMA IRQ

IRQ output for voice DMA can be set either on the leading edge of TC input from PC. The IRQ output is routed to user selected IRQ line from the settings for the voice DMA software configuration register. In addition IRQ driver must be disabled to Hi Z state if IRQENA bit in Voice DMA Control register (27E) is reset or if it is not enabled by the software configuration setting.

Voice DMA REQ Mux

DREQ output for voice DMA is set by MAC by writing to DREQ bit in the Voice DMA Control register. This DREQ output must be routed to user selected DREQ line using the setting for DMA channel select from software configuration setting. In addition the DREQ driver must be disabled to Hi Z state if REQENA bit in Voice DMA Control register is reset or if Voice DMA is not enabled by the software configuration register.

Voice DMA Acknowledge Mux

DACKx signals from the PC are connected to a multiplexer. The output of the multiplexer (DACK) is used to reset the DREQ latch. DMA Channel selection is done by Plug and Play, see Plug and Play section.

MPU-401 MIDI Ports

The supported ISA ports for the MPU-401 MIDI port are:

OFFSET FROM BASE (HEX)	READ	WRITE
0	Data port	Data port
1	Status port	Command port

SOUND BLASTER EMULATION

The supported ISA ports for the Sound Blaster, OPL FM chip and mixer are:

OFFSET FROM BASE (HEX)	READ	WRITE
0	FM Timer status	OPL3 FM Synthesis register select #1
1	N/A	OPL3 FM Synthesis data #1
2*	N/A	OPL3 FM Synthesis register select #2
3*	N/A	OPL3 FM Synthesis data #2
4	N/A	Mixer register select
5	Mixer data	Mixer data
6	N/A	System reset
8	FM Timer status	OPL3 FM Synthesis register select #1
9	N/A	OPL3 FM Synthesis data #1
A	'DSP' data avail port	N/A
C	'DSP' cmd/data buffer status	'DSP' command/data write buffer
E	'DSP' data avail status	N/A

* These registers may be switched on or off.

Sound Blaster Command Set

OEH – Write Internal ASP Register Data
OFH – Read Internal ASP Register Data

Command	Description
10H	8-bit Direct PCM Data
14H	8-bit DMA PCM Data
16H	DMA ADPCM 4:1 Data
17H	DMA ADPCM 4:1 Data with Reference Byte
1CH	8-bit DMA PCM Data with Auto-Initialize
1EH	8-bit DMA 4:1 ADPCM Data with Auto-Initialize
1FH	8-bit DMA 4:1 ADPCM Data with Auto-Initialize + Reference Byte
20H	8-bit Direct ADC Data Read
24H	8-bit DMA ADC Data Read
2CH	8-bit DMA ADC Data Read with Auto-Initialize
30H	Polling Mode MIDI Data Read
31H	Interrupt Mode MIDI Data Read
34H	MIDI UART Polling Mode
35H	MIDI UART Interrupt Mode
36H	MIDI Time Stamping Mode
37H	MIDI Time Stamping Mode
38H	MIDI Data Write
40H	Set PCM Time Constant
41H	Set Digital Audio Playback Sampling Rate
42H	Set Digital Audio Record Sampling Rate
48H	Set Block Size
74H	DMA 2:1 ADPCM Data
75H	DMA 2:1 ADPCM Data with Reference Byte
76H	DMA 2.6:1 ADPCM Data
77H	DMA 2.6:1 ADPCM Data with Reference Byte
7CH	DMA 2:1 ADPCM Data with Auto-Initialize
7DH	DMA 2:1 ADPCM Data with Auto-Initialize + Reference Byte
7EH	DMA 2.6:1 ADPCM Data with Auto-Initialize
7FH	DMA 2.6:1 ADPCM Data with Auto-Initialize + Reference Byte
80H	Play Silence Command
90H	High Speed DAC DMA with Autoinitialize
91H	High Speed DAC DMA
98H	High Speed ADC DMA with Autoinitialize
99H	High Speed ADC DMA
A0H	Set Mono Recording Mode
A8H	Set Stereo Recording Mode
BxH	16-bit DMA Read and Write Modes
CxH	8-bit DMA Read and Write Modes
D0H	8-bit Halt DMA
D1H	Turn On Speaker
D3H	Turn Off Speaker
D4H	8-bit Continue DMA
D5H	16-bit Halt DMA
D6H	16-bit Continue DMA
D8H	Get Speaker Status
D9H	Disable 16-bit DMA Restart
DAH	Disable 8-bit DMA Restart
E1H	Return Version Code
F2H	Generate 8-Bit Interrupt
F3H	Generate 16-Bit Interrupt

Sound Blaster Address Ports

All Sound Blaster commands are interpreted by the SC11954 in order to control the functional blocks of the emulation hardware. Sound Blaster commands and any data associated with the commands are sent to the card via port base+0CH. Unknown commands are simply ignored. Any data returned from the card in response to the commands is read at port base+0AH.

The protocol for sending commands is to check the command buffer status bit by reading port base+0CH until the bit indicates that the port is empty (i.e. bit 7 is low). The Sound Blaster command can then be sent to the command/data buffer port base+0CH. If any data is to follow the command, the command buffer status bit must be checked until it is again low, followed by a single data byte being written to the command/data buffer. This sequence must be repeated for every data byte that follows the command.

If any data is expected to be returned in response to the command sent, then the data available status bit (bit 7 of port base+0EH) must be checked until it is high, indicating that the data byte is ready to be read from the data available port base+0AH. This sequence must be repeated for every byte expected in response to a given command (if any).

A Sound Blaster reset is initiated by writing '1' followed by a '0' to bit 0 of the 'system reset' port. This causes a reset of the Sound Blaster emulation logic in the SC11954. Immediately following the 'system reset,' the value AAH will be placed in the data available port base+0AH and the data available bit set high (bit 7 of port base+0EH).

OPL FM Address Ports

The OPL3 FM synthesis ports are decoded at base+0 to base+3 and are decoded at ISA addresses 388H to 38BH. OPL4 can be decoded at ISA addresses 388H to 38FH. These decodes are used to generate the OPL chip select supplied to the OPL3/OPL4.

Mixer Address Ports

The mixer is accessed via Sound Blaster addresses base+4 and base+5. Address base+4 is the mixer register select port. Address base+5 is the mixer data port which may be read or written after setting the mixer register select.

Direct Memory Access (DMA)

The Sound Blaster DMA controller is based on an 8-bit 1ms timer and a 16-bit counter. The timer preset is set by the Sound Blaster 'Set Time Constant' commands 40H/41H/42H, while the counter LSB and then the MSB follow any 'start DMA' command. On overflow of the timer, the timer preset is reloaded and an ISA DMA request is generated with the 'command buffer status bit' (bit 7 of Sound Blaster port base+0CH) held logical high for approximately 20ms during the DMA cycle. Finally, after the DMA cycle has completed, the counter is decremented. When a DMA cycle occurs with a count = 0000H, the DMA transfers have completed and an ISA interrupt is generated and the timer and counter disabled.

The DMA controller has four control bits which are set and cleared by Sound Blaster commands. These are a counter/timer enable; a DMA direction control; a DMA request enable which allows generation of an ISA DMA request upon overflow of the timer; and a DMA data transfer enable which allows writing of the DMA data the DAC. ADC DMA transfers to the ISA bus sample the ADC and return the current value upon initiation of each DMA cycle.

High speed DMA is essentially the same, except that the DMA length must be preset using SB command 48H. In addition, all SB commands are ignored during the full length of the DAC or ADC transfers until the last DMA cycle occurs. The only way to stop a transfer is to initiate a SB reset by writing to the SB reset port, base+6.

Midi Ports

The MPU-401 UART mode MIDI port is decoded at two consecutive addresses from the port base 330H or 300H. Status port 3x1H has two bits defined. Bit 6 is cleared when the MIDI interface is ready to receive a data/command for output. Bit 7 is cleared when data is available for read from the MIDI input interface. Bits 5 to 0 are undefined.

The following 4 commands can be sent to port 3x1H. All other commands return ACK (FEH) and then are ignored.

3FH—SET UART MODE – Places the MPU-401 into UART send/receive mode. A command ACK byte, FEH can be read back from the MIDI data port 3x0H if the mode switch is successful.

ACH—GET VERSION NUMBER – Returns ACK (FEH) followed by 15H at the MIDI data port 3x0H.

ADH—GET REVISION NUMBER – Returns ACK (FEH) followed by 01H at the MIDI data port 3x0H.

FFH—RESET – Resets the MPU-401 interface. Returns ACK (FEH) if not in UART mode.

To send data to the MIDI port, the interface must initially be set to UART mode. Before writing each MIDI byte to port 3x0H, bit 6 of the status port 3x1H must be clear. To receive data from the MIDI port, the interface must also be set to UART mode. When bit 7 of the status port 3x1H is clear, a data byte may be read from data port 3x0H. An interrupt on the host PC will also be generated when each MIDI data byte is received.

The Sound Blaster MIDI port is controlled via Sound Blaster commands (see **Sound Blaster Command Set**).

MIXER

Sound Blaster 16 Registers

The supported internal registers for Sound Blaster 16 mixer functions are:

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00H	DATA RESET							
04H	DIGITAL AUDIO VOL. LEFT				DIGITAL AUDIO VOL. RIGHT			
0AH						MIC MIXING		
0CH			X		X	INPUT SOURCE		
0EH			X				STEREO	
22H	MASTER VOL. LEFT				MASTER VOL. RIGHT			
26H	FM VOL. LEFT				FM VOL. RIGHT			
28H	CD VOL. LEFT				CD VOL. RIGHT			
2EH	LINE IN VOL. LEFT				LINE IN VOL. RIGHT			
30H	MASTER VOL. LEFT							
31H	MASTER VOL. RIGHT							
32H	DIGITAL AUDIO VOL. LEFT							
33H	DIGITAL AUDIO VOL. RIGHT							
34H	FM SYNTH VOL. LEFT							
35H	FM SYNTH VOL. RIGHT							
36H	CD AUDIO VOL. LEFT							
37H	CD AUDIO VOL. RIGHT							
38H	LINE IN VOL. LEFT							
39H	LINE IN VOL. RIGHT							
3AH	MIC. VOLUME							
3BH	MODEM VOL.							
3CH				OUTPUT MIXER SWITCHES				
				LINE L.	LINE R.	CD L.	CD R.	MIC
3DH		INPUT MIXER LEFT SWITCHES						
		FM L.	FM R.	LINE L.	LINE R.	CD L.	CD R.	MIC
3EH		INPUT MIXER RIGHT SWITCHES						
		FM L.	FM R.	LINE L.	LINE R.	CD L.	CD R.	MIC
3FH	UNUSED							
40H	UNUSED							
41H	UNUSED							
42H	UNUSED							
43H								AGC
44H	TREBLE LEFT							
45H	TREBLE RIGHT							
46H	BASS LEFT							
47H	BASS RIGHT							
80H	1	1	1	1	IRQ10	IRQ7	IRQ5	IRQ2
81H	DMA7	DMA6	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0
82H						MPU401	16-bit DMA	8-bit DMA
83H						MASK	MASK	MASK

RESERVED BITS **NOTE:** All "UNUSED" locations preserve any programmed data values.

SC18075 Mixer Registers

The SC18075 mixer registers are defaulted as follows –

	BITS							
Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00H	0	1	1	0	1	1	0	0
01H	0	1	1	1	1	1	1	1
02H	0	0	0	1	1	1	1	1
03H	0	0	1	1	1	1	1	1
04H	0	1	0	1	1	1	1	1
05H	0	0	1	0	0	1	1	1
06H	0	1	0	0	0	1	1	1
07H	0	0	1	1	1	1	1	1
08H	0	1	0	1	1	1	1	1
09H	0	0	1	0	0	1	1	1
0AH	0	1	0	0	0	1	1	1
0BH	1	0	0	1	1	1	1	1
0CH	1	0	0	1	1	1	1	1
0DH	1	0	0	0	1	0	0	0
0EH	1	0	0	0	1	0	0	0
0FH	0	1	1	0	0	1	1	0
10H	1	0	1	1	1	1	1	1

00H Connect modem audio to left and right mixer, set modem audio volume to level 1.

01H Connect mic left input to left and right mixer, set mic left volume to level 0.

02H Disconnect mic right input from left and right mixer, set mic right volume to level 0.

03H Connect line left input to left mixer, set line input left volume to level 0.

04H Connect line right input to right mixer, set line input right volume to level 0.

05H Connect MIDI left input to left mixer, set MIDI left volume to level 24.

06H Connect MIDI right input to right mixer, set MIDI right volume to level 24.

07H Connect CD audio left input to left mixer, set CD audio left volume to level 0.

08H Connect CD audio right input to right mixer, set CD audio right volume to level 0.

09H Enable DAC, connect wave (DAC) left input to left mixer, set wave left volume to level 24.

0AH Enable ADC, connect wave (DAC) right input to right mixer, set wave right volume to level 24.

0BH Set master left volume to level 24.

0CH Set master right volume to level 24.

0DH Set left treble/bass tone controls to flat.

0EH Set right treble/bass tone controls to flat.

0FH Select microphone right and CD audio right for input to the right ADC summer, select microphone left and CD audio left for input to the left ADC summer.

10H Select FCLK frequency of 10.584 MHz, normal power-up mode, stereo mixer mode, enable the left and right line outputs, enable both DACs and ADCs, and set the bandwidth of the ADC antialiasing filters to one fourth the sample rate.

Mixer Register Functions

Register 00H, Reset

Any 8-bit value written to this register address will reset the mixer. All registers will be restored to their original default values, including those in the SC18075 mixer. **NOTE:** This register is write-only

Register 04H, Digital Audio Volume

This register provides volume control for the Sound Blaster digital audio. The upper 4 bits control the left channel volume and the lower 4 bits control the right channel volume. Default level is 12.

Register 0AH, Microphone Mixing

This register provides a 3-bit input volume control for the microphone. Default level is 0.

Register 0CH, Input Source (Sound Blaster Pro emulation only)

Bits 1 and 2 of this register are used to set the recording input source for the Sound Blaster Pro. The following selections are possible:

0 or 2	Microphone
1	CD audio
3	Line input

These bits will update the appropriate Sound Blaster 16 mixer registers by setting the selected source and clearing all other input sources (see Registers 3DH and 3EH). Default input source is 0 (Microphone).

Register 0EH, Stereo Mode (Sound Blaster Pro only)

Bit 1 of this register is used to set the system into stereo mode for Sound Blaster Pro compatibility. A 1 indicates stereo, 0 (default) indicates mono.

Register 22H, Master Volume

This register provides volume control for the master output. The upper 4 bits control the left channel volume and the lower 4 bits control the right channel volume. Default level is 12.

Register 26H, FM Synth Volume

This register provides volume control for the OPL2/3 FM synthesizer. The upper 4 bits control the left channel volume and the lower 4 bits control the right channel volume. Default level is 12.

Register 28H, CD-Audio Volume

This register provides volume control for the CD-ROM audio. The upper 4 bits control the left channel volume and the lower 4 bits control the right channel volume. Default level is 0.

Register 2EH, Line Input Volume

This register provides volume control for external line input audio. The upper 4 bits control the left channel volume and the lower 4 bits control the right channel volume. Default level is 0.

Register 30H, Left Master Volume
Register 31H, Right Master Volume

These registers provide volume control for the master output. The upper 5 bits of each register (bits 3-7) control the specified volume (32 levels, -62 dB to 0 dB, in 2 dB steps). Default level is 24 (-14 dB).

Register 32H, Left Digital Audio Volume
Register 33H, Right Digital Audio Volume

These registers provide volume control for the Sound Blaster digital audio. The upper 5 bits of each register (bits 3-7) control the specified volume (32 levels, -62 dB to 0 dB, in 2 dB steps). Default level is 24 (-14 dB).

Register 34H, Left FM Synth Volume
Register 35H, Right FM Synth Volume

These registers provide volume control for the OPL3 FM synthesizer audio. The upper 5 bits of each register (bits 3-7) control the specified volume (32 levels, -62 dB to 0 dB, in 2 dB steps). Default level is 24 (-14 dB).

Register 36H, Left CD-Audio Volume
Register 37H, Right CD-Audio Volume

These registers provide volume control for the CD-ROM audio input. The upper 5 bits of each register (bits 3-7) control the specified volume (32 levels, -62 dB to 0 dB, in 2 dB steps). Default level is 0 (-62 dB).

Register 38H, Left Line Input Volume
Register 39H, Right Line Input Volume

These registers provide volume control for the external line input. The upper 5 bits of each register (bits 3-7) control the specified volume (32 levels, -62 dB to 0 dB, in 2 dB steps). Default level is 0 (-62 dB).

Register 3AH, Microphone Volume

This register provides volume control for the microphone input. The upper 5 bits of this register (bits 3-7) controls the volume (32 levels, -62 dB to 0 dB, in 2 dB steps). Default level is 0 (-62 dB).

Register 3BH, Modem Audio Volume

This register provides volume control for the modem audio. The upper 2 bits of this register controls the volume (4 levels, MUTE / -18 / -6 / 0 dB). Default is 1 (-18 dB).

Register 3CH, Output Mixer Switches

Each of the 5 specified bits of this register control the mixer output switches. A value of 1 closes the switch, 0 opens the switch. Default is all bits set (switches closed).

Register 3DH, Left Input Mixer Switches
Register 3EH, Right Input Mixer Switches

These bits control the mixer input switches to the ADC. A value of 1 closes the switch, 0 opens the switch. Defaults are shown below:

Registers 3FH - 42H, Unused

Register 43H, AGC Select

Register 44H/45H, Left/Right Treble Control
Register 46H/47H, Left/Right Bass Control

The upper 4 bits of these registers determine the treble/bass cut or boost for the left and right channels. Default is 8 (flat). 0 is maximum cut, 15 is maximum boost.

Register 80H, Interrupt Status Register

This register is used by the Sound Blaster 16 to configure or determine the IRQ setting. For the SQ3265 this is used as a read-only register—Plug and Play registers must be used for IRQ configuration.

Register 81H, DMA Status Register

This register is used by the Sound Blaster 16 to configure or determine the DMA channel settings. For Casino this is used as a read-only register – Plug and Play registers must be used for DMA channel configuration.

Register 82H, Interrupt Status Register

This read-only register provides status as to what type of interrupt was triggered on the host PC. If bit 0 is set, the interrupt was due to 8-bit DMA or Sound Blaster MIDI. If bit 1 is set, the interrupt was due to 16-bit DMA. If bit 2 is set, the interrupt was due to MPU-401 MIDI.

Interrupts must be acknowledged by the PC by reading one of the following I/O ports:

2xEH = 8-bit DMA or Sound Blaster MIDI
2xFH = 16-bit DMA
3x0H = MPU-401 MIDI

Register 83H, Interrupt Mask Register

This register provides three mask bits corresponding to each bit of the Interrupt Status Register (82H). The mask bits are all defaulted to 1, indicating that each of the status bits are active. To disable an interrupt status bit, set the corresponding mask bit to 0.

MIDI L	MIDI R.	LINE L.	LINE R.	CD L.	CD R.	MIC
0	0	1	0	1	0	1

3DH, Left Input Mixer Switch Defaults

MIDI L	MIDI R.	LINE L.	LINE R.	CD L.	CD R.	MIC
0	0	0	1	0	1	1

3EH, Right Input Mixer Switch Defaults

CLOCK SYNTHESIZER

The SC11954 system requires several clock signals. The modem requires a clock for the internal controller, DSP, and analog front end; the mixer needs both a sample rate and a filter clock; and the OPL3/4 needs a master clock for operation.

The clock for the analog front-end is generated in the DSP chip from the DSP master clock. So, the modem DSP and controller only require selection between two different clock rates: 39.3216MHz or 49.15197MHz.

The sample rate clocks for the SC18075 mixer/ADC/DAC will be generated in digital logic derived from a fixed 48MHz clock. The resulting sampling rates will range from 5KHz to 45KHz. The serial interface bit clock for the SC18075 mixer is based on the sample rate x 48. Additionally, a 10.584MHz filter clock must be generated for the SC18075 treble/bass tone control circuit.

The OPL3 FM synthesis chip needs a 14.31818 MHz clock. Support for OPL4 must be provided by an additional external clock. A 2 MHz master clock is also needed for the Sound Blaster and MIDI UART sections.

To generate all the necessary clocks a 14.31818 MHz crystal oscillator will be used. The output of the oscillator will directly supply the clock to the OPL3 chip.

The Sound Blaster 2 MHz clock is generated by dividing the 14.31818 MHz master clock by 7.166666. The logic divides the master clock by 7 and every sixth edge of the divided clock it eliminates one pulse from the divider clock. This effectively divides the clock 5 cycles by 7 and one cycle by 8. The effective divide ratio is (5x7+8)/6=7.16666. The frequency of the resulting clock is 14.31818/7.16666=1.99789MHz which is within 0.1% of the desired 2 MHz signal.

The SC18075 filter clock is generated by dividing the 14.31818 MHz master clock by 1.333333. The logic uses the master clock and every fourth edge it eliminates one pulse from the divider clock. This effectively divides the clock 2 cycles by one and one cycle by 2. The effective divide ratio is (2x1+2)/

3=1.33333. The frequency of the resulting clock is 10.73864 MHz which is within 1.5% of the desired frequency.

The other sample rate clock for the SC18075 is generated by a clock synthesizer PLL. The required 48MHz clock is derived from the 14.31818MHz master clock.

The modem clock is generated by a second clock synthesizer PLL. The PLL also uses the 14.31818MHz master clock to synthesize the necessary clock for the modem system. One frequency select input (CLKSEL), programs the PLL into the appropriate mode. When CLKSEL is 0, the modem output clock will be 39.3216MHz. When CLKSEL is 1, the modem output clock will be 49.1520MHz. The CLKSEL input is controlled by the Modem Controller Register bit GCR1.0.

The VCO and crystal divider ratios for the PLLs are given in the following:

F_{XTL} = 14.31818 MHz

$F_{48} = F_{XTL} x (224/67) = F_{XTL} x 2 x (112/67)$ = 47.86973 MHz (~48 MHz)

$F_{39} = F_{XTL} x (184/67) = F_{XTL} x 2 x (92/67)$ = 39.32157 MHz

$F_{49} = F_{XTL} x (230/67) = F_{XTL} x 2 x (115/67)$ = 49.15197 MHz

In all cases the error is insignificant. Notice that the VCO divider has a factor of two that has been extracted for all three possible cases. This allows using a PLL circuit that has a 7-bit counter. The feedback resistor for the crystal oscillator circuit will be included on-chip. The capacitors however will be external.

The PLL clock system also has a power-down mode which will shut down both PLLs and the crystal oscillator.

GAME PORT

The game port is provided to connect joysticks and game paddles to the PC. It provides four digital input points and four resistance sensing input points. These points are typically used to sense the trigger buttons and joystick potentiometer positions. The game control card is decoded at address range 0200H-0207H. An I/O Write, with any data, will fire four one-shot circuit devices. The output of the one-shot devices can be read by using an I/O Read at address 0201H. The input register at address 0200H-0207H also contains the four trigger inputs from the connector. The outputs of the one shot circuits are determined by an RC time-constant circuit attached to each one-shot device. The resistive portion of the time-constant is added by the user's interface in the form of a potentiometer in the joystick. Thus, by measuring the length of the one-shot output and knowing the capacitive value of the circuit, one can determine the value of the resistance attached to the input.

The resistive element must be attached to a +5V for the circuit to operate properly. Thus, any external condition that can be represented as a resistive value can be sensed and read using the circuit. For a joystick, the resistance represents the position of the joystick. The joystick read port is defined as follows:

BIT	USE	PIN ON DB15
0	POSITION 1	3
1	POSITION 2	6
2	POSITION 3	11
3	POSITION 4	13
4	SWITCH 1	2
5	SWITCH 2	7
6	SWITCH 3	10
7	SWITCH 4	14

The relationship of the one-shot output pulse length and the external resistance is defined by the following equation –

Time = 24.2 + 0.011 x R (in microseconds)

This equation will give only an approximate value in a range of resistive values from 0 to 100k Ohms. If the cable length to the resistive value is long, extra capacitance will be added to the circuit, changing the time-constant. The sample rate obtained using this circuit is dependent on the maximum resistive value being measured. The larger the resistance, the longer the time. It should also be pointed out that the one-shot circuits cannot be fired individually; all are fired at once.

Some fast PC's need a shorter one-shot pulse length for a given sensing resistance value. To accommodate this, a programming bit is included in the Plug and Play interface register (JOYSP), which will control the value of the comparator reference voltage hence reducing the length of the pulse. Nominally the value of the comparator reference voltage for the nominal value of the one-shot pulse is V_{REF}=(2/3)xVDD. For fast PC's the length of he one-shot is half of the nominal value. This requires the reference voltage to be V_{REF}=0.42xVDD.

ENHANCED IDE INTERFACE

The Enhanced IDE interface is relatively simple. The ISA bus address bits A[2:0], ISA I/O read strobe, and ISA I/O write strobe are buffered and supplied as outputs for the interface. In addition, the IDE interrupt is driven onto the ISA bus by the Plug and Play logic. The Plug and Play logic also supplies two chip selects and two buffer enables to the external IDE interface. The chip selects indicate valid ISA address decode ranges based on the decodes programmed into the Plug

and Play logic and are supplied directly to the IDE bus connector. The two buffer enables are used to enable two external 74LS245 buffers that sit between the IDE 16 bit data bus and the ISA 16 bit data bus. The low byte buffer enable is valid (active low) whenever either of the two chip selects is valid. The high byte buffer enable is valid when the IDE chip select A is valid and the IDE interface is indicating a 16 bit transfer (i.e. the input pin IDE16B is low.)

The enhanced IDE interface can actually be used to implement any other interface (CDROM or other) that requires ISA I/O space decoding and/or the use of an ISA interrupt. The first ISA decode (chip select A) can be configured via Plug and Play to decode either 4, 8, 16, or 32 bytes of I/O space. The second ISA decode (chip select B) is fixed to decode only one byte of I/O space. The buffered ISA bus strobes can be used (if needed) and the 74LS245 buffer enables are also available. Note that the high byte buffer enable is only active for chip select A while IDE16B is low (see above.) The interrupt input will be driven onto the appropriate ISA bus IRQ as defined by Plug and Play. Any other logic required to implement the interface must be designed externally. Note that no DMA channel is supplied for use by the interface, as CDROMs no longer use DMA access due to its lower bandwidth than straight programmed I/O.

PLUG AND PLAY AUTO-CONFIGURATION

The Plug and Play auto-configuration logic is provided in order to eliminate the need of hardware jumpers and ease installation of a peripheral card in an ISA bus-based host system. This logic configures all necessary I/O base address ports, port decoding ranges, interrupt request (IRQ) lines and direct memory access (DMA) channels. All data required for Plug and Play is stored in an external 93C66 EERAM; data values shown in this section as **FFH** are when no EERAM is present. When the last byte in the EERAM reads 55H, these values are read from EERAM.

The major steps of the auto-configuration process are as follows:

- Put Plug and Play ISA card in configuration mode
- Isolate Plug and Play ISA card
- Assign a handle and read the card's resource data structure
- After the resource requirements and capabilities are determined for the card, use the handle to assign conflict free resources to each card in the host system
- Activate Plug and Play ISA card and remove it from configuration mode

The Plug and Play software identifies and configures devices using a set of commands defined in this specification. The commands are executed using three, 8-bit I/O ports.

Hardware Protocol

The isolation protocol can be invoked by the Plug and Play software at any time. The initiation key puts the card into configuration mode. The hardware on the card expects 72 pairs of I/O read accesses to the READ_DATA port. The card's response to these reads depends on the value of each bit of the serial identifier which is being examined one bit at a time.

If the current bit of the serial identifier is a "1", then the card will drive the data bus to 55H to complete the first I/O read cycle. If the bit is "0", then the card puts its data bus driver into high impedance. The card in high impedance will check the data bus during the I/O read cycle to sense if another card is driving D[1:0] to "01." During the second I/O read, the card(s) that drove the 55H, will now drive a AAH. All high impedance cards in the host system will check the data bus to sense if another card is driving D[1:0] to "10."

If a high impedance card sensed another card driving the data bus with the appropriate data during both cycles, then that card ceases to participate in the current iteration of card isolation. Such cards, which lose out, will participate in future iterations of the isolation protocol.

NOTE: During each read cycle, the Plug and Play hardware drives the entire 8-bit data bus, but only checks the lower 2 bits.

If a card was driving the bus or if the card was in high impedance and did not sense another card driving the bus, then it should prepare for the next pair of I/O reads. The card shifts the serial identifier by one bit and uses the shifted bit to decide its response.

The above sequence is repeated for the entire 72-bit serial identifier. At the end of this process, one card remains. This card is assigned a handle referred to as the *Card Select Number* (CSN) that will be used

PORT NAME	LOCATION	TYPE
ADDRESS	0279H (Printer status port)	Write-only
WRITE_DATA	0A79H (Printer status port + 0800H)	Write-only
READ_DATA	Relocatable in range 0203H to 03FFH	Read-only

Table 3.

later to select the card. Cards which have been assigned a CSN will not participate in subsequent iterations of the isolation protocol. The card must be assigned a CSN before it will respond to the other commands defined in the specification.

It should be noted that the protocol permits the 8-bit checksum to be stored in non-volatile memory on the card or generated by the on-card logic in real-time. The same LFSR algorithm described in the initiation key section is used in the checksum generation.

The Plug and Play card must not drive the IOCHRDY signal during serial isolation. However, the card may drive IOCHRDY at any other time.

Plug and Play Resources

This specification will only detail the Plug and Play resources specific to the SC11954 product. For other information regarding Plug and Play resources and programming Plug and Play devices, please consult the "Plug and Play ISA Specification" (version 1.0a), published by Intel Corporation and Microsoft Corporation.

Plug and Play cards return read-only configuration information in two formats. The serial identifier is returned bit-wise by the Plug and Play devices in response to reads from the Serial Isolation register. Plug and Play cards also provide resource data sequentially a byte at a time in response to reads from the Resource Data register. The resource configuration data completely describes all resource needs and options of the device.

Serial Identifier

FIELD NAME	LENGTH	DEFINITION
Vendor ID Byte 0	8 bits	Bit[7] 0 Bits[6:2] First character in compressed ASCII Bits[1:0] Second character in compressed ASCII bits[4:3]
Vendor ID Byte 1	8 bits	Bits[7:5] Second character in compressed ASCII bits[2:0] Bits[4:0] Third character in compressed ASCII
Vendor ID Byte 2	8 bits	Product Number (Vendor Assigned)
Vendor ID Byte 3	8 bits	Product Number (Vendor Assigned)
Serial Number Byte 0	8 bits	Serial Number Bits[7:0]
Serial Number Byte 1	8 bits	Serial Number Bits[15:8]
Serial Number Byte 2	8 bits	Serial Number Bits[23:16]
Serial Number Byte 3	8 bits	Serial Number Bits [31:24]
Checksum	8 bits	Checksum of ID and serial number verifies that the information has been correctly read from a Plug and Play ISA card.

Vendor ID

The 32-bit vendor identifier is an EISA ID. This ID consists of -

- `bits[15:0] – three character compressed ASCII EISA ID. Compressed ASCII is defined as 5 bits per character, "00001" = "A" ... "11010" = "Z".
- bits[31:16] – manufacturer specific device code. The SC11954 device code is vendor definable.

Serial/Unique Number

The 32-bit serial number is used in the isolation process for selection of individual Plug and Play ISA cards. If **FFFFFFFFH** is returned, no serial number has been pre-programmed.

Checksum

The checksum field is used to ensure that no conflicts have occurred while reading the device identifier information. The checksum generation is described in Appendix B of the "Plug and Play ISA Specification."

Plug and Play Resource Data Types

Plug and Play resource data fully describes all resource requirements of a Plug and Play ISA card as well as resource programmability and interdependencies. Plug and Play resource data can be described as a series of "tagged" data structures. For a detailed example of resource data is shown on the next page.

SC11954 reserves the last two xbytes of the stored resource information in the 4 Kbit EERAM. They are used as default information and the bits are defined as follows:

BYTE	BITS	DESCRIPTION	BINARY DATA
510	0	Reserved	1
	1	OPL FM synthesizer select	0 = OPL2/3, 1 = OPL4
	2	Alternate Plug and Play MAP used to add separate OPL	0 = 5 logical devices 1 = 6 logical devices
	3	Joystick speed	0 = fast, 1 = slow
	5:4	IDE decode range select	0 0 = 4 bytes, 0 1 = 8 bytes, 1 0 = 16 bytes, 1 1 = 32 bytes
	7:6	Sound Blaster version number	0 0 = version 4.4, 0 1 = version 3.2, 1 0 = version 2.1, 1 1 = version 1.5
511	7:0	Always set to 55H	0 1 0 1 0 1 0 1

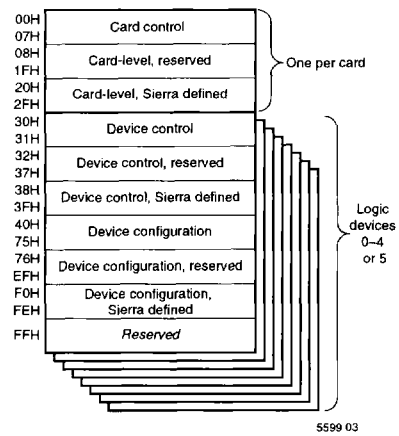
Plug and Play Standard Registers

This specification will only detail the Plug and Play registers specific to the SC11954 product. For other information regarding Plug and Play registers and programming Plug and Play devices, please consult the "Plug and Play ISA Specification" (version 1.0a), published by Intel Corporation and Microsoft Corporation.

The figure illustrates the order of the card registers and the logical device registers. As this figures shows, the card registers are unique for each card. However, the logical devices registers are repeated for each logical device on the card. SC11954 supports 6 logical devices: FAX/Modem, Modem Voice Channel, Sound Blaster 16, OPL FM Synthesizer, Joystick and an Auxiliary device.

NOTE: Any unimplemented registers in the range 00H to FFH must return 0 on reads.

Plug and Play Register Map



Plug and Play Card Control Registers (00H to 2FH)

NAME	REGISTER INDEX	DEFINITION
Set RD_DATA Port	00H	Writing to this location modifies the address of the port used for reading from the Plug and Play ISA cards. Bits[7:0] become I/O read port address bits[9:2]. Reads from this register are ignored.
Serial Isolation	01H	If the card is in the ***Isolation*** state, a read to this register causes the card to compare one bit of the boards ID. This register is read only.
Config Control	02H	Bit[2] - Reset CSN to 0. A write to bit[2] of this register causes all cards to reset their CSN to zero. Bit[1] - Return to the ***Wait for Key*** state. A write to bit[1] of this register causes the card to enter the ***Wait for Key*** state, but all CSNs are preserved and logical devices are not affected. Bit[0] - Reset all logical devices and restore configuration registers to their power-up values. A write to bit[0] of this register performs a reset function on all logical devices. This resets the contents of configuration registers to their default state. The card's logical devices enter their default state and the CSN is preserved. This register is write-only. The values are not sticky, that is, hardware will automatically clear them and there is no need for software to clear the bits.
Wake[CSN]	03H	If the card has a CSN that matches the write data[7:0], a write to this port will cause the card to go from the ***Sleep*** state to the either the ***Isolation*** state if the write data for this command is zero or the ***Config*** state if the write data is not zero. Additionally, the pointer to the byte-serial device is reset. This register is write-only.
Resource Data	04H	A read from this address reads the next byte of resource information. The Status register must be polled until bit[0] is set before this register may be read. This register is read only.
Status	05H	Bit[0] when set indicates it is okay to read the next data byte from the Resource Data register. This register is read-only.
Card Select Number	06H	A write to this port sets the card's CSN. The CSN is a value uniquely assigned to each ISA card after the serial identification process so that each card may be individually selected during a Wake[CSN] command. This register is read/write.
Logical Device Number	07H	Selects the current logical device (0 - 7). All reads and writes of I/O, interrupt and DMA configuration information access the registers of the logical device written here. In addition, the I/O Range Check and Activate commands operate only on the selected logical device. This register is read/write.
Card Level Reserved	08H - 1FH	*Reserved for future use (return 0)*
Card Level Vendor Defined	20H - 2FH	*Vendor defined (not used, return 0)*

Plug and Play Logical Devices

The logical devices can be mapped differently, depending on the setting of the "Alternage Plug and Play map" bit in the E^2PROM. If only 5 logical devices are defined, the Plug and Play map will appear as follows:

LOGICAL DEVICE	DESCRIPTION	I/O PORTS	IRQS	DMA CH'S
0	Modem	1	1	—
1	Modem Voice Channel	—	1	1
2	Sound Blaster 16 / MIDI / OPL	3	1	2
3	Joystick	1	—	—
4	Enhanced IDE	2	1	—

This is the best setup for Sound Blaster 16 and OPL3 compatibility under Windows 3.1 and Windows95.

If 6 logical devices are defined, the map will be altered to include a separate OPL synthesizer device as follows:

LOGICAL DEVICE	DESCRIPTION	I/O PORTS	IRQS	DMA CH'S
0	Modem	1	1	—
1	Modem Voice Channel	—	1	1
2	Sound Blaster 16 / MIDI	2	1	2
3	OPL	1	—	—
4	Joystick	1	—	—
5	Enhanced IDE	2	1	—

This setup is best when a separate driver is desired for an OPL synthesizer (such as OPL4).

The following tables detail the logical devices and specific registers that are supported by multibanded sound modem.

Modem Logical Device 0 Registers (30H to 3FH)

NAME	REGISTER INDEX	DEFINITION
Activate	30H	This register controls whether or not the modem is active on the ISA bus. Bit[0] if set, activates the modem. Bits[7:1] are reserved and must be zero. This is a read/write register. Before the modem device is activated, I/O range check must be disabled.
I/O Range Check	31H	This register is used to perform a conflict check on the I/O port range programmed for use by the modem. Bit[7:2] Reserved. Bit[1] Enable I/O Range check, if set then I/O Range Check is enabled. I/O range check is only valid when the modem is inactive. Bit[0] if set, forces the modem to respond to I/O reads of the modem's assigned I/O range with a 55H when I/O range check is in operation. If clear, the logical device drives AAH. This register is read/write.
Modem Ctrl Reserved	32H - 37H	*Reserved for future use*
Modem Ctrl Sierra Defined	38H - 3FH	*Vendor defined registers (not used)*

Modem Configuration Registers

The resource assignments of Plug and Play cards are programmed through the address and command/data port in the same method used for issuing commands. The following registers define I/O and interrupt resources used by the modem. These configuration registers are read/write so all current configuration information may be read from the card.

Modem Memory Configuration Registers (40H to 5FH, 76H to A8H)

These are not used by the device.

Modem I/O Configuration Registers (60H to 6FH)

Configuration registers 60H - 6FH are used for I/O range configuration. Of the maximum eight I/O descriptors available per logical device, the modem uses only one. Writing a base address of 0000H will disable the I/O range.

NAME	REGISTER INDEX	DEFINITION
Modem I/O port base address bits[15:8]	60H	Read/write value indicating the selected COM port I/O lower limit address bits[15:8]. If a logical device indicates it only uses 10 bit decoding, then bits[15:10] do not need to be supported.
Modem I/O port base address bits [7:0]	61H	Read/write value indicating the selected COM port I/O lower limit address bits[7:0].
I/O port base address	62H - 6FH	*Not used*

Modem Interrupt Configuration Registers (70H to 73H)

NAME	REGISTER INDEX	DEFINITION
Modem COM port interrupt request level	70H	Read/write value indicating selected interrupt level for the modem COM port. Bits[3:0] select which interrupt level is used. Three selects IRQL 3, four selects IRQL 4, etc. IRQL 0 is not a valid interrupt selection and represents no interrupt selection.
Modem COM port rupt request type	71H	Read value indicating which type of interrupt is used for the inter-Request Level selected above. Bit[0] : Type, **0 = edge** Bit[1] : Level, **1 = high** Bits[7:2] : Reserved.
Interrupt request level/type	72H - 73H	*Not used*

Modem DMA Configuration Registers (74H to 75H)

These are not used by this device. Reads will return 04H.

Modem Vendor-Specific Configuration Registers (A9 to FEH)

These are not used by the device.

Modem Voice Channel Logical Device 1 Registers (30H to 3FH)

NAME	REGISTER INDEX	DEFINITION
Activate	30H	This register controls whether or not the modem voice channel is active on the ISA bus. Bit[0] if set, activates the voice. Bits[7:1] are reserved and must be zero. This is a read/write register. Before the voice device is activated, I/O range check must be disabled.
I/O Range Check	31H	*This register is not supported.*
Modem Ctrl Reserved	32H - 37H	*Reserved for future use*
Modem Ctrl Sierra Defined	38H - 3FH	*Vendor defined registers (not used)*

Modem Voice Channel Configuration Registers

The following registers define the interrupt and DMA resources used by the modem voice channel. These configuration registers are read/write so all current configuration information may be read from the card.

Modem Memory Configuration Registers (40H to 5FH, 76H to A8H)

These are not used by the device.

Modem I/O Configuration Registers (60H to 6FH)

These are not used by the device.

Modem Voice Channel Interrupt Configuration Registers (70H to 73H)

NAME	REGISTER INDEX	DEFINITION
Voice DMA interrupt request level	70H	Read/write value indicating selected interrupt level for voice DMA terminal count. Bits[3:0] select which interrupt level is used. Five selects IRQL 5, nine selects IRQL 9, etc. IRQL 0 is not a valid interrupt selection and represents no interrupt selection.
Voice DMA interrupt type	71H	Read value indicating which type of interrupt is used for the request Request Level selected above. Bit[0] : Type, **0 = edge** Bit[1] : Level, **1 = high** Bits[7:2] : Reserved.
Interrupt request level/type	72H - 73H	*Not used*

Modem Voice Channel DMA Configuration Registers (74H to 75H)

NAME	REGISTER INDEX	DEFINITION
Modem Voice 8-bit channel select	74H	Read/write value indicating selected Modem Voice 8-bit DMA DMA channel. Bits[2:0] select which DMA channel is in use. One selects DMA channel 1, three selects DMA channel 3. DMA channel 4, the cascade channel is used to indicate no 8-bit DMA channel is active.
DMA channel select	75H	*Not used.* Reads return 04H.

Modem Voice Channel Vendor-Specific Configuration Registers (A9 to FEH)

These are not used by the device.

Sound Blaster 16 Logical Device 2 Registers (30H to 3FH)

NAME	REGISTER INDEX	DEFINITION
Activate	30H	This register controls whether or not the Sound Blaster 16 is active on the ISA bus. Bit[0] if set, activates the Sound Blaster. Bits[7:1] are reserved and must be zero. This is a read/write register. Before the sound device is activated, I/O range check must be disabled.
I/O Range Check	31H	*This register is not supported.*
Sound Ctrl Reserved	32H - 37H	*Reserved for future use*
Sound Ctrl Sierra Defined	38H - 3FH	*Vendor defined registers (not used)*

Sound Blaster Memory Configuration Registers (40H to 5FH, 76H to A8H)

These are not used by the device.

Sound Blaster I/O Configuration Registers (60H to 6FH)

NAME	REGISTER INDEX	DEFINITION
Sound Blaster I/O port address bits [15:8]	60H	Read/write value indicating the Sound Blaster I/O base address base bits[15:8].
Sound Blaster I/O port base address bits [7:0]	61H	Read/write value indicating the Sound Blaster I/O base address bits[7:0].
MIDI I/O port base address bits [15:8]	62H	Read/write value indicating the MPU-401 MIDI I/O base address bits [15:8].
MIDI I/O port base address bits [7:0]	63H	Read/write value indicating the MPU-401 MIDI I/O base address bits [7:0].
OPL I/O port base address bits [15:8]	64H	Read/write value indicating the OPL FM synthesizer I/O base address bits [15:8]. *Note: Optional I/O port.*
OPL I/O port base address bits [7:0]	65H	Read/write value indicating the OPL FM synthesizer I/O base address bits [7:0]. *Note: Optional I/O port.*
I/O port base address	62H - 6FH	*Not used*

NOTE: The OPL I/O port base registers are available only when 5 logical devices are defined.

Sound Blaster Interrupt Configuration Registers (70H to 73H)

NAME	REGISTER INDEX	DEFINITION
Sound Blaster interrupt request level select	70H	Read/write value indicating selected interrupt level for the Sound Blaster. Bits[3:0] select which interrupt level is used. Five selects IRQL 5, seven selects IRQL 7, etc. IRQL 0 is not a valid interrupt selection and represents no interrupt selection.
Sound Blaster interrupt type select	71H	Read value indicating which type of interrupt is used for the request Request Level selected above. Bit[0] : Type, **0 = edge** Bit[1] : Level, **1 = high** Bits[7:2] : Reserved.
Interrupt request level/type	72H - 73H	*Not used*

Sound Blaster DMA Configuration Registers (74H to 75H)

NAME	REGISTER INDEX	DEFINITION
Sound Blaster 8-bit DMA channel select	74H	Read/write value indicating selected Sound Blaster 8-bit DMA channel. Bits[2:0] select which DMA channel is in use. One selects DMA channel 1, three selects DMA channel 3. DMA channel 4, the cascade channel is used to indicate no 8-bit DMA channel is active.
Sound Blaster 16-bit DMA channel select	75H	Read/write value indicating selected Sound Blaster 16-bit DMA channel.

Sound Blaster Vendor-Specific Configuration Registers (A9 to FEH)

NAME	REGISTER INDEX	DEFINITION
Sound Blaster device configuration reserved	A9H - EFH	*Reserved*
Sound Blaster device configuration Sierra	F0H	Bit[0] Reserved. Bits[2:1] are used to define the Sound Blaster returned version number: 00 = version 4.4 (S.B. 16) 01 = version 3.2 (S.B. Pro) 10 = version 2.1 (S.B. Basic) 11 = version 1.5 (S.B. Basic) Bits[7:3] are not used.
Sound Blaster device configuration Sierra defined	F1H - FEH	*Reserved*

OPL FM Synthesizer Logical Device 4 Registers (30H to 3FH)

NAME	REGISTER INDEX	DEFINITION
Activate	30H	This register controls whether or not the OPL synthesizer is active on the ISA bus. Bit[0] if set, activates the OPL chip. Bits[7:1] are reserved and must be zero. This is a read/write register. Before the sound device is activated, I/O range check must be disabled.
I/O Range Check	31H	This register is used to perform a conflict check on the I/O port range programmed for use by the OPL chip. Bits[7:2] Reserved. Bit[1] Enable I/O Range check, if set then I/O Range Check is enabled. I/O range check is only valid when the OPL is inactive. Bit[0] if set, forces the OPL to respond to I/O reads of the device's assigned I/O range with a 55H when I/O range check is in operation. If clear, the logical device drives AAH. This register is read/write.
OPL Ctrl Reserved	32H - 37H	*Reserved for future use*
OPL Ctrl Sierra Defined	38H - 3FH	*Vendor defined registers (not used)*

OPL Configuration Registers

The following registers define I/O, interrupt and DMA resources used by the Sound Blaster and OPL FM synthesizer sections of the Plug and Play card. These configuration registers are all read/write so all current configuration information may be read from the card.

OPL Memory Configuration Registers (40H to 5FH, 76H to A8H)

These are not used by the device.

OPL I/O Configuration Registers (60H to 6FH)

NAME	REGISTER INDEX	DEFINITION
OPL I/O port base address bits[15:8]	60H	Read/write value indicating the OPL FM chip I/O base address bits[15:8].
OPL I/O port base address bits[7:0]	61H	Read/write value indicating the OPL FM chip I/O base address bits[7:0].
I/O port base address	62H - 6FH	*Not used*

OPL Interrupt Configuration Registers (70H to 73H)

These are not used by the device.

OPL DMA Configuration Registers (74H to 75H)

These are not used by the device. Reads return 04H.

MIDI Logical Device Registers (30H to 3FH)

NAME	ADDRESS PORT VALUE	DEFINITION
Activate	30H	This register controls whether or not the MIDI port is active on the ISA bus. Bit[0] if set, activates the MIDI port. Bits[7:1] are reserved and must be zero. This is a read/write register. Before the device is activated, I/O range check must be disabled.
I/O Range Check	31H	This register is used to perform a conflict check on the I/O port range programmed for use by the MIDI port. Bits[7:2] Reserved. Bit[1] Enable I/O Range check, if set then I/O Range Check is enabled. I/O range check is only valid when the MIDI port is inactive. Bit[0] if set, forces the MIDI port to respond to I/O reads of the device's assigned I/O range with a 55H when I/O range check is in operation. If clear, the logical device drives AAH. This register is read/write.
MIDI Ctrl Reserved	32H - 37H	*Reserved for future use*
MIDI Ctrl Sierra Defined	38H - 3FH	*Vendor defined registers (not used)*

MIDI Configuration Registers

The following registers define I/O resources used by the MIDI port. These configuration registers are read/write so all current configuration information may be read from the card.

MIDI Memory Configuration Registers (40H to 5FH, 76H to A8H)

These are not used by the device.

MIDI I/O Configuration Registers (60H to 6FH)

NAME	REGISTER INDEX	DEFINITION
MIDI I/O port base address bits [15:8]	60H	Read/write value indicating the MIDI I/O base address bits[15:8].
MIDI I/O port base address bits [7:0]	61H	Read/write value indicating the MIDI I/O base address bits[7:0].
I/O port base address	62H - 6FH	*Not used*

MIDI Interrupt Configuration Registers (70H to 73H)

NAME	REGISTER INDEX	DEFINITION
MIDI interrupt request level select	70H	Read/write value indicating selected interrupt level for the MIDI port. This is an optional interrupt in addition to the interrupt generated by the Sound Blaster. Bits[3:0] select which interrupt level is used. Five selects IRQL 5, seven selects IRQL 7, etc. IRQL 0 is not a valid interrupt selection and represents no interrupt selection.
MIDI interrupt request select	71H	Read value indicating which type of interrupt is used for the type Request Level selected above. Bit[0] : Type, **0 = edge** Bit[1] : Level, **1 = high** Bits[7:2] : Reserved.
Interrupt request level/type	72H - 73H	*Not used*

MIDI DMA Configuration Registers (74H to 75H)

These are not used by the device. Reads return 04H.

MIDI Vendor-Specific Configuration Registers (A9 to FEH)

These are not used by the device.

Joystick/Game Port Logical Device Registers (30H to 3FH)

NAME	REGISTER INDEX	DEFINITION
Activate	30H	This register controls whether or not the joystick is active on the ISA bus. Bit[0] if set, activates the joystick. Bits[7:1] are reserved and must be zero. This is a read/write register. Before the joystick is activated, I/O range check must be disabled.
I/O Range Check	31H	This register is used to perform a conflict check on the I/O port range programmed for use by the joystick. Bit[7:2] Reserved. Bit[1] Enable I/O Range check, if set then I/O Range Check is enabled. I/O range check is only valid when the joystick is inactive. Bit[0] if set, forces the joystick to respond to I/O reads of the joystick's assigned I/O range with a 55H when I/O range check is in operation. If clear, the logical device drives AAH. This register is read/write.
Joystick Ctrl Reserved	32H - 37H	*Reserved for future use*
Joystick Ctrl Sierra Defined	38H - 3FH	*Vendor defined registers (not used)*

Joystick/Game Port Configuration Registers

The following registers define I/O resources used by the joystick. These configuration registers are read/write so all current configuration information may be read from the card.

Joystick Memory Configuration Registers (40H to 5FH, 76H to A8H)

These are not used by the device.

Joystick/Game Port Configuration Registers

The following registers define I/O resources used by the joystick. These configuration registers are read/write so all current configuration information may be read from the card.

Joystick Memory Configuration Registers (40H to 5FH, 76H to A8H)

These are not used by the device.

Joystick I/O Configuration Registers (60H to 6FH)

NAME	REGISTER INDEX	DEFINITION
Joystick I/O port base address bits[15:8]	60H	Read/write value indicating the selected joystick port I/O lower limit address bits[15:8]. If a logical device indicates it only uses 10-bit decoding, then bits[15:10] do not need to be supported.
Joystick I/O port base address bits [7:0]	61H	Read/write value indicating the selected joystick port I/O lower limit address bits[7:0].
I/O port base address	62H - 6FH	*Not used*

Joystick Interrupt Configuration Registers (70H to 73H)

These are not used by the device.

Joystick DMA Configuration Register (74H to 75H)

These are not used by the device. Reads return 04H.

Joystick Vendor-Specific Configuration Registers (A9H to FEH)

NAME	REGISTER INDEX	DEFINITION
Joystick device configuration reserved	A9H - EFH	*Reserved*
Joystick device ration Sierra defined	F0H	Bit[0] is used to set the game port speed for use with joystick configu-controllers. If bit[0] is set to a '0' (default), this selects a fast speed for faster host PC's. A '1' indicates slow speed. Bits[7:1] are not used.
Logical device configuration Sierra defined	F1H - FEH	*Reserved*

Enhanced IDE Logical Drive Registers (30H to 3FH)

NAME	REGISTER INDEX	DEFINITION
Activate	30H	This register controls whether or not the Enhanced IDE device is active on the ISA bus.
I/O Range Check	31H	This register is used to perform a conflict check on the I/O port range programmed for use by the Enhanced IDE device.
Enhanced IDE Ctrl Reserved	32H - 37H	*Reserved for future use*
Enhanced IDE Ctrl Sierra Defined	38H - 3FH	*Vendor defined registers (not used)*

Enhanced IDE Configuration Registers

The following registers define I/O and interrupt resources used by the Enhanced IDE device. These configuration registers are read/write so all current configuration information may be read for the card

Enhanced IDE Memory Configuration Registers (40H to 5FH, 76H to A8H)

These are not used by the device.

Enhanced IDE Configuration Registers (60H to 6FH)

NAME	REGISTER INDEX	DEFINITION
Enhanced IDE I/O port base A address bits[15:8]	60H	Read/write value indicating the IDE port A I/O lower limit address bits[15:8].
Enhanced IDE I/O port base A address bits[7:0]	61H	Read/write value indicating the IDE port A I/O lower limit address bits[7:0].
Enhanced IDE I/O port base B address bits[15:8]	62H	Read/write value indicating the IDE port B I/O lower limit address bits[15:8].
Enhanced IDE I/O port base B address bits[7:0]	63H	Read/write value indicating the IDE port B I/O lower limit address bits[7:0].
I/O port base address	64H - 6FH	*Not used*

Enhanced IDE Interrupt Configuration Registers (70H to 73H)

NAME	REGISTER INDEX	DEFINITION
Enhanced IDE interrupt request level	70H	Read/write value indicating selected interrupt level for the Enhanced IDE port.
Enhanced IDE interrupt request type	71H	Read/write value indicating which type of interrupt is used for the Request Level selected above. Read only (03H).
IRQ/type	72H - 73H	*Not used*

Enhanced IDE DMA Configuration Registers (74H to 75H)

These are not used by the device. Reads return 04H.

Enhanced IDE Vendor-Specific Configuration Registers (A9H to FEH)

NAME	REGISTER INDEX	DEFINITION
Enhanced IDE device configuration reserved	A9H - EFH	*Reserved*
IDE device configuration Sierra defined	F0H	Bits[1:0] are used to set the IDE I/O port A decode range: 00 = 4 bytes (default) 01 = 8 bytes (used for IDE) 10 = 16 bytes 11 = 32 bytes Bits[7:2] are not used.
Logical device configuration Sierra defined	F1H - FEH	*Reserved*

SC18075 GENERAL DESCRIPTION

The SC18075 has a stereo 16 bit analog to digital converter and a stereo 16 bit digital to analog converter.

The SC18075 can be configured to have 5 stereo inputs and a mono input or can be configured as 11 indepen-dent mono channels. Each input has independent level control of 1.5 dB per step with a range of 0–34.6 dB. The stereo input channels MICxx can be connected to internal op-amps for signal amplification, making them ideal for use as microphone inputs. The 16 bit DAC can be configured to connect to one of the input channels so that the synthesized music or digital audio playback can be added to the mix. The SC18075 chip has a stereo output that can be connected to either the master volume control or it can bypass the volume control.

The chip operates from a 10 Volt supply. The SC18075 is packaged in a 68 pin PLCC.

BLOCK DIAGRAM

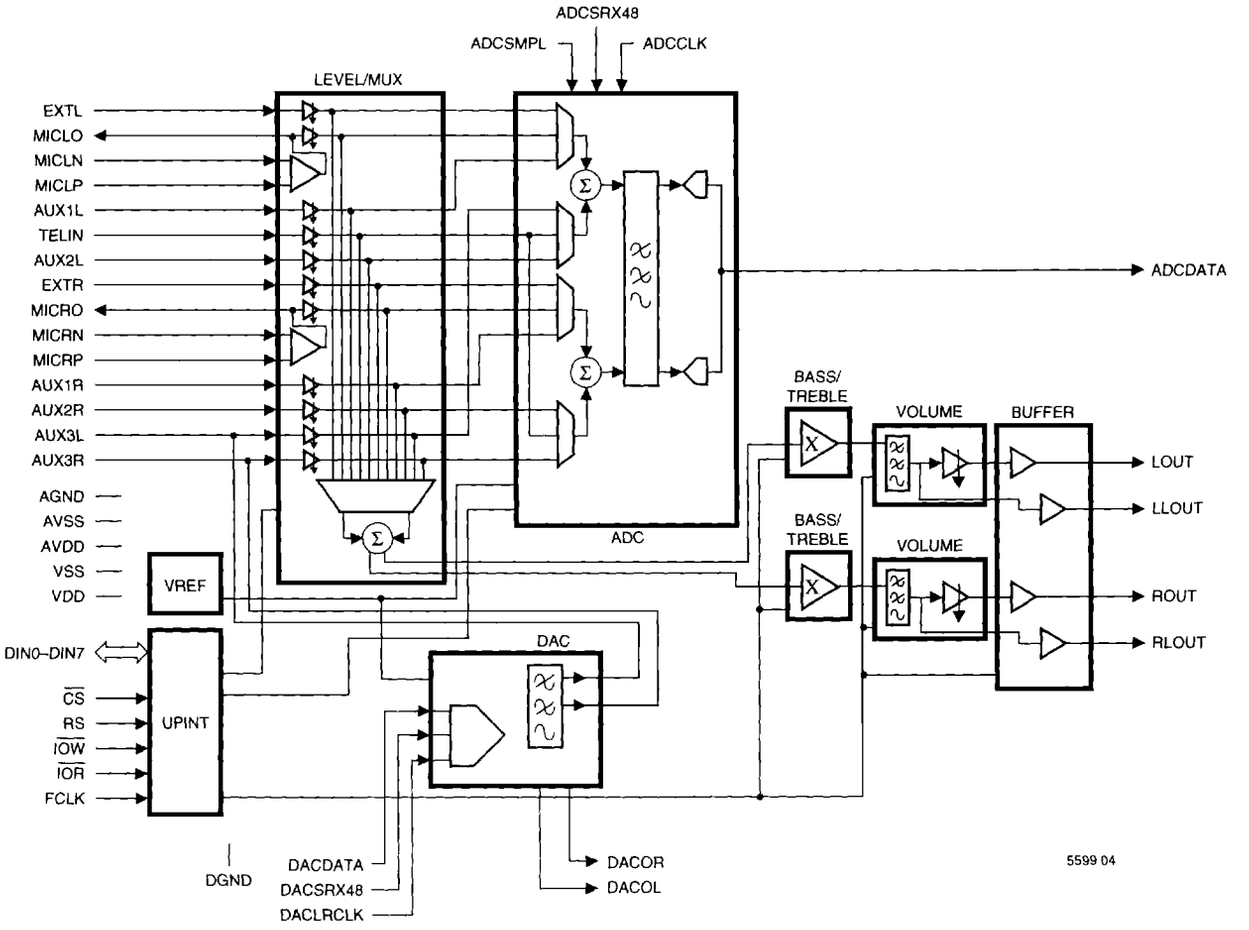
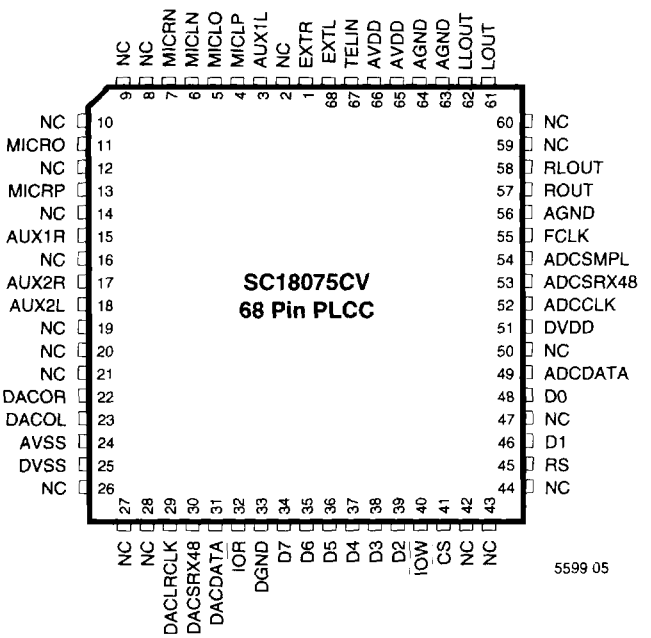


Figure 1.

Pin Description

PIN NAME	PIN NUMBER	DESCRIPTION
ADCCLK	52	**INPUT.** ADC serial interface shift clock.
ADCDATA	49	**OUTPUT.** ADC digital data serial output.
ADCSMPL	54	**INPUT.** ADC sample clock.
ADCSRX48	53	**INPUT.** 48 times ADCSMPL clock.
AGND	56, 63, 64	**POWER.** Analog ground.
AUX1L	3	**INPUT.** Auxiliary1 left input.
AUX1R	15	**INPUT.** Auxiliary1 right input.
AUX2L	18	**INPUT.** Auxiliary2 left input.
AUX2R	17	**INPUT.** Auxiliary2 right input.
AUX3L	—	**INPUT.** Auxiliary3 left input. See "Pin Descriptions" above.
AUX3R	—	**INPUT.** Auxiliary3 right input. See "Pin Descriptions" above.
AVDD	65, 66	**POWER.** Analog +5V.
AVSS	24	**POWER.** Analog -5V.
CS	41	**INPUT.** Chip select, with Internal pull-up of 100K ohm.
D7–D0	34–39, 46, 48	**INPUT/OUTPUT.** 8-bit CPU parallel I/O bus. Internal pull-up 10K ohm.
DACDATA	31	**INPUT.** DAC digital data serial input.
DACLRCLK	29	**INPUT.** DAC left/right clock.
DACOL	23	**OUTPUT.** DAC smoothing filter left output.
DACOR	22	**OUTPUT.** DAC smoothing filter right filter.
DACSRX48	30	**INPUT.** DAC serial interface shift clock.
DGND	33	**POWER.** Digital ground.
DVDD	51	**POWER.** Digital +5V.
DVSS	25	**POWER.** Digital -5V.
EXTL	68	**INPUT.** External left input.
EXTR	1	**INPUT.** External right input.
FCLK	55	**INPUT.** 10.584 MHz or 16.9344 MHz filter sampling clock.
IOR	32	**INPUT.** I/O read control input.
IOW	40	**INPUT.** I/O write control input.
LOUT	61	**OUTPUT.** Left output.
LLOUT	62	**OUTPUT.** Left line output.
MICLO	5	**OUTPUT.** Microphone left channel opamp output.
MICLN	6	**INPUT.** Microphone left channel opamp inverting input.
MICLP	4	**INPUT.** Microphone left channel opamp noninverting input.
MICRO	11	**OUTPUT.** Microphone right channel opamp output.
MICRN	7	**INPUT.** Microphone right channel opamp inverting input.
MICRP	13	**INPUT.** Microphone right channel opamp noninverting input.
NC	2, 8–10, 12, 14, 16, 19–21, 26–28, 42–44, 47, 50, 59–60	Not connected.
RLOUT	58	**OUTPUT.** Right line output.
ROUT	57	**OUTPUT.** Right output.
RS	45	**INPUT.** Control register select input.
TELIN	67	**INPUT.** Telephone input.

CONNECTION DIAGRAMS



NOTE: Pinout subject to change without notice.

FUNCTIONAL DESCRIPTION

The Multimedia Analog Mixer chip is a monolithic CMOS integrated circuit designed to be used in a Multimedia PC environment where a variety of analog sources must be mixed with different levels into a single stereo output pair that connects to an amplifier. System software will control the mixer chip to adjust the relative levels of the individual sources, as well as set the master volume control for the mixed outputs. It supports the mixing of five analog stereo audio sources and one mono source. The chip has two 16-bit Analog-to-Digital (ADC) converters to sample a stereo audio source and a 16-bit Digital-to-Analog (DAC) converter that is multiplexed between the left and right channels of a digital stereo source. It also has a stereo Bass/Treble tone control circuits that can be programmed through external control.

The block diagram of the mixer chip is shown in Figure 1. The mixer chip includes five stereo and one mono input channels, and two stereo output channels. The stereo input channels include the microphone, external input, Auxiliary 1 and 2 and the waveform channel. In addition there is one mono input channel for telephone input. For the left and right inputs of the microphone input, two opamps are provided which can be used to amplify the level of the input signal by using two external resistors. The auxiliary stereo input can be connected to the output of a CD player and the waveform stereo input channel is internally connected to the output of a dual output stereo 16-bit DAC which is used for waveform synthesis.

All input channels first pass through a level control circuit. The level control adjusts the level of the individual input signal within a 0–34.6 dB range with a 1.5 dB/step resolution. Each level control circuit is followed by a channel control mux which under the control of the configuration bits routes the output of the corresponding level control to either the left mixer, right mixer, both left and right mixers or mutes the channel altogether. The ability to independently control the routing of the left and right inputs of a stereo channel provides the flexibility of setting each channel in the mono or stereo mode independent of the setting of the other channels. The output of the channel control muxes are brought to two analog mixers which sum the inputs to form a stereo output. The left and right channels are also summed to provide a mono output. The mono and the left and right stereo outputs are brought to a two-input mux. The output of the mux is applied to the input of a Bass/Treble control circuit. The setting of the Bass/Treble circuit can be altered by the bits in the configuration register. The Bass/Treble stereo signal is brought off-chip as stereo left and right Line outputs. The output of the Bass/Treble circuit also goes to the master volume control which controls the level of the output signal within a 0–71.50 dB range with 0.75 dB/step. The master volume control drives the left and right stereo output drivers.

The mixer chip has two switched-capacitor antialiasing filters followed by two independent 16-bit Analog-to-Digital converters (ADC) that can be used to sample the analog signals from the left and right channel outputs, and convert them to two 16-bit linear PCM codes. The two ADCs can provide two samples (one stereo sample) at a maximum sample rate of 44.1 kHz. The input to the switched-capacitor filters come from a stereo summer. Each summer has two inputs: one from the output of a mux which selects one of the signals from the Microphone, External, Auxiliary1, or ground; and the second from the output of a mux which selects one of the signals from the DAC, telephone, Auxiliary2, or ground. The switched-capacitor antialiasing filter has a clock programmable passband which can be altered by changing the external filter clock frequency.

For sampled and stored or synthesized signals, a 16-bit DAC is provided which can be used to convert the digital stereo inputs to analog outputs. The DAC is multiplexed between the two stereo channels. The outputs of the DAC are sampled-and-held at the sampling rate before they are applied to two switched-capacitor smoothing filters. The passband of the filters are programmed by changing the input clock frequency. The switched-capacitor filters are followed by smoothing filters, the outputs of which are connected to the inputs of the DAC channel level control circuits. They are also brought to pins to be used in such applications as telephone messaging systems.

The data transfer between the mixer and the bus controller is achieved by two independent serial interfaces, one for the DAC and the other for the ADC. The control and interface registers in the mixer are accessed through a parallel interface which can be directly connected to the CPU bus and occupies two I/O addresses. The detailed block diagram of the chip and its connection to the interface chip are shown in Figures 1 and 2 respectively.

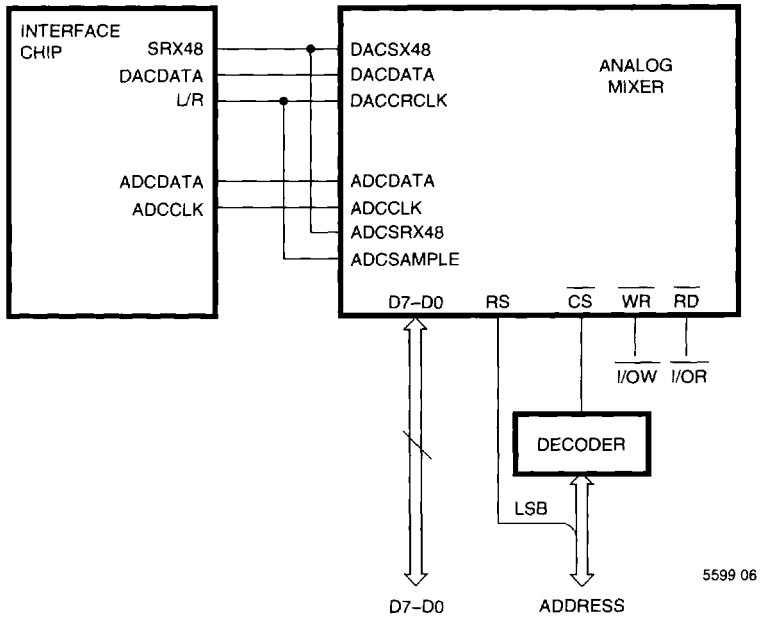


Figure 2.

HARDWARE DESCRIPTION

16-Bit Stereo DAC

The chip includes a two's complement 16-bit DAC that is multiplexed between the left and right outputs of a stereo channel. The data is shifted into the chip through a 3-pin serial interface. The three signals are the DACSRx48 (bit clock) which is always 48 times the conversion rate, DACLRCLK (DAC left/right clock) which indicated whether the left or the right data is being shifted in and the DACDATA which is the DAC stereo serial data. The left and right channel data are shifted in during the high and low cycle of the DACLRCLK respectively. The transition of the DACLRCLK corresponds to the end of the data transfer and is coincident with the falling edge of the DACSRx48. The data changes on the falling edge of DACSRx48 and should be shifted into the chip on the rising edge. The DAC timing and the relevant internal signals are shown in Figure 5.

On every transition of the DACLRCLK the shifted data is transferred to internal buffers and is converted to an analog value by the 16-bit DAC. The left and right samples are converted separately. First the left sample is converted and stored on a temporary sample-and-hold. Next, on the rising edge of DACLRCLK the right sample, and the left sample that was stored on a temporary sample-and-hold, is transferred to the output sample-and-holds and is held until the next rising edge of DACLRCLK. This arrangement allows for both left and right samples to appear at the output at the same time.

The DAC sample-and-holds are followed by two switched-capacitor smoothing low-pass filters. The conversion rate of the DAC is controlled by the

frequency of the DACLRCLK. The passband of the lowpass filters controlled by the frequency of the DACSRx48 clock. The filter passband is 1/96th of the DACSRx48 which corresponds to half the DAC sampling frequency. For each case, the lowpass filter has a shaped passband that compensates for the sin(x)/x droop of the sample-and-hold effects. The passband of the filter is programmed by altering the clock frequency. The clock of the filter is derived by dividing the DACSRx48 by six. The filter sampling frequency for the cases where the DAC sample rate is 44.1 kHz, 22.05 kHz, 31.5 kHz and 15.75 kHz are 352.8 kHz, 176.4 kHz 252 kHz and 126 kHz respectively. The ripple passband edges for the corresponding sampling rates are 18.67 kHz, 9.335 kHz, 13.336 kHz and 6.668 kHz. The filter uses a linear interpolator at the output section to double the effective output sampling rate. The two switched-capacitor filters are followed by two 2nd order analog smoothing lowpass filters. The switched-capacitor lowpass filter has a 6th order transfer function with two transmission zeros which provides a minimum of 50 dB loss in the stopband.

16-Bit Stereo ADC

The chip has a dual two's complement 16-bit ADC that can be used to convert the left and right inputs of a stereo channel to linear PCM. The sampling rate and the sampling instance of both ADCs are controlled by the ADCSAMPLE clock. On the rising edge of the ADCSAMPLE clock both ADCs take an analog sample from their corresponding inputs and convert it to a digital value. In the meantime the PCM code corresponding to the left channel of the previous sample is transferred to the serial interface. The right sample is transferred to a temporary buffer and is held there until the serial interface shifts the left sample out and is ready to accept a new sample. The shift clock is provided from the interface chip and is a burst of 16 pulses. The data is shifted out on the falling edge of the shift clock. There are 16 clock pulses and the MSB is shifted out first. Notice that the MSB should be available for the interface chip to sample on the rising edge of the first clock. Therefore the first falling edge of the clock will transfer the next significant bit out.

The two ADCs are preceded by two switched-capacitor antialiasing filters. The sampling clock of the filters are derived from the ADCSRx48 by dividing it by six. The passband of the filter is designed to be 1/96th of ADCSRx48 which corresponds to half the sampling rate. Therefore for 44.1 kHz, 22.05 kHz, 31.5 kHz and 15.75 kHz sampling rates, the filter clock will be 352.8 kHz, 176.4 kHz, 252 kHz and 126 kHz respectively. The ripple passband corresponding to these cases are 18.67 kHz, 9.335 kHz, 13.336 kHz and 6.668 kHz. The above passbands are valid for the case when SADC = "0", when SADC = "1" the filter clock is changed to 1/12th of ADCSRx48 and the switched-capacitor filter passband is reduced to 1/192nd of the ADCSCx48 which corresponds to one fourth of the ADC sampling rate. This feature is useful is cases where the signal is oversampled at twice the Nyquist rate and later it is decimated by dropping every other sample without digitally filtering it.

The two switched-capacitor antialiasing filters are preceded with two analog antialising filters that bandlimit the filter to prevent aliasing effects. The ADC serial interface timing is shown in Figure 5.

Bass/Treble Circuits

Each of the left and right outputs of the stereo channel has a Bass/Treble circuit which can be used for tone control purposes. They are switched-capacitor filters with programmable pole/zero pairs. The Bass and Treble have 15 settings each, which include one flat, seven cut and seven boost responses. The sampling frequency for the Bass/Treble circuit is 264.6 kHz which is derived from a fixed 10.584 MHz or 16.9344 MHz frequency which is supplied to the chip as an input. The choice between the 10.584 MHz and 16.9344 MHz is made by writing into Bit 7 of configuration register 2. When this bit is a "1," 10.584 MHz is selected. When this bit is a "0," 16.9344 MHz is selected. The various responses achieved from the Bass/Treble circuit is shown in the attached diagrams.

CPU INTERFACE AND CONTROL BITS

The mixer chip uses an indexed addressing mode for the CPU interface. It uses two I/O address locations, one for the index and the other for reading or writing the addressed register. The interface consists of the 8-bit data, $\overline{IOR}$ (I/O Read), $\overline{IOW}$ (I/O Write), $\overline{CS}$ (Chip Select) and RS (Register Select) pins. The chip $\overline{CS}$ is generated by decoding all address lines but the LSB. The RS connects to the low address line. The two address locations are defined as follows:

$\overline{CS}$ = "0" and RS = "0" Read or Write Index Register.

$\overline{CS}$ = "0" and RS = "1" Read or Write the Data Register addressed by the index register.

To read or write a specified register, first the index should be written into the index register (RS = "0") followed by writing the data into the data register (RS = "1"). A CPU I/O cycle and the Read/Write Timing are shown in Figures 3 and 4, respectively.

REGISTER DESCRIPTION

The index register is 8-bit wide and it can address 256 locations. Out of the 256 available address locations, 17 are used by control registers and the remaining 239 remain unused.

Location	Name	7	6	5	4	3	2	1	0
00H	LCMCTI	—	TM1	TM0	TL4	Tl3	TL2	TL1	TL0
01H	LCMCMLI	—	MLM1	MLM0	MLL4	MLL3	MLL2	MLL1	MLL0
02H	LCMCMRI	—	MRM1	MRM0	MRL4	MRL3	MRL2	MRL1	MRL0
03H	LCMCELI	—	ELM1	ELM0	ELL4	ELL3	ELL2	ELL1	ELL0
04H	LCMCERI	—	ERM1	ERM0	ERL4	ERL3	ERL2	ERL1	ERL0
05H	LCMCA1LI	—	A1LM1	A1LM0	A1LL4	A1LL3	A1LL2	A1LL1	A1LL0
06H	LCMCA1RI	—	A1RM1	A1RM0	A1RL4	A1RL3	A1RL2	A1RL1	A1RL0
07H	LCMCA2LI	—	A2LM1	A2LM0	A2LL4	A2LL3	A2LL2	A2LL1	A2LL0
08H	LCMCA2RI	—	A2RM1	A2RM0	A2RL4	A2RL3	A2RL2	A2RL1	A2RL0
09H	LCMCDLI	DDEN	DLM1	DLM0	DLL4	DLL3	DLL2	DLL1	DLL0
0AH	LCMCDRI	ADEN	DRM1	DRM0	DRL4	DRL3	DRL2	DRL1	DRL0

Table 1. SC18075 Level and Channel Mux Control Registers

Location	Name	7	6	5	4	3	2	1	0
0BH	LOMVC	—	MVL6	MVL5	MVL4	MVL3	MVL2	MVL1	MVL0
0CH	ROMVC	—	MVR6	MVR5	MVR4	MVR3	MVR2	MVR1	MVR0

Table 2. SC18075 Master Volume Control Registers

Location	Name	7	6	5	4	3	2	1	0
0DH	LOBTTCR	TL3	TL2	TL1	TL0	BL3	BL2	BL1	BL0
0EH	ROBTTCR	TR3	TR2	TR1	TR0	BR3	BR2	BR1	BR0

Table 3. SC18075 Bass/Treble Tone Control Registers

Location	Name	7	6	5	4	3	2	1	0
0FH	CR1	AMR3	AMR2	AMR1	AMR0	AML3	AML2	AML1	AML0
10H	CR2	CLKSEL	LVPD	Mono/ Stereo	RLOUTC	LLOUTC	ENADC	SADC	ENDAC

Table 4. SC18075 Configuration Registers

LEVEL and CHANNEL MUX CONTROL REGISTERS

There are eleven level and channel mux control registers that control the level and the mux switch of the five stereo and one mono input channels. Upon poweron, all bits in the level and channel mux control registers will be reset to zero. This will set the attenuation level of all channels to 0 dB and will squelch all inputs to the left and right mixers. The registers are described as below:

Level and Channel Mux Control Telephone Input (LCMCTI), location 00H

Bit Number	Bit Name	Description
7		Not used. Should be reset to zero.
6–5	TM1–TM0	These bits control the mux prior to the mixer according to the following table:

TM1	TM0	STATE
0	0	Disconnect level control output of Telephone input from Left and Right mixer.
0	1	Connect level control output of Telephone input to Left mixer only.
1	0	Connect level control output of Telephone input to Right mixer only.
1	1	Connect level control output of Telephone input to both Right and Left mixer.

4–0 TL4–TL0 These bits adjust the attenuation level of the Telephone input according to the following table:

TL4	TL3	TL2	TL1	TL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040 dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

Level and Channel Mux Control Microphone Left Input (LCMCMLI), location 01H

Bit Number	Bit Name	Description
7		Not used. Should be reset to zero.
6–5	MLM1–MLM0	These bits control the mux prior to the mixer according to the following table:

MLM1	MLM0	STATE
0	0	Disconnect level control output of Microphone Left input from Left and Right mixer.
0	1	Connect level control output of Microphone Left input to Left mixer only.
1	0	Connect level control output of Microphone Left input to Right mixer only.
1	1	Connect level control output of Microphone Left input to Right and Left mixer.

4–0 MLL4–MLL0 These bits adjust the attenuation level of the Microphone Left input according to the following table:

MLL4	MLL3	MLL2	MLL1	MLL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040 dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

LEVEL and CHANNEL MUX CONTROL REGISTERS (continued)

Level and Channel Mux Control Microphone Right Input (LCMCMRI), location 02H

Bit Number	Bit Name	Description
7		Not used. Should be reset to zero.
6-5	MRM1–MRM0	These bits control the mux prior to the mixer according to the following table:

MRM1	MRM0	STATE
0	0	Disconnect level control output of Microphone Right input from Left and Right mixer.
0	1	Connect level control output of Microphone Right input to Left mixer only.
1	0	Connect level control output of Microphone Right input to Right mixer only.
1	1	Connect level control output of Microphone Right input to Right and Left mixer.

Bit Number	Bit Name	Description
4–0	MRL4–MRL0	These bits adjust the attenuation level of the Microphone Right input according to the following table:

MRL4	MRL3	MRL2	MRL1	MRL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

Level and Channel Mux Control External Left input (LCMCELI), location 03H

Bit Number	Bit Name	Description
7		Not used. Should be reset to zero.
6–5	ELM1–ELM0	These bits control the mux prior to the mixer according to the following table:

ELM1	ELM0	STATE
0	0	Disconnect level control output of External Left input from Left and Right mixer.
0	1	Connect level control output of External Left input to Left mixer only.
1	0	Connect level control output of External Left input to Right mixer only.
1	1	Connect level control output of External Left input to Right and Left mixer.

Bit Number	Bit Name	Description
4–0	ELL4–ELL0	These bits adjust the attenuation level of the External Left input according to the following table:

ELL4	ELL3	ELL2	ELL1	ELL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040 dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

LEVEL and CHANNEL MUX CONTROL REGISTERS (continued)

Level and Channel Mux Control External Right Input (LCMCERI), location 04H

Bit Number	Bit Name	Description
7		Not used. Should be reset to zero.
6–5	ERM1–ERM0	These bits control the mux prior to the mixer according to the following table:

ERM1	ERM0	STATE
0	0	Disconnect level control output of External Right input from Left and Right mixer.
0	1	Connect level control output of External Right input to Left mixer only.
1	0	Connect level control output of External Right input to Right mixer only.
1	1	Connect level control output of External Right input to Right and Left mixer.

Bit Number	Bit Name	Description
4–0	ERL4–ERL0	These bits adjust the attenuation level of the External Right input according to the following table:

ERL4	ERL3	ERL2	ERL1	ERL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040 dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

Level and Channel Mux Control Auxiliary1 Left Input (LCMCA1LI), location 05H

Bit Number	Bit Name	Description
7		Not used. Should be reset to zero.
6–5	A1LM1–A1LM0	These bits control the mux prior to the mixer according to the following table:

A1LM1	A1LM0	STATE
0	0	Disconnect level control output of Auxiliary1 Left input from Left and Right mixer.
0	1	Connect level control output of Auxiliary1 Left input to Left mixer only.
1	0	Connect level control output of Auxiliary1 Left input to Right mixer only.
1	1	Connect level control output of Auxiliary1 Left input to Right and Left mixer.

Bit Number	Bit Name	Description
4–0	A1LL4–A1LL0	These bits adjust the attenuation level of the Auxiliary1 Left input according to the following table:

A1LL4	A1LL3	A1LL2	A1LL1	A1LL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040 dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

LEVEL and CHANNEL MUX CONTROL REGISTERS (continued)

Level and Channel Mux Control Auxiliary1 Right Input (LCMCA1RI), location 06H

Bit Number	Bit Name	Description
7		Not used. Should be reset to zero.
6–5	A1RM1–A1RM0	These bits control the mux prior to the mixer according to the following table:

A1RM1	A1RM0	STATE
0	0	Disconnect level control output of Auxiliary1 Right input from Left and Right mixer.
0	1	Connect level control output of Auxiliary1 Right input to Left mixer only.
1	0	Connect level control output of Auxiliary1 Right input to Right mixer only.
1	1	Connect level control output of Auxiliary1 Right input to Right and Left mixer.

Bit Number	Bit Name	Description
4–0	A1RL4–A1RL0	These bits adjust the attenuation level of the Auxiliary1 Right input according to the following table:

A1RL4	A1RL3	A1RL2	A1RL1	A1RL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040 dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

Level and Channel Mux Control Auxiliary2 Left Input (LCMCA2LI), location 07H

Bit Number	Bit Name	Description
7		Not used. Should be reset to zero.
6–5	A2LM1–A2LM0	These bits control the mux prior to the mixer according to the following table:

A2LM1	A2LM0	STATE
0	0	Disconnect level control output of Auxiliary2 Left input from Left and Right mixer.
0	1	Connect level control output of Auxiliary2 Left input to Left mixer only.
1	0	Connect level control output of Auxiliary2 Left input to Right mixer only.
1	1	Connect level control output of Auxiliary2 Left input to Right and Left mixer.

Bit Number	Bit Name	Description
4–0	A2LL4–A2LL0	These bits adjust the attenuation level of the Auxiliary2 Left input according to the following table:

A2LL4	A2LL3	A2LL2	A2LL1	A2LL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040 dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

LEVEL and CHANNEL MUX CONTROL REGISTERS (continued)

Level and Channel Mux Control Auxiliary2 Right Input (LCMCA2RI), location 08H

Bit Number	Bit Name	Description
7		Not used. Should be reset to zero.
6–5	A2RM1–A2RM0	These bits control the mux prior to the mixer according to the following table:

A2RM1	A2RM0	STATE
0	0	Disconnect level control output of Auxiliary2 Right input from Left and Right mixer.
0	1	Connect level control output of Auxiliary2 Right input to Left mixer only.
1	0	Connect level control output of Auxiliary2 Right input to Right mixer only.
1	1	Connect level control output of Auxiliary2 Right input to Right and Left mixer.

Bit Number	Bit Name	Description
4–0	A2RL4–A2RL0	These bits adjust the attenuation level of the Auxiliary2 Right input according to the following table:

A2RL4	A2RL3	A2RL2	A2RL1	A2RL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040 dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

Level and Channel Mux Control DAC Left Input (LCMCDLI), location 09H

Bit Number	Bit Name	Description
7	DDEN	DAC Data ENable. This bit is used to set both DACs' inputs to logical one, disconnecting DACDATA pin from DACs. 0 = Normal operation. 1 = DAC inputs are set to one.
6–5	DLM1–DLM0	These bits control the mux prior to the mixer according to the following table:

DLM1	DLM0	STATE
0	0	Disconnect level control output of DAC Left input from Left and Right mixer.
0	1	Connect level control output of DAC Left input to Left mixer only.
1	0	Connect level control output of DAC Left input to Right mixer only.
1	1	Connect level control output of DAC Left input to Right and Left mixer.

Bit Number	Bit Name	Description
4–0	DLL4–DLL0	These bits adjust the attenuation level of the DAC Left input according to the following table:

DLL4	DLL3	DLL2	DLL1	DLL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040 dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

LEVEL and CHANNEL MUX CONTROL REGISTERS (continued)

Level and Channel Mux Control DAC Right Input (LCMCDRI), location 0AH

Bit Number	Bit Name	Description
7	ADEN	ADC Data ENable. This bit is used to set ADCDATA pin to logical one, disconnecting ADCs' outputs from ADCDATA pin. 0 = Normal operation. 1 = Set ADCDATA pin to one.
6–5	DRM1–DRM0	These bits control the mux prior to the mixer according to the following table:

DRM1	DRM0	STATE
0	0	Disconnect level control output of DAC Right input from Left and Right mixer.
0	1	Connect level control output of DAC Right input to Left mixer only.
1	0	Connect level control output of DAC Right input to Right mixer only.
1	1	Connect level control output of DAC Right input to Right and Left mixer.

Bit Number	Bit Name	Description
4–0	DRL4–DRL0	These bits adjust the attenuation level of the DAC Right input according to the following table:

DRL4	DRL3	DRL2	DRL1	DRL0	ATTENUATION
0	0	0	0	0	0.000 dB
0	0	0	0	1	1.505 dB
0	0	0	1	0	3.010 dB
0	0	1	0	0	6.020 dB
0	1	0	0	0	12.040 dB
1	0	0	0	0	24.080 dB
1	1	x	x	x	Mute (x is don't care)

MASTER VOLUME CONTROL REGISTERS

The chip has two 7-bit master volume control registers. One for the Left and the other for the Right channel of the stereo output. The master volume control has a 0–71.5 dB range, and the left and right channels can be adjusted independently. The adjustment size is 0.75 dB/step and one of the control code combinations will switch off the selected channel. Upon power-on all bits in the left and right volume control registers are set to high value. This will result in the two stereo channel analog outputs to be muted. The two registers are described as follows.

Left Output Master Volume Control (LOMVC), location 0BH

Bit Number	Bit Name	Description
7		Not used. Should be set to one.
6–0	MVL6–MVL0	The master volume control attenuation levels are listed in the following table:

MVL6	MVL5	MVL4	MVL3	MVL2	MVL1	MVL0	Attenuation
0	0	0	0	0	0	0	0.000 dB
0	0	0	0	0	0	1	0.752 dB
0	0	0	0	0	1	0	1.505 dB
0	0	0	0	1	0	0	3.010 dB
0	0	0	1	0	0	0	6.020 dB
0	0	1	0	0	0	0	12.040 dB
0	1	0	0	0	0	0	24.080 dB
1	0	0	0	0	0	0	48.165 dB
1	1	x	x	x	x	x	Mute

Right Output Master Volume Control (ROMVC), location 0CH

Bit Number	Bit Name	Description
7		Not used. Should be set to one.
6–0	MVR6–MVR0	The master volume control attenuation levels are listed in the following table:

MVL6	MVL5	MVL4	MVL3	MVL2	MVL1	MVL0	Attenuation
0	0	0	0	0	0	0	0.000 dB
0	0	0	0	0	0	1	0.752 dB
0	0	0	0	0	1	0	1.505 dB
0	0	0	0	1	0	0	3.010 dB
0	0	0	1	0	0	0	6.020 dB
0	0	1	0	0	0	0	12.040 dB
0	1	0	0	0	0	0	24.080 dB
1	0	0	0	0	0	0	48.165 dB
1	1	x	x	x	x	x	Mute

BASS/TREBLE TONE CONTROL REGISTERS

The chip has two 8-bit Bass/Treble Tone control registers. One for the Left and the other for the Right channel of the stereo output. Each Bass/Treble Tone control circuit has 15 settings, and the left and right channels can be adjusted independently. Upon power-on all bits in the two Bass/Treble tone control registers will be reset to zero, this will result in both tone control circuits to have a 0 dB flat loss. The two registers are described as follows:

Left Output Bass/Treble Tone Control Register (LOBTTCR), location 0DH

Bit Number	Bit Name	Description
7–4	TL3–TL0	These bits control the Treble tone control for the Left channel according to the following table:

TL3	TL2	TL1	TL0	MODE
0	0	0	0	Flat
0	0	0	1	Cut0
0	0	1	0	Cut1
0	0	1	1	Cut2
0	1	0	0	Cut3
0	1	0	1	Cut4
0	1	1	0	Cut5
0	1	1	1	Cut6
1	0	0	0	Flat
1	0	0	1	Boost0
1	0	1	0	Boost1
1	0	1	1	Boost2
1	1	0	0	Boost3
1	1	0	1	Boost4
1	1	1	0	Boost5
1	1	1	1	Boost6

Bit Number	Bit Name	Description
3–0	BL3–BL0	These bits control the Bass tone control for the Left channel according to the following table:

BL3	BL2	BL1	BL0	MODE
0	0	0	0	Flat
0	0	0	1	Cut0
0	0	1	0	Cut1
0	0	1	1	Cut2
0	1	0	0	Cut3
0	1	0	1	Cut4
0	1	1	0	Cut5
0	1	1	1	Cut6
1	0	0	0	Flat
1	0	0	1	Boost0
1	0	1	0	Boost1
1	0	1	1	Boost2
1	1	0	0	Boost3
1	1	0	1	Boost4
1	1	1	0	Boost5
1	1	1	1	Boost6

BASS/TREBLE TONE CONTROL REGISTERS (continued)

Right Output Bass/Treble Tone Control Register (ROBTTCR), location 0EH

Bit Number	Bit Name	Description
7–4	TR3–TR0	These bits control the Treble tone control for the Right channel according to the following table:

TR3	TR2	TR1	TR0	MODE
0	0	0	0	Flat
0	0	0	1	Cut0
0	0	1	0	Cut1
0	0	1	1	Cut2
0	1	0	0	Cut3
0	1	0	1	Cut4
0	1	1	0	Cut5
0	1	1	1	Cut6
1	0	0	0	Flat
1	0	0	1	Boost0
1	0	1	0	Boost1
1	0	1	1	Boost2
1	1	0	0	Boost3
1	1	0	1	Boost4
1	1	1	0	Boost5
1	1	1	1	Boost6

Bit Number	Bit Name	Description
3–0	BR3–BR0	These bits control the Bass tone control for the Right channel according to the following table:

BR3	BR2	BR1	BR0	MODE
0	0	0	0	Flat
0	0	0	1	Cut0
0	0	1	0	Cut1
0	0	1	1	Cut2
0	1	0	0	Cut3
0	1	0	1	Cut4
0	1	1	0	Cut5
0	1	1	1	Cut6
1	0	0	0	Flat
1	0	0	1	Boost0
1	0	1	0	Boost1
1	0	1	1	Boost2
1	1	0	0	Boost3
1	1	0	1	Boost4
1	1	1	0	Boost5
1	1	1	1	Boost6

CONFIGURATION REGISTERS

Two 8-bit registers set the configuration bits in the mixer chip. The description of the registers are as follows:

Configuration Register I (CR1), location 0FH

Bit Number	Bit Name	Description
7–4	AMR3–AMR0	These bits select the first input to the Right ADC summer. The inputs are selected from among Microphone Right, External Right, Auxiliary1 and Auxiliary2 Right inputs, Right DAC and Telephone inputs, or it is squeltched according to the following tables:

AMR1	AMR0	Mode
0	0	Squelch input
0	1	Select Right Aux1 input
1	0	Select Right Microphone input
1	1	Select Right External input

AMR3	AMR2	Mode
0	0	Squelch input
0	1	Select Right Aux2 input
1	0	Select Right DAC input
1	1	Select Telephone input

3–0	AML3–AML0	These bits select the first input to the Left ADC summer. The inputs are selected from among Microphone Left, External Left, Auxiliary1 and Auxiliary2 Left inputs, Left DAC and Telephone inputs, or it is squeltched according to the following tables:

AML1	AML0	Mode
0	0	Squelch input
0	1	Select Left Aux1 input
1	0	Select Left Microphone input
1	1	Select Left External input

AML3	AML2	Mode
0	0	Squelch input
0	1	Select Left Aux2 input
1	0	Select Left DAC input
1	1	Select Telephone input

CONFIGURATION REGISTERS (continued)

Configuration Register II (CR2), location 10H

The bits in this configuration register control the ADC switched-capacitor filters and the ADC and DAC. Upon power-on all bits in both configuration registers are reset to a low state. The bits are described as below:

Bit Number	Bit Name	Description
7	CLKSEL	Selects the FCLK frequency. 0 = Selects FCLK = 16.934 MHz 1 = Selects FCLK = 10.584 MHz
6	LVPD	Controls the power-down of the entire chip except for the ADCs and DACs. 0 = Normal (Powerup) 1 = Power-down
5	Mono/Stereo	In the mono mode the left and right outputs of the two mixers are summed to form the mono signal. 0 = Mono mode 1 = Stereo mode
4–3	LLOUTC, RLOUTC	Used to control the line output in the following form: LLOUTC: 0 = Mute Left Line output. LLOUTC: 1 = Enable Left Line output. RLOUTC: 0 = Mute Right Line output. RLOUTC: 1 = Enable Right Line output.
2	ENADC	Controls the dual 16-bit ADC. 0 = Disables both ADCs and the serial interface 1 = Enables both ADCs
1	SADC	This bit controls the bandwidth of the ADC antialiasing filters. The ADC switched-capacitor antialising filters use the ADCSRx48 clock divided by six as their clocks. This will correspond to a passband that is half the ADC sampling frequency. The SADC bit allows changing the passband to one fourth of the ADC sampling frequency. 0 = Passband of ADC antialiasing filter equal to half the sample rate. 1 = Passband of ADC antialiasing filter equal to one fourth of the sample rate.
0	ENDAC	Controls the dual 16-bit DAC. 0 = Disables both DACs and the serial interface 1 = Enables both DACs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	6 V
Supply Voltage, V_{SS}	–6 V
DC Input Voltage (Analog Signals)	V_{SS}–0.6 to V_{CC} +0.6 V
DC Input Voltage (Digital Signals)	V_{SS}–0.6 to V_{CC} +0.6 V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.
NOTE 2: Unless otherwise specified, all voltages are referenced to ground.
NOTE 3: Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Negative Supply Voltage		–4.5	–5.0	–5.5	V
GND	Ground			0		V
T_R, T_F	Input Rise or Fall Time	All digital inputs			5	ns

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = +5 V ± 10%, V_{SS} = –5 V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	Normal		60	80	mA
I_{SS}	Quiescent Current			60	80	mA
V_{IH}	High Level Input Voltage; Digital pinS		2.4		V_{DD}+.3	V
V_{IL}	Low Level Input Voltage; Digital pins		V_{SS}–.3		0.8	V
V_{OH}	High Level Output	I_{OH} = 1.6 mA I_{OH} = 100 µA		3.0 V_{DD}–.4		V
V_{OL}	Low Level Output	I_{OL} = 1.6 mA I_{OL} = 100 µA			0.8 0.4	V

AC ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic Range	SNR referenced to full scale, A-Weighted		78		dB
	Signal-to-(THD+N)	A-Weighted		0.02 74		% dB
	Signal-to-intermodulation distortion			90		dB
	ADC Crosstalk	Line Inputs (Input L, ground R, read R; input R, ground L, read L)		-80		dB
		Line to Mic (Input LINE ground and select MIC, read both channels)		-60		dB
		Line to AUX1		-60		dB
		Line to AUX2		-60		dB
	DAC Crosstalk	Input L, zero R, measure R_LOUT; input R, zero L, measure L_LOUT		-80		dB
	Gain Error	Full-scale span relative to nominal		5		%
	Differential Non-Linearity			±4		bits
	Integral Linearity			12		bits
	Resolution			16		bits
Analog Input	Input Voltage Line			6		V_{PP}
Analog Output	Full-Scale Output Voltage			6		V_{PP}
	External Load Capacitance			50		pF
	Output Impedance			600		ohms
	Mute Attenuation			-80		dB
	ADC THD+N	A-Weighted		0.15%		

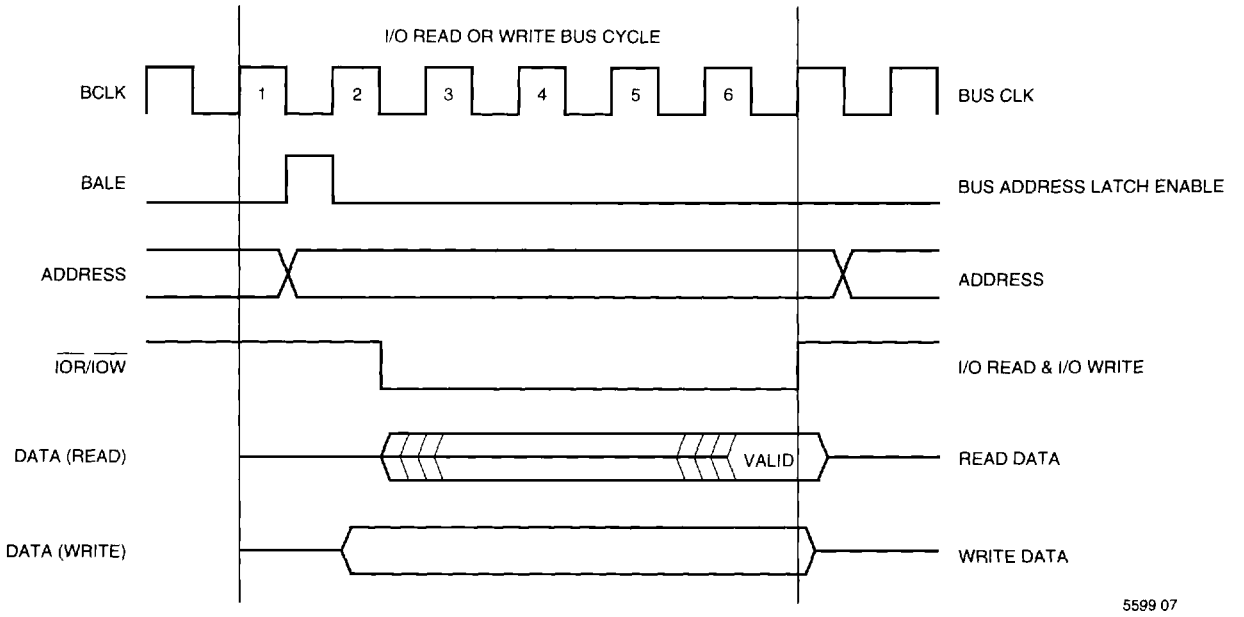
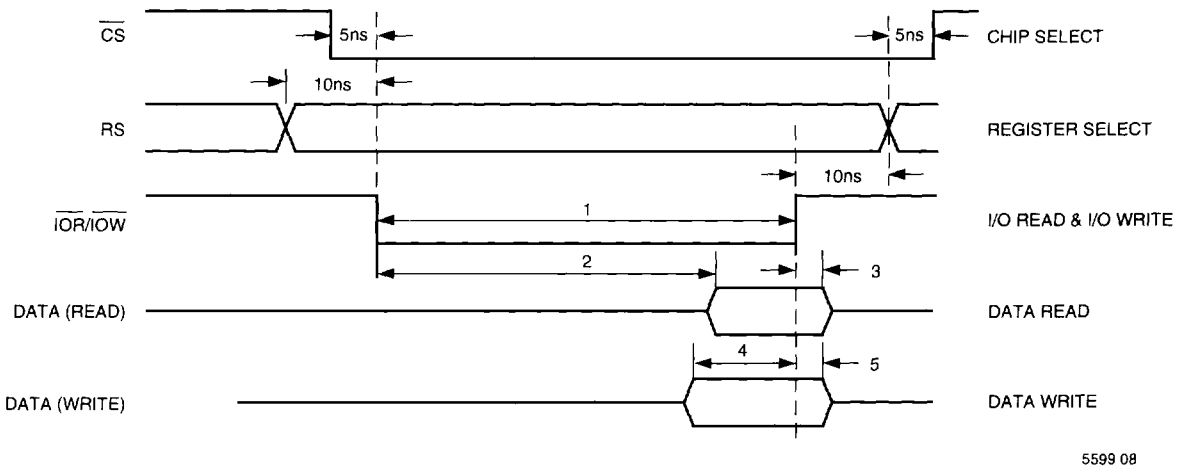


Figure 3. 8-Bit CPU I/O Access Cycles



NO.	SYMBOL	PARAMETER AND DESCRIPTION	MIN	TYP	MAX	UNITS
1		IOR or IOW pulse width low	42			ns
2		IOR asserted to data valid			25	ns
3		IOR negated to data bus tristated	0		16	ns
4		Write data setup	30			ns
5		Write data hold	10			ns
		Rise/fall times		5		ns
		Capacitive load on data pins			30	pF

NOTE: Back-to-back read/write instruction cycle—250 ns.

Figure 4. Read/Write Timing

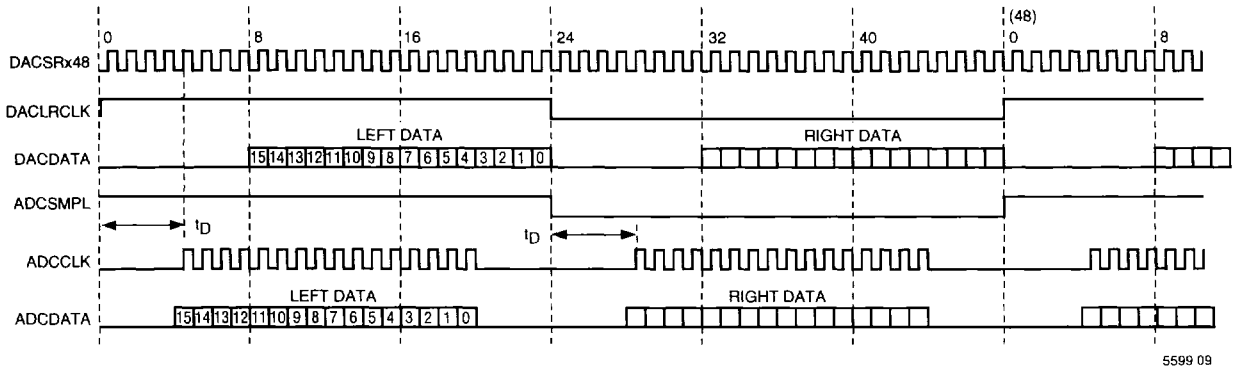


Figure 5a. DAC and ADC Timing Signals

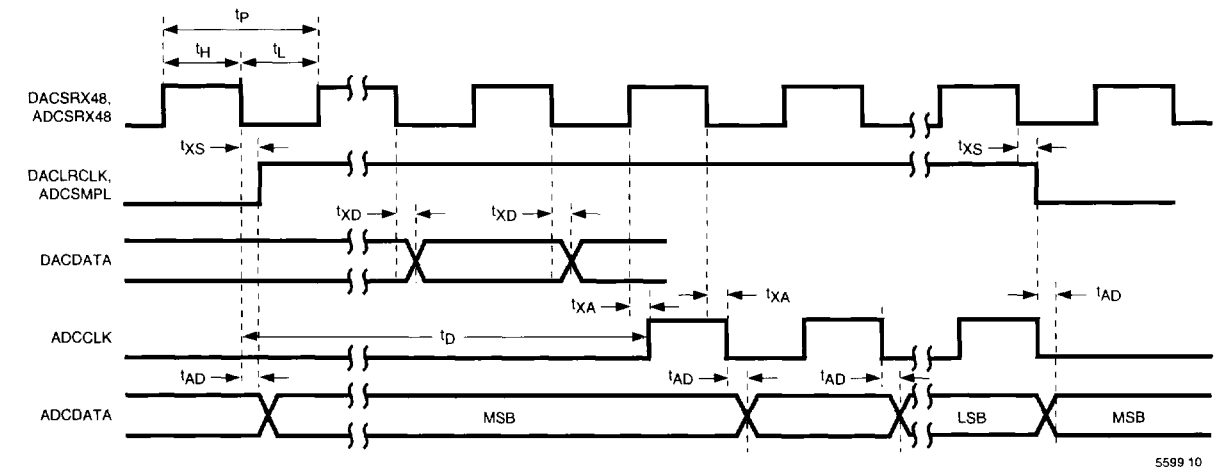


Figure 5b. ADC and DAC Timing Detail

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{XS}	DACLRCLK (ADCSMPL) rise or fall delay from falling edge of DACSRX48 (ADCSRX48)	0	70	ns
t_{XD}	DACDATA delay from falling edge of DACSRX48	0	100	ns
t_{XA}	ADCCLK (rise (fall) delay from ADCSRX48 rising (falling) edge	0	50	ns
t_{AD}	ADCCLK falling edge delay from rising or falling edge of ADCSMPL	0	180	ns
t_D	First rising edge delay from rising or falling edge of ADCSMPL ($t_D = 4.5\ t_P$)	2.12585	5.95238	µs
t_P	DACSRX48 (ADCSRX48) period	0.47241	1.32275	µs
F_{SMPL}	Clock frequency of DACLRCLK or ADCSMPL	15.75	44.1	KHz
	Duty cycle of clocks in Figure 5b	40	60	%

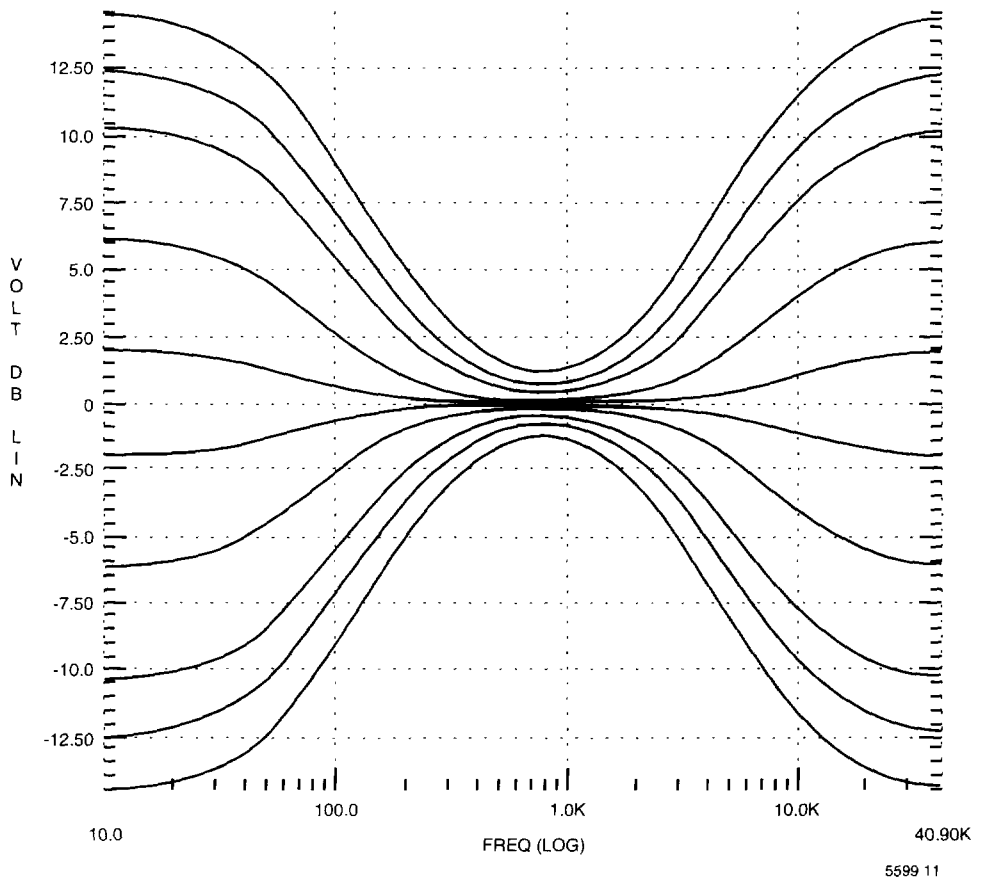


Figure 6. Bass/Treble Tone Control Frequency Response

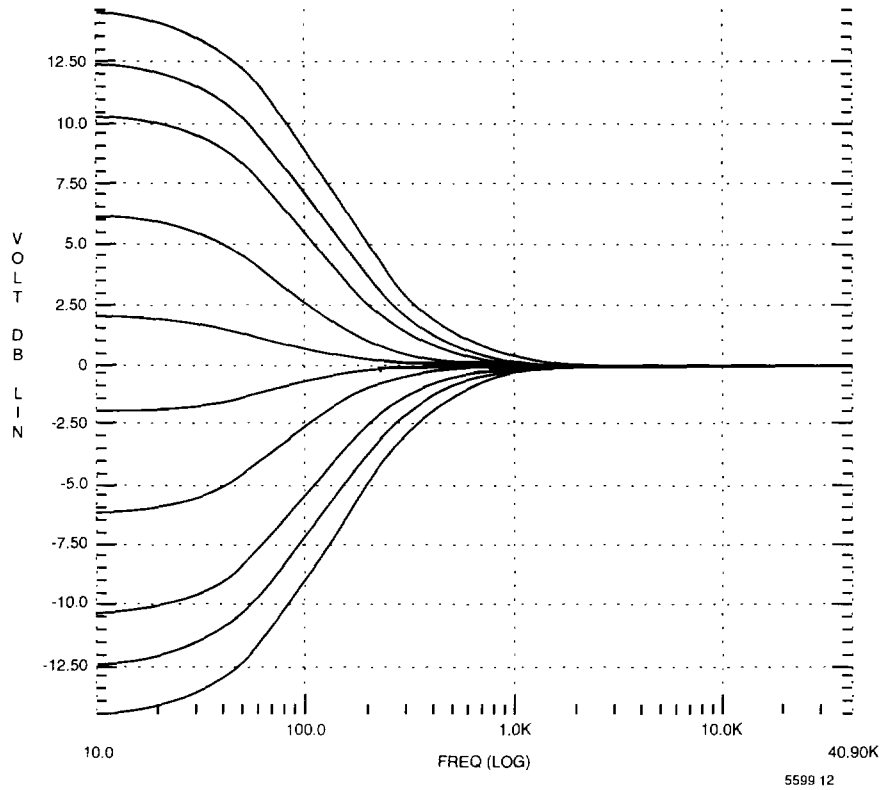


Figure 7. Bass Tone Control Frequency Response

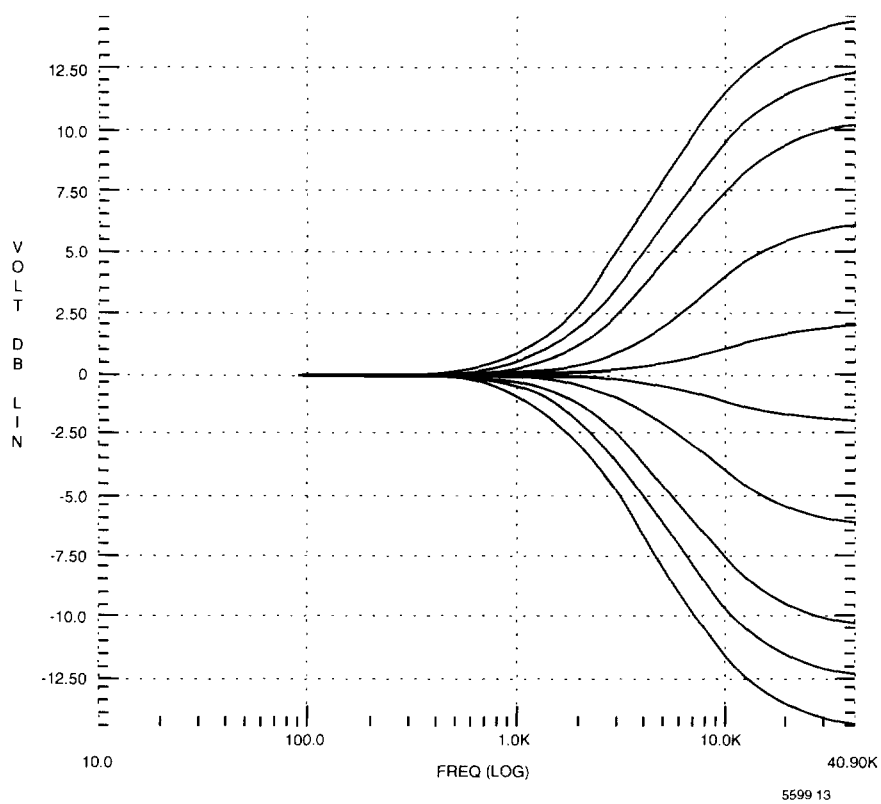


Figure 8. Treble Tone Control Frequency Response

SC11293CQ MODEM ANALOG FRONT END

This Modem Analog Front End (MAFE) is used with a Digital Signal Processor (DSP) to implement full duplex speaker phone data, Fax and voice modes.

One of the key features of the MAFE is the inclusion of circuitry to implement an adaptive hybrid. This circuitry, in conjunction with four external RC networks, will cancel the local echo by minimum of 20 dB. The adaptation process for the hybrid takes place during the training period of the echo canceller.

Band-split filters are also included to separate the receive and transmit signals, allowing the simple implementation of the V.22, V.22 bis, V.23, V.21 and Bell 212A/103 modes.

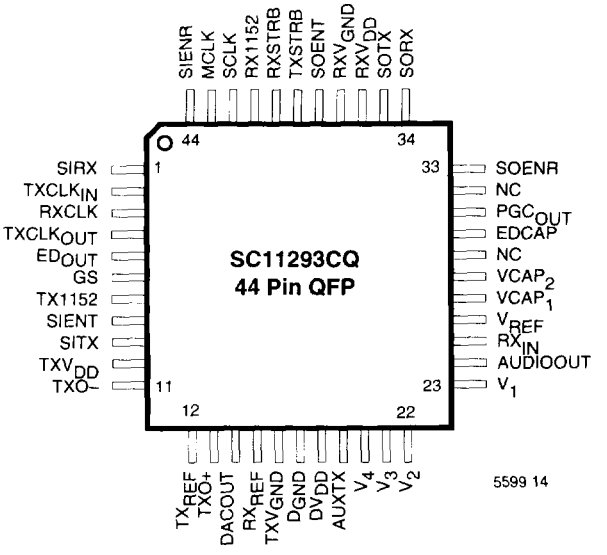
PIN DESCRIPTIONS – SC11293CQ – MAFE

PIN NAME	PIN NUMBER	DESCRIPTION
AUDIOOUT	24	Audio output. The analog receive signal is passed through a programmable gain/loss buffer to drive a speaker for line monitoring.
AUXTX	19	Transmit auxiliary input; analog signal.
DACOUT	14	Transmit DAC's sampled and held output; analog signal. This auxiliary output is used for trimming the 12-bit transmit DAC output.
DV_{DD}	18	Digital V_{DD}; V_{DD} = +5 V.
D_{GND}	17	Digital GND; D_{GND} = 0 V.
EDCAP	30	Energy detect capacitor; analog input. An external 0.1 µF capacitor should be connected between this pin and RX_{GND}.
ED_{OUT}	5	Energy detect output; when high, energy is detected. Same status as ED bit of the SOR pin.
GS	6	Gain Select to compensate for loss in line coupling transformer; input. When left open or tied to V_{DD} (5V), the compensation is +3dB; connected to ground (0V), the compensation is 0dB.
MCLK	43	Master clock; input. Must be 9.216 MHz. This clock generates various timing signals for the chip.
N/C	29, 32	Do not connect. (29 use for test only; this output indicates proper operating conditions)
PGC_{OUT}	31	Programmable gain-control section's sampled and held output; analog signal.
RXCLK	3	Receive data clock; output. This signal which is generated internally by receive phase-locked loop provides timing for receive data stream.
RX_{IN}	25	Receive input; analog signal.
RX_{REF}	15	Receive analog REF; RX_{REF} =2.5 V.
RXSTRB	40	Receive strobe; input/output. This pin will be input if RSINT in receive interface is low, otherwise it will be an output. The falling edge of this signal will trigger the receive ADC.
RXS1152	41	Output. This pin provides a clock frequency which is 1.152 MHz and synchronous to RXCLK.
RXV_{DD}	36	Receive analog V_{DD}; RXV_{DD} = +5V.
RXV_{GND}	37	Receive analog GND; RXV_{GND} = 0V.
SCLK	42	Shift clock; output and its frequency is 1/4 of the MCLK. This clock is used for serially shifting data in or out of the chip.

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER	DESCRIPTION
SIENR	44	Receive serial input enable; input. A positive pulse on this input allows the serial data on SIR pin to enter the receive interface register.
SIENT	8	Transmit serial input enable; input. A positive pulse on this input allows the serial data on SIT to enter the transmit interface register.
SIRX	1	Receive serial input; input. Data is shifted serially into a 16-bit register with MSB entering first. If additional bits are sent in, they will be ignored.
SITX	9	Transmit serial input; input. Data is shifted serially into a 16-bit register with MSB entering first. If additional bits are sent in, they will be ignored.
SOENR	33	Receive serial output enable; output. A positive pulse on this pin enables the data stored in receive output register to be serially shifted out through SORX pin.
SOENT	38	Transmit serial output enable; output. A positive pulse on this pin enables the data stored in the transmit register to be serially shifted out through SOTX pin.
SORX	34	Receive serial output; output. Data is shifted in 13-bit blocks. The first 12-bit correspond to ADC data. Bit 13 (ED) indicates the status of energy detect.
SOTX	35	Transmit serial output; output. During each transmit strobe cycle, this pin outputs two blocks of data. First one carries echo signal information and the second one corresponds to adaptive hybrid output.
$TXCLK_{IN}$	2	Transmit clock input; input. This is the external timing source which transmit phase-locked loop locks into.
$TXCLK_{OUT}$	4	Transmit data clock; output. This signal which is generated internally by transmit phase-locked loop provides timing for transmit data stream.
TXO+	13	Positive transmit output; analog signal.
TXO–	11	Negative transmit output; analog signal.
TX_{REF}	12	Transmit analog REF; TX_{REF} = 2.5 V.
TXSTRB	39	Transmit strobe; input/output. This pin will be input if TSIN/EX in transmit input interface is low otherwise, it will be an output. Falling edge of this signal triggers the transmit DAC and echo canceller ADC.
TXS1152	7	Output. This pin provides a clock frequency which is 1.152 MHz and synchronous to $TXCLK_{OUT}$.
TXV_{DD}	10	Transmit analog V_{DD}; TXV_{DD} = +5 V.
TXV_{GND}	16	Transmit analog GND; TXV_{GND} = 0 V.
V_1–V_4	23–20	Four inputs to the adaptive hybrid; analog signal.
$VCAP_1$, $VCAP_2$	27, 28	An external 0.1µF capacitor is required between the two pins. This capacitor together with an internal 25 kΩ resistor forms a high-pass filter that removes the DC component of the signal before entering the PGC.
V_{REF}	26	Reference voltage; analog signal. V_{REF} = 2.5V

CONNECTION DIAGRAMS



NOTE: Pinouts subject to change without notice.

SC11351 Digital Signal Processor (DSP)

The SC11351 performs all of the digital signal processing functions of the data pump. The SC11351 is a 5 volt CMOS part and is available in a 80 pin PQFP. All interface pins are CMOS.

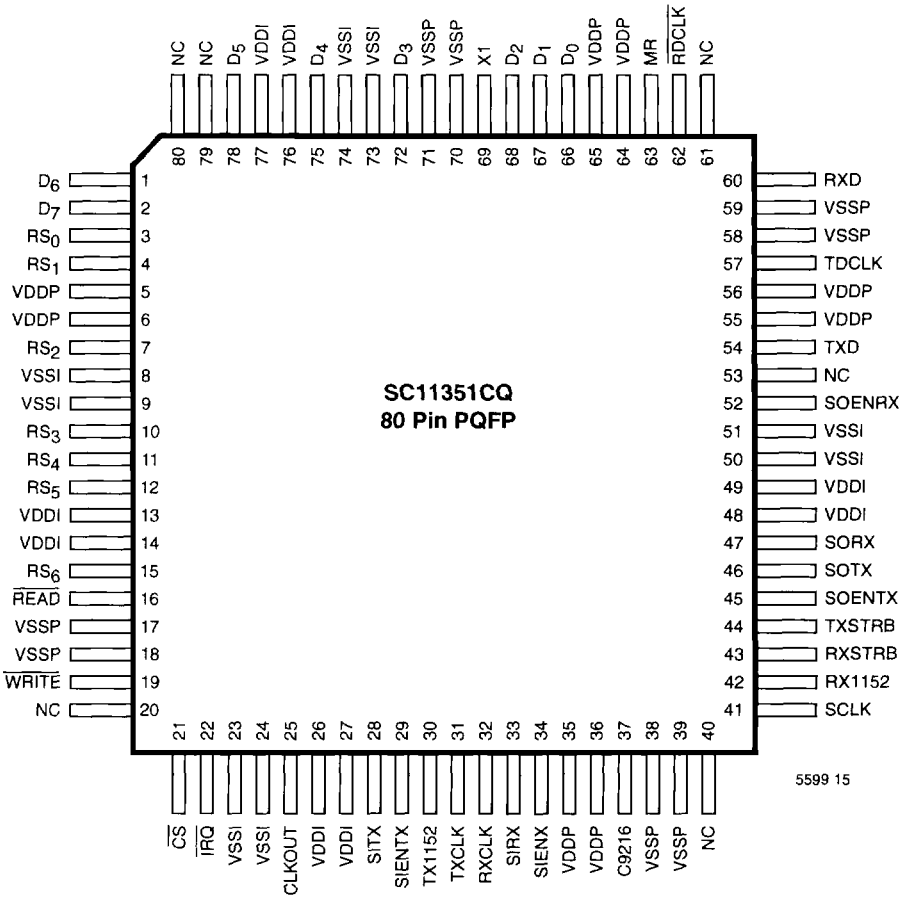
Pin Descriptions – SC11351CQ DSP

PIN NAME	PIN NUMBER	DESCRIPTION
C9216	37	**OUTPUT.** 9.216 MHz clock output for AFE.
CLKOUT	25	**OUTPUT.** 39.3216 MHz clock output.
$\overline{CS}$	21	**INPUT.** Host DPRAM chip select, active low.
D0,1,2,3 4,5,6,7	66, 67, 68,72, 75, 78,1,2	**INPUT/OUTPUT, TTL.** 8 bit data bus.
$\overline{IRQ}$	22	**OUTPUT.** Interrupt request. Open drain with internal 80K pullup.
MR	63	Master Reset. Active high.
N/C	20, 40, 53, 61, 79, 80	Do not connect to GND or VCC. Do not use.
$\overline{RDCLK}$	62	**OUTPUT.** Receive data clock.
$\overline{READ}$	16	**INPUT.** Host read enable.
RS0,1,2 3,4,5,6	3, 4, 7, 10, 11, 12, 15	**INPUT.** Host address bus.
RX1152	42	**INPUT.** 1.152 MHz receive clock.
RXCLK	32	**INPUT.** Receive clock.
RXD	60	**OUTPUT.** Receive data.
RXSTRB	43	**INPUT.** Receive strobe.
SCLK	41	**INPUT.** Transmit/Receive serial port clock.
SIENRX	34	**INPUT.** Receive serial data input enable.
SIENTX	29	**INPUT.** Transmit serial data input enable.
SIRX	33	**INPUT.** Receive serial data input.
SITX	28	**INPUT.** Transmit serial data input.
SOENRX	52	**OUTPUT.** Receive serial data output enable.
SOENTX	45	**OUTPUT.** Transmit serial data output enable.
SORX	47	**OUTPUT.** Receive serial data output.
SOTX	46	**OUTPUT.** Transmit serial data output.
TDCLK	57	**OUTPUT.** Transmit data clock.
TX1152	30	**INPUT.** 1.152 MHz transmit clock.
TXCLK	31	**INPUT.** Transmit clock.
TXD	54	**INPUT.** Transmit data.
TXSTRB	44	**INPUT.** Transmit strobe.
VDDI	13, 14, 26, 27, 48, 49, 76, 77	**VDD.** (+5V)
VDDP	5, 6, 35, 36, 55, 56, 64, 65	**VDD.** (+5V)

Pin Descriptions – SC11351 DSP (continued)

PIN NAME	PIN NUMBER	DESCRIPTION
VSSI	8, 9, 23, 24, 50, 51, 73, 74	**VSS for core.** (GND)
VSSP	17, 18, 38, 39, 58, 59, 70, 71	**VSS.** (GND)
$\overline{\text{WRITE}}$	19	**INPUT.** Host write enable.
X1	69	**INPUT.** Accepts 39.3216 MHz crystal oscillator output from MAC.

CONNECTION DIAGRAMS



TYPICAL POWER CONSUMPTION

	OPERATING
SQ3265CT	750 mW

ELECTRICAL SPECIFICATIONS – SC11293 Analog Front End (AFE)

Absolute Maximum Ratings (Notes 1, 2 and 3)

V_{DD} Supply Voltage	6V
Input Signals with Respect to Ground	V_{SS} – 0.6V to V_{DD} + 0.6V
Operating Temperature Range	0 to +70°C
Storage Temperature Range	-65 to 150°C
Lead Temperature (Soldering 10 sec)	300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.
NOTE 2: Power dissipation temperature derating — Plastic Package: –12 mW/C from 65°C to 85°C.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{DD} = +5V ± 10%, V_{SS} = RXGND = GND)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Quiescent Current			19	30	mA
V_{IH}	High Level Input Voltage; Digital Pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital Pins				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Output (I_{OL} = 1.6 mA)				0.6	V
V_{OM}	Maximum Peak Output Level on TxOUT Pin	R_L = 600 Ω Referenced to TX_{REF} pin	±1.5			V
V_{IM}	Maximum Peak Level on RX_{IN} Pin	Referenced to RX_{REF} pin			±1.5	V

ELECTRICAL SPECIFICATIONS (SC11351, SC11951, SC11140)

Absolute Maximum Ratings (Notes 1, 2)

V_{CC} Supply Voltage	+6V
Input Signals with Respect to Ground	-0.6V to V_{CC} + 0.6V
Operating Temperature Range	0 to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering for 10 sec)	+300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.
NOTE 2: Power dissipation temperature derating — Plastic Package: –12 mW/C from 65°C to 85°C.

DC Electrical Characteristics (T_A = 0 to 70°C, V_{CC} = +5V ± 10%, GND = 0V)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I_{CC}	Nominal Operating Current @ V_{CC} = 5.0 V, F_{CLK} = 39 MHz SC11951 only		65		mA
I_{CC}	Nominal Operating Current @ V_{CC} = 5.0 V, F_{CLK} = 39 MHz SC11351 only		60		mA
I_{CCPD}	Power Down Current @ V_{CC} = 5.0 V, F_{CLK} = 39 MHz SC11351 only		10		mA
V_{IH}	High Level Input Voltage for TTL input pins for CMOS input pins	 2 0.8 V_{CC}			 V V
V_{IL}	Low Level Input Voltage for TTL input pins for CMOS input pins			 0.7 0.2 V_{CC}	 V V
VT+	Positive Hysteresis Threshold for RESET & RI input pins	2.6	2.8	3.4	V
VT–	Negative Hysteresis Threshold for RESET & RI input pins	1.8	2.2	2.5	V
V_{OH}	High Level Output Voltage for D7–D0, INT0 @ I_{OH} = 8 mA for RDY—open collector for other output pins @ I_{OH} = 2 mA	2.4			 V
V_{OL}	Low Level Output Voltage for D7–D0, INT0 pins @ I_{OL} = 8 mA for RDY @ I_{OL} = 8 mA for other output pins @ I_{OL} = 2 mA			0.4	 V
I_1	Leakage Current		±1	±20	µA
F_{CLK}	Crystal Clock Frequency	±0.005%	39.3216	±0.005%	MHz

SYSTEM INTERFACES

Clock

The chip set needs only a single 39.3216 MHz clock. The SC11951 provides this clock with an on-board oscillator circuit requiring an external crystal. The CKOUT pin of the SC11951 provides the 39.3216 MHz clock for the SC11351. The 9.216 MHz clock for the SC11293 is generated by the SC11351.

The specification for the 39.3216 MHz crystal is shown in Table 1.

Approved parts:
SaRonix SRX5515
TXC 148-3932A-2001

DSP Memory

The DSP has three sets of internal memory—ROM for the receive program, ROM for the transmit program and SRAM for bulk delay.

Controller Memory

A 32K X 8 SRAM with 90 nS access time is required if V.42bis and/or voice functions are to be implemented.

A 128K X 8 EPROM is used in the FastTrack demo board and accomodates all the features that are available at this time. The access time of this memory must be 90 nS max.

A 64K x 8 EPROM is used in applications only requiring Class I fax, and no voice.

DAA

The Data Access Arrangement (DAA) connects the SC11293 AFE to the RJ11 phone jacks and thus to the telephone line. The primary function of the DAA is to isolate the modem from the telephone line so the modem will not harm the GSTN. This isolation is mandated by the FCC, Telephone Operating Companies (PTT) and UL.

The recommended transformer for high speed modem DAA's, used in the *FastTrack*™ Kits, is one that has no DC current/loop current (dry transformer) flowing in the primary winding. A dry transformer, with the same equivalent size as a wet transformer, can be designed with better amplitude, frequency and phase characteristics.

Relays are used for on/off hook, voice mode and Caller ID functions. A MOV provides protection from telephone line transients. Inductor-capacitor networks prevent frequencies generated by the modem from being transmitted into the telephone line (limits are specified in Code of Federal Regulations TITLE 47 PART 15B).

Host Bus Interface

The interface to the host PC consists of a COM PORT (COM1 to COM4) interface and a Direct Memory Access (DMA) interface. The 16C550 compatible UART in the SC11951 is connected to the PC COM PORT using a generate a DMA request signal, for data transfer, and force the selection of the scratchpad register (STR) in the 16C550. The PC then issues a DMA acknowledgment that allows STR to be used for DMA.

Serial EEPROM

The SC11951 will address a 2K X 1 serial EEPROM that is required for non-volatile storage of telephone numbers and modem settings.

T.I.E.S.

Time Independent Escape Sequence (T.I.E.S.) is an in-band escape sequence that allows the modem to escape from the data mode to the command mode. The escape command is identical to that used by Hayes. The escape character is normally a + (default setting), however, it can be changed using S-Register S2. T.I.E.S. provides the same results and reliability as the Hayes patented time dependent escape sequence, but without requiring a license or royalty. T.I.E.S. is the default setting in Sierra controller firmware. It can be changed, however, to the time dependent escape sequence for those who prefer and have a license to the Hayes patented technology.

Hayes is a trademark of Hayes Microcomputer Systems

Operating Temperature Range	-20°C to +70°C
Frequency Temperature Stability	± 0.005% from -20°C to +70°C
Specifications at 25°C ± 2°C	
Frequency	39.321600 MHz
Frequency Calibration Tolerance	0.005% (50 ppm)
Load Capacitance	12 pF
Effective Series Resistance	40Ω max.
Drive Level—correlation/operating	0.5 mW
Shunt Capacitance	5.5 pF max.
Oscillation Mode	3rd overtone
Test Circuit	Saunders 150C
Mechanical Holder Type	HC-49/U
Mechanical Dimensions	
Height	13.46 mm max.
Width	11.80 mm max.
Depth	4.64 mm max.
Lead Length	12.70 mm min.
Lead Spacing	4.88 mm
Lead Diameter	0.43 mm

Table 1. Specifications for 39.3216 MHz Crystal

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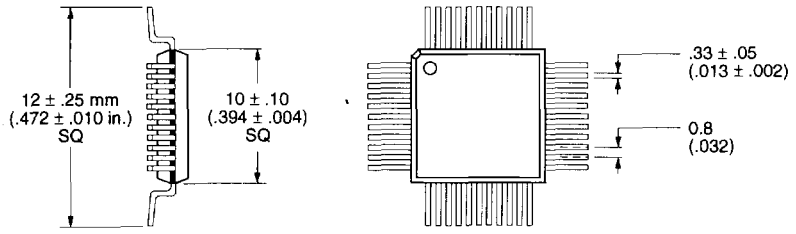
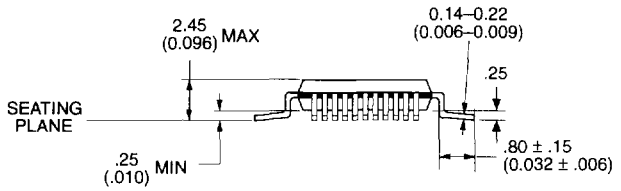
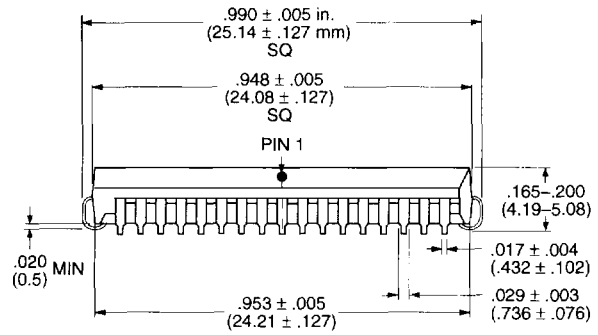
SC11293CQ – 44-Pin Plastic Quad Flat Pack (10mm)

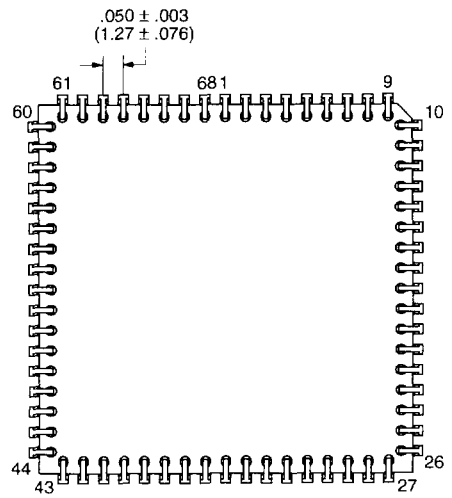




NOTE: All dimensions are in millimeters with (English-inch) conversion in parentheses. In case of conflict, metric dimensions govern.

SC18075CV – 68-Lead Plastic Chip Carrier

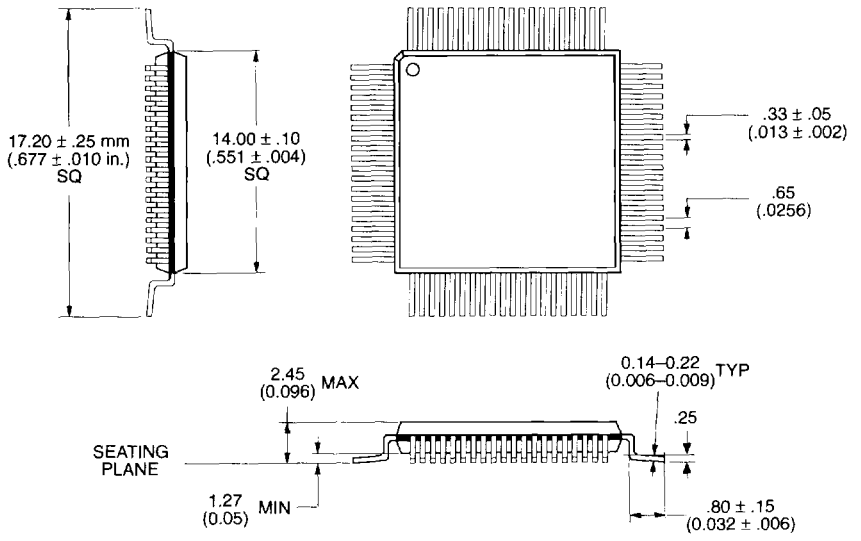




(BOTTOM VIEW)

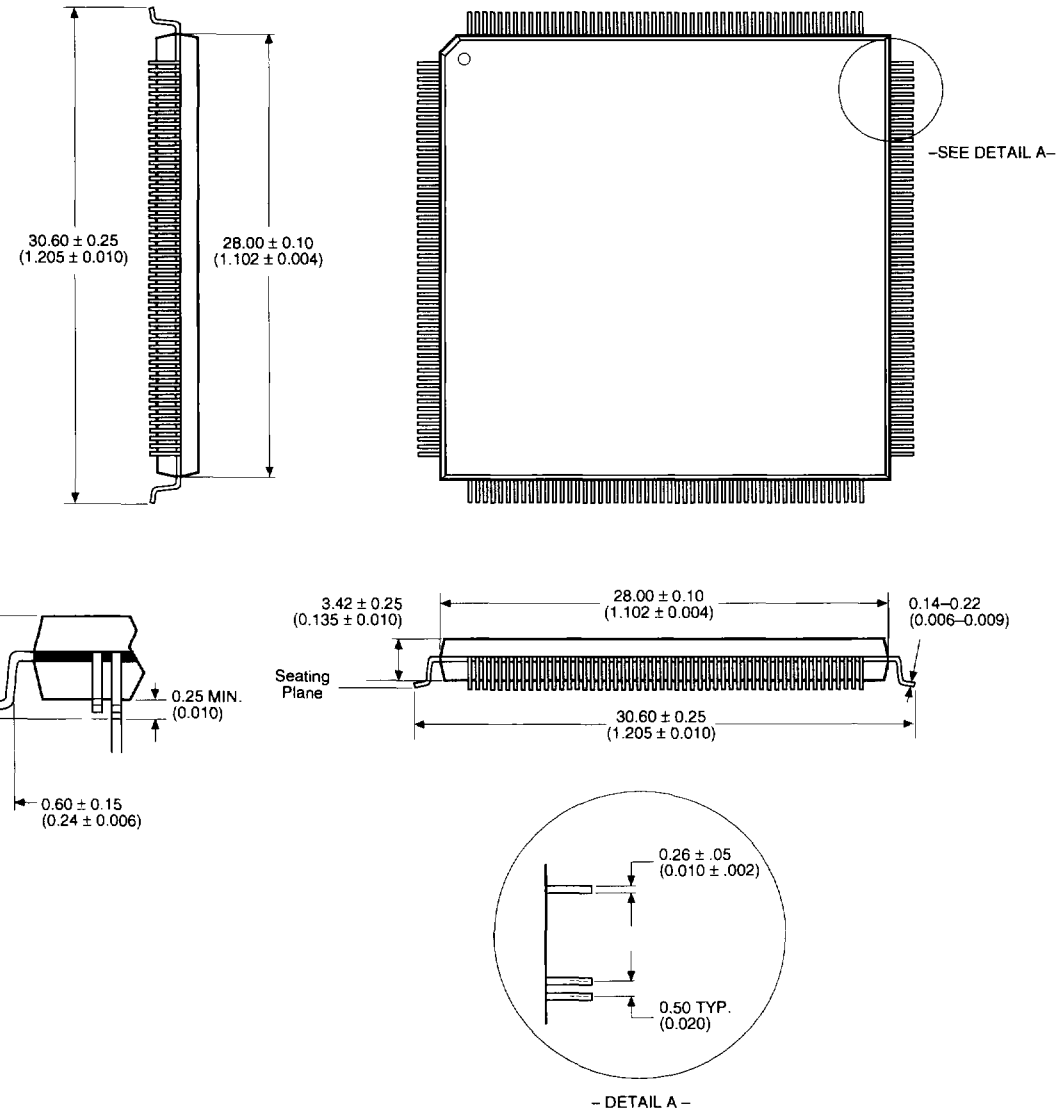
NOTE: All dimensions are in inches with (Metric-mm) conversion in parentheses. In case of conflict, English dimensions govern.

SC11351CQ – 80-Pin Plastic Quad Flat Pack (14mm)



NOTE: All dimensions are in millimeters with (English-inch) conversion in parentheses. In case of conflict, metric dimensions govern.

SC11954CQ – 208-Lead Plastic Quad Flat Pack



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