Chapter 5

Electrical Specifications

Electrical specifications for the TI486 are provided in this chapter. The specifications include electrical connection requirements for all package pins, maximum ratings, recommended operating conditions, dc electrical, and ac characteristics.

Electrical connection requirements provides the designer with specific requirements for power and ground connections decoupling, termination of inputs having internal pullup/pulldown resistors, termination of system functional inputs requiring external pullup resistors, termination of unused inputs, and termination of inputs designated NC.

The absolute maximum ratings provide the designer with specific limits regarding power supply and input voltages, input and output current limits, and operating and storage temperatures.

Recommended operating conditions provide the designer with specific values for power supply and input voltages, required input threshold ranges, output drive currents available for system interfacing, and operating levels for clamp currents and case temperature.

The dc electrical characteristics provides specific data regarding the capabilities of the TI486 devices to interface directly with either CMOS or TTL type system functions.

The ac characteristics provide detailed information regarding measurement points, specific timing requirements for setup and hold times, and propagation delay times of the TI486 processors.

Topic **Page**

5.1 Electrical Connections

5.1.1 Power and Ground Connections and Decoupling

Due to the high frequency operation of the TI486, it is necessary to install and test this device using standard high-frequency techniques. The high clock frequencies used in the TI486 and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the dc power leads with low-inductance decoupling capacitors, using low-impedance wiring, and by connecting all of the V_{CC} and GND (V_{SS}) pins. There are 14 V_{CC} and 18 Vss pins on the 100-pin quad flat package, and 20 V_{CC} and 21 V_{SS} pins on the 132-pin pin grid array package.

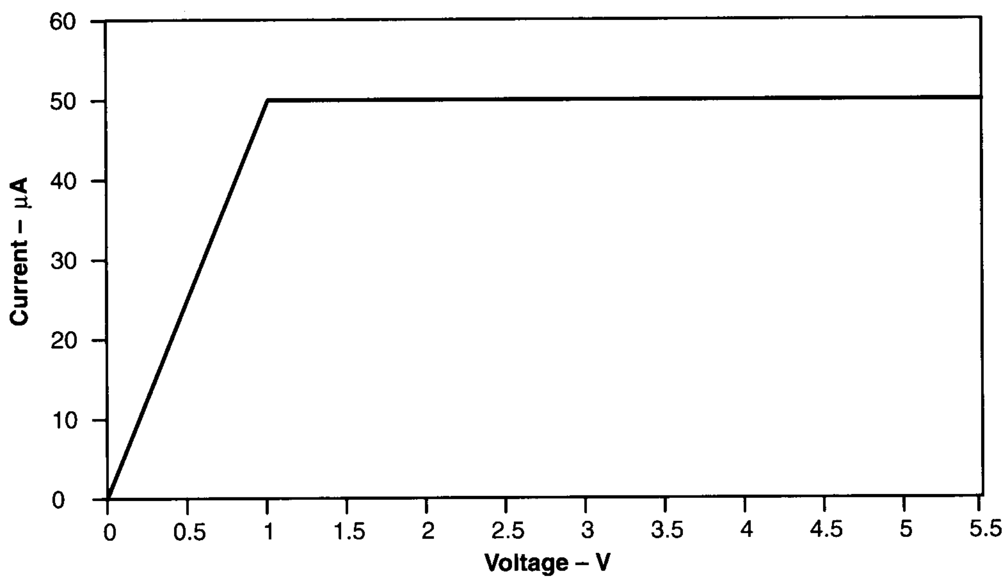
5.1.2 Pullup/Pulldown Resistors

Table 5–1 lists the input pins that are internally connected to pullup and pulldown resistors (See Figure 5–1). The pullup resistors are connected to V_{CC} and the pulldown resistors are connected to V_{SS}. When unused, these inputs do not require connection to external pullup or pulldown resistors.

Table 5–1. Pins Connected to Internal Pullup and Pulldown Resistors

SIGNAL	TI486SLC/E PIN	TI486DLC/E PIN	RESISTOR
$\overline{\text{A20M}}$	31	F13	pullup
$\overline{\text{BUSY}}$	34	B9	pullup
$\overline{\text{ERROR}}$	36	A8	pullup
$\overline{\text{FLT}}$	28	–	pullup
$\overline{\text{FLUSH}}$	30	E13	pullup
$\overline{\text{KEN}}$	29	B12	pullup
PEREQ	37	C8	pulldown
$\overline{\text{SMI}}$	47	C7	pullup
$\overline{\text{SUSP}}$	43	A4	pullup

Figure 5–1. Internal Pullup/Pulldown-IV Characteristic



It is recommended that the $\overline{ADS}$ and $\overline{LOCK}$ output pins be connected to pullup resistors, as indicated in Table 5–2. The external pullups guarantee that the signals will remain negated during hold acknowledge states.

Table 5–2. Pins Requiring External Pullup Resistors

SIGNAL	TI486SLC/E PIN	TI486DLC/E PIN	EXTERNAL RESISTOR
$\overline{ADS}$	16	E14	20-kΩ pullup
$\overline{LOCK}$	26	C10	20-kΩ pullup

5.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 5–1 should be connected either to ground or to V_{CC}. Connect active-high inputs to ground through a 20-kΩ (± 10%) pulldown resistor and active-low inputs to V_{CC} through a 20-kΩ (± 10%) pullup resistor to prevent possible spurious operation.

5.1.4 NC Designated Pins

Pins designated NC should be left disconnected. Connecting an NC pin to a pullup resistor, pulldown resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

5.2 Absolute Maximum Ratings

Table 5–3 specifies the absolute maximum ratings for the TI486SLC/E, TI486SLC/E-V, TI486DLC/E, and TI486DLC/E-V microprocessors.

Table 5–3. Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

PARAMETER		MIN	MAX	UNIT
Supply voltage, V_{CC}	With respect to V_{SS}	–0.5	6.5	V
Voltage on any pin	With respect to V_{SS}	–0.5	V_{CC}+0.5	V
Input clamp current, I_{IK}	Power applied		10	mA
Output clamp current, I_{OK}	Power applied		25	mA
Case temperature	Power applied	–65	110	°C
Storage temperature	No bias	–65	150	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.3 Recommended Operating Conditions

Table 5–4 and Table 5–5 presents the recommended operating conditions for the TI486SLC/E, TI486SLC/E-V, TI486DLC/E, and TI486DLC/E-V processors.

Table 5–4. TI486 SLC/E Recommended Operating Conditions

PARAMETER			TI486SLC/E		TI486SLC/E-V		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	With respect to V_{SS}	4.75	5.25	3	3.6	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	–0.3	0.6	V
V_{ILC}	CLK2 low-level input voltage		–0.3	0.8	–0.3	0.5	V
V_{IHC}	CLK2 high-level input voltage		3.7	V_{CC}+0.3	V_{CC}–0.5	V_{CC}+0.3	V
I_{OH}	High-level output current	$V_{OH}=V_{OH(min)}$		–1		–1	mA
I_{OL}	Low-level output current	$V_{OL}=V_{OL(max)}$		5		3	mA
I_{IK}	Input clamp current	$V_{IN}<V_{SS}$ or $V_{IN}>V_{CC}$		10		10	mA
I_{OK}	Output clamp current	$V_{OUT}<V_{SS}$ or $V_{OUT}>V_{CC}$		25		25	mA
t_c	Case temperature	Power applied	0	100	0	85	°C

Table 5–5. TI486DLC/E Recommended Operating Conditions

PARAMETER			TI486DLC/E		TI486DLC/E-V		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	With respect to V_{SS}	4.75	5.25	3	3.6	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	–0.3	0.6	V
V_{ILC}	CLK2 low-level input voltage		–0.3	0.8	–0.3	0.5	V
V_{IHC}	CLK2 high-level input voltage		3.7	V_{CC}+0.3	V_{CC}–0.5	V_{CC}+0.3	V
I_{OH}	High-level output current	$V_{OH}=V_{OH(min)}$		–1		–1	mA
I_{OL}	Low-level output current	$V_{OL}=V_{OL(max)}$		5		3	mA
I_{IK}	Input clamp current	$V_{IN}<V_{SS}$ or $V_{IN}>V_{CC}$		10		10	mA
I_{OK}	Output clamp current	$V_{OUT}<V_{SS}$ or $V_{OUT}>V_{CC}$		25		25	mA
t_c	Case temperature	Power applied	0	85	0	85	°C

5.4 DC Electrical Characteristics

Table 5–6 and Table 5–7 presents the dc electrical characteristics for the TI486SLC/E, TI486SLC/E-V, TI486DLC/E, and TI486DLC/E-V processors.

Table 5–6. TI486SLC/E DC Electrical Characteristics at Recommended Operating Conditions (Typical values are at nominal V_{CC} (5 V or 3.3 V) and $T_A = 25°C$)

PARAMETER		TEST CONDITIONS	TI486SLC/E			TI486SLC/E-V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	Low-level output voltage	I_{OL} = 3 mA						0.35	V
		I_{OL} = 5 mA			0.45				
V_{OH}	High-level output voltage	I_{OH} = –1 mA	2.4			V_{CC}–0.4			V
		I_{OH} = –0.2 mA	V_{CC}–0.5			V_{CC}–0.4			
I_I	Input current (leakage)	0 < V_{IN} < V_{CC}, See Note 1			±15			±15	µA
I_{IH}	High-level input current at PEREQ	V_{IN} = 2.4, See Note 2			200			200	µA
I_{IL}	Low-level input current	V_{IL} = 0.45 V, See Note 3			–400			–400	µA
I_{CC}	Supply current (Active mode)	25 MHz (CLK2 = 50 MHz)		395	495		225	285	mA
		33 MHz (CLK2 = 66 MHz)		495	615		—	—	
I_{CCSM}	Supply current (Suspend mode)	25 MHz (CLK2 = 50 MHz)		9	15		6	10	mA
		33 MHz (CLK2 = 66 MHz)		10	18		—	—	
I_{CCSS}	Standby supply current	0 MHz, Suspended/ CLK2 stopped, See Note 3		0.4	2		0.3	2	mA
C_{IN}	Input capacitance	f_C = 1 MHz, See Note 5			10			10	pF
C_{OUT}	Output or I/O capacitance	f_C = 1 MHz, See Note 5			12			12	pF
C_{CLK}	Input capacitance CLK2	f_C = 1 MHz, See Note 5			20			20	pF

Notes:
1) Applicable for all input pins except those listed in Note 3.
2) PEREQ input has an internal pulldown resistor.
3) Applicable for $\overline{A20M}$, $\overline{BUSY}$, $\overline{ERROR}$, $\overline{FLT}$, $\overline{FLUSH}$, $\overline{KEN}$, $\overline{SMI}$, and $\overline{SUSP}$ inputs that have an internal pullup resistor.
4) All inputs at 0.4 or V_{CC}–0.4 (CMOS levels). All inputs held static, (except CLK2 as indicated). All outputs unloaded (static I_{OUT} = 0 mA).
5) Not 100% tested.

Table 5–7. TI486DLC/E DC Electrical Characteristics at Recommended Operating Conditions (Typical values are at nominal V_{CC} (5 V or 3.3 V) and T_A = 25°C)

PARAMETER		TEST CONDITIONS	TI486DLC/E			TI486DLC/E-V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	Low-level output voltage	I_{OL} = 3 mA						0.35	V
V_{OL}	Low-level output voltage	I_{OL} = 5 mA			0.45				V
V_{OH}	High-level output voltage	I_{OH} = –1 mA	2.4			V_{CC}–0.4			V
V_{OH}	High-level output voltage	I_{OH} = –0.2 mA	V_{CC}–0.5			V_{CC}–0.4			V
I_I	Input current (leakage)	0 < V_{IN} < V_{CC}, See Note 1			±15			±15	µA
I_{IH}	High-level input current at PEREQ	V_{IN} = 2.4, See Note 2			200			200	µA
I_{IL}	Low-level input current	V_{IL} = 0.45 V, See Note 3			–400			–400	µA
I_{CC}	Supply current (Active mode)	25 MHz (CLK2 = 50 MHz)		—	—		240	305	mA
I_{CC}	Supply current (Active mode)	33 MHz (CLK2 = 66 MHz)		520	650		300	375	mA
I_{CC}	Supply current (Active mode)	40 MHz (CLK2 = 80 MHz)		560	700		—	—	mA
I_{CCSM}	Supply current (Suspend mode)	25 MHz (CLK2 = 50 MHz)		—	—		6	10	mA
I_{CCSM}	Supply current (Suspend mode)	33 MHz (CLK2 = 66 MHz)		7.5	15		7	12	mA
I_{CCSM}	Supply current (Suspend mode)	40 MHz (CLK2 = 80 MHz)		10	20		—	—	mA
I_{CCSS}	Standby supply current	0 MHz, Suspended/ CLK2 stopped, See Note 3		0.4	2		0.3	2	mA
C_{IN}	Input capacitance	f_c = 1 MHz, See Note 5			10			10	pF
C_{OUT}	Output or I/O capacitance	f_c = 1 MHz, See Note 5			12			12	pF
C_{CLK}	Input capacitance CLK2	f_c = 1 MHz, See Note 5			20			20	pF

Notes:
1) Applicable for all input pins except those listed in Note 3.
2) PEREQ input has an internal pulldown resistor.
3) Applicable for $\overline{A20M}$, $\overline{BUSY}$, $\overline{ERROR}$, $\overline{FLUSH}$, $\overline{KEN}$, $\overline{SMI}$, and $\overline{SUSP}$ inputs that have an internal pullup resistor.
4) All inputs at 0.4 or V_{CC}–0.4 (CMOS levels). All inputs held static, (except CLK2 as indicated). All outputs unloaded (static I_{OUT} = 0 mA).
5) Not 100% tested.

5.5 AC Characteristics

5.5.1 Measurement Points for Switching Characteristics

The rising clock edge reference level V_{REFC}, and other reference levels are specified in Table 5–8 for the TI486SLC/E, TI486SLC/E-V, TI486DLC/E, and TI486DLC/E-V. Input or output signals must cross these levels during testing. Table 5–9, Table 5–10, Table 5–11, and , Table 5–12 list the ac characteristics including output delays, input setup requirements, input hold requirements, and output float delays. These measurements are based on the measurement points identified in Figure 5–2, Figure 5–3, and Figure 5–4.

Figure 5–2 and Figure 5–3 show delays (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

The TI486SLC/E and TI486SLC/E-V outputs A23–A1, $\overline{ADS}$, $\overline{BHE}$, $\overline{BLE}$, D/$\overline{C}$, HLDA, $\overline{LOCK}$, M/$\overline{IO}$, $\overline{SMADS}$, $\overline{SMI}$, and W/$\overline{R}$ change only at the beginning of phase one (Figure 5–2, ϕ1). Outputs D15–D0 (write cycles) and $\overline{SUSPA}$ change at the beginning of phase two, ϕ2.

The TI486SLC/E and TI486SLC/E-V inputs $\overline{BUSY}$, D15–D0 (read cycles), $\overline{ERROR}$, $\overline{FLT}$, HOLD, PEREQ, and $\overline{READY}$ are sampled at the beginning of phase one (Figure 5–2, ϕ1). Inputs $\overline{A20M}$, $\overline{FLUSH}$, INTR, $\overline{KEN}$, $\overline{NA}$, NMI, $\overline{SMI}$ and $\overline{SUSP}$ are sampled at the beginning of phase two, ϕ2.

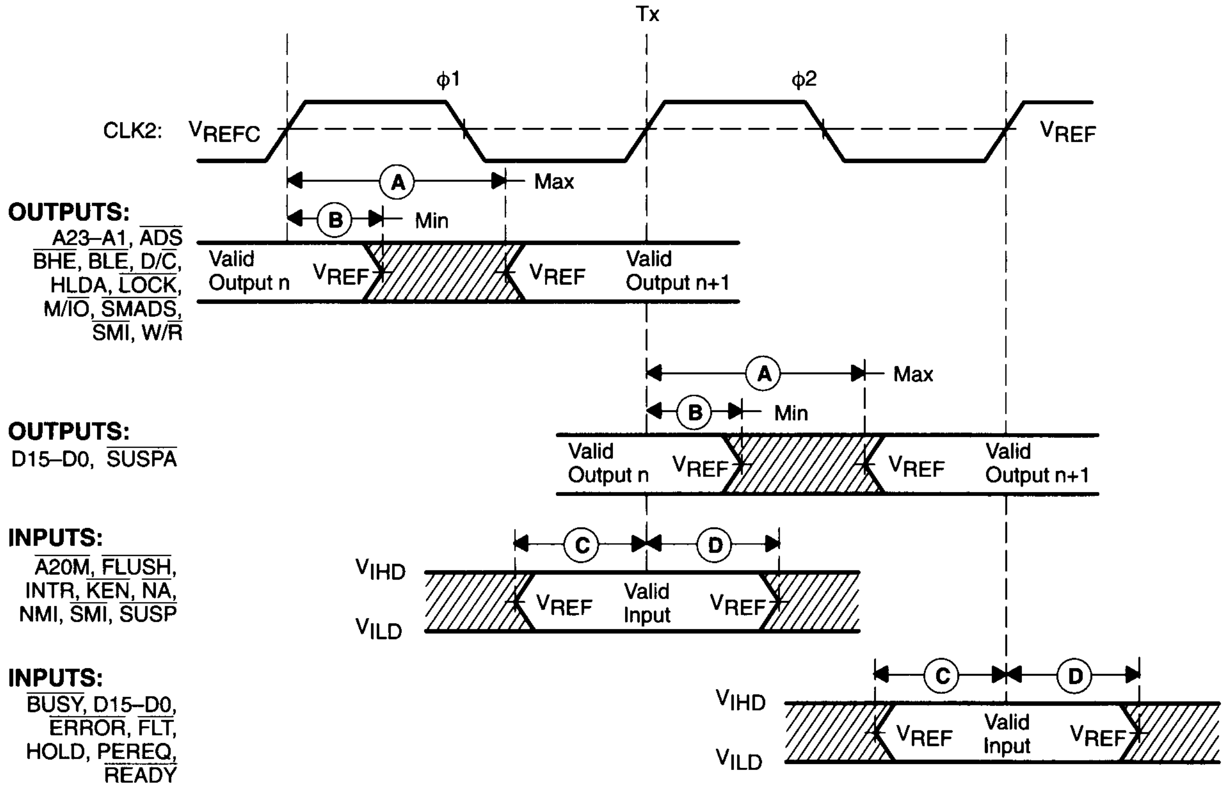
The TI486DLC/E and TI486DLC/E-V outputs A31–A2, $\overline{ADS}$, $\overline{BE3}$ – $\overline{BE0}$, D/$\overline{C}$, HLDA, $\overline{LOCK}$, M/$\overline{IO}$, $\overline{SMADS}$, $\overline{SMI}$, and W/$\overline{R}$ change only at the beginning of phase one (Figure 5–3, ϕ1). Outputs D31–D0 (write cycles) and $\overline{SUSPA}$ change at the beginning of phase two, ϕ2.

The TI486DLC/E and TI486DLC/E-V inputs $\overline{BUSY}$, D31–D0 (read cycles), $\overline{ERROR}$, HOLD, PEREQ, and $\overline{READY}$ are sampled at the beginning of phase one (Figure 5–3, ϕ1). Inputs $\overline{A20M}$, $\overline{BS16}$, $\overline{FLUSH}$, INTR, $\overline{KEN}$, $\overline{NA}$, NMI, $\overline{SMI}$ and $\overline{SUSP}$ are sampled at the beginning of phase two, ϕ2.

Table 5–8. Measurement Points for Switching Characteristics

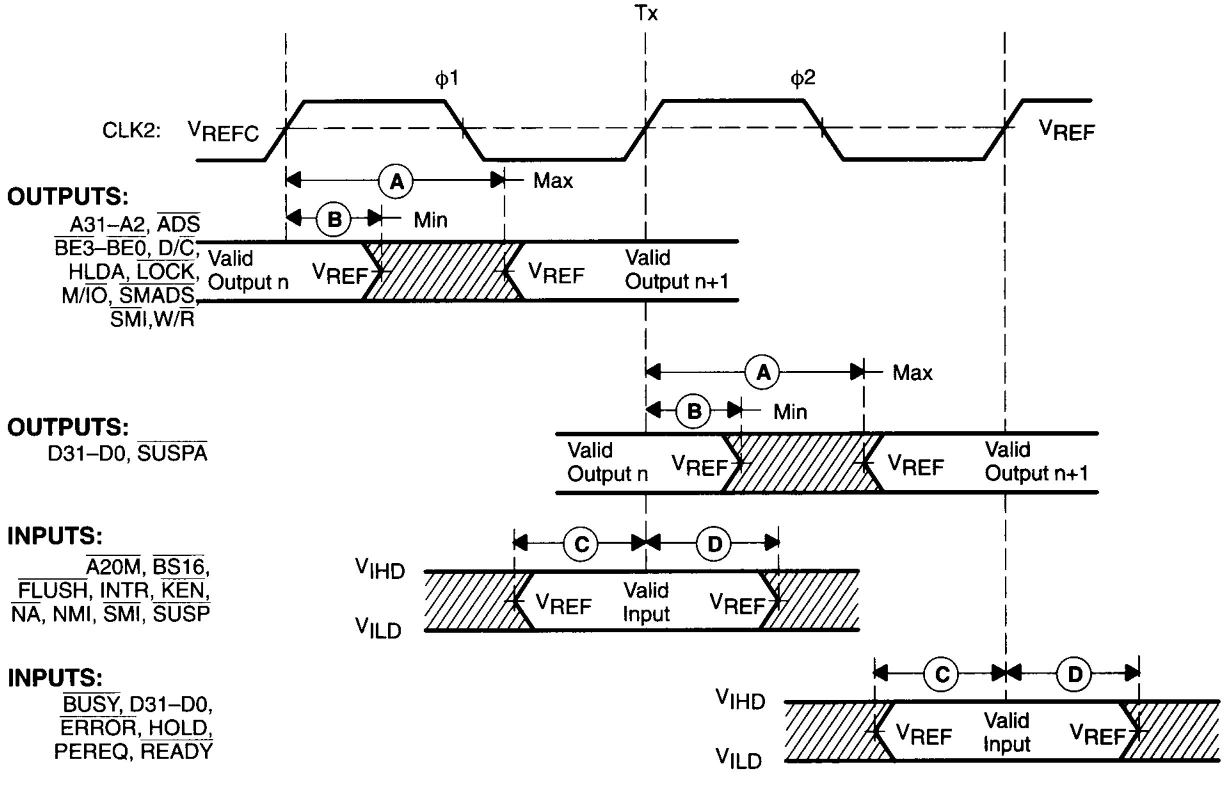
SYMBOL	TI486SLC/E	TI486SLC/E-V	TI486DLC/E	TI486DLC/E-V	UNIT
V_{REFC}	2	1.5	2	1.5	V
V_{REF}	1.5	1.2	1.5	1.2	V
V_{IHC}	V_{CC}–0.8	V_{CC}–0.5	V_{CC}–0.8	V_{CC}–0.5	V
V_{ILC}	0.8	0.6	0.8	0.6	V
V_{IHD}	3	2.3	3	2.3	V
V_{ILD}	0	0	0	0	V

Figure 5–2. TI486SLC/E and TI486SLC/E-V Drive Level and Measurement Points for Switching Characteristics



LEGEND: A – Maximum Output Delay Specification
B – Maximum Output Delay Specification
C – Minimum Input Setup Specification
D – Minimum Input Hold Specificaton

Figure 5–3. TI486DLC/E Drive Level and Measurement Points for Switching Characteristics



LEGEND: A – Maximum Output Delay Specification
B – Maximum Output Delay Specification
C – Minimum Input Setup Specification
D – Minimum Input Hold Specificaton

5.5.2 CLK2 Timing Measurement Points

The CLK2 timing measurement points are illustrated in Figure 5–4 for the TI486SLC/E, TI486SLC/E-V, TI486DLC/E, and TI486DLC/E-V.

Figure 5–4. CLK2 Timing Measurement Points

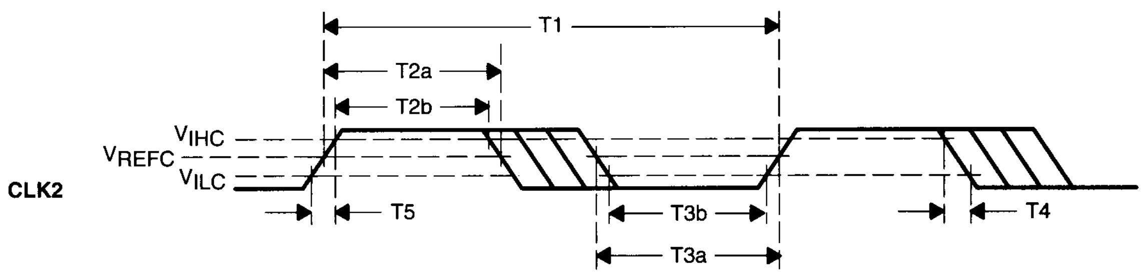


Table 5–9. AC Characteristics for TI486SLC/E-25 and TI486SLC/E-33, V_{CC} = 4.75 V to 5.25 V, T_C = 0°C to 100°C

SYMBOL	PARAMETER	TI486SLC/E-25		TI486SLC/E-33		FIGURE	NOTES
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)		
T1	CLK2 period	20		15		5-4	Note 1
T2a	CLK2 high time	7		6.25		5-4	Note 2
T2b	CLK2 high time	4		4.5		5-4	Note 2
T3a	CLK2 low time	7		6.25		5-4	Note 2
T3b	CLK2 low time	5		4.5		5-4	Note 2
T4	CLK2 fall time		7		4	5-4	Note 2
T5	CLK2 rise time		7		4	5-4	Note 2
T6	A23–A1 valid delay	4	21	4	15	5-7, 5-10	C_L = 50 pF
T6a	$\overline{SMI}$ valid delay	4	21	4	15	5-7, 5-10	C_L = 50 pF
T7	A23–A1 float delay	4	30	4	20	5-10	Note 3
T8	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ valid delay	4	21	4	15	5-7, 5-10	C_L = 50 pF
T9	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ float delay	4	30	4	20	5-10	Note 3
T10	$\overline{ADS}$, D/$\overline{C}$, M/$\overline{IO}$, W/$\overline{R}$ valid delay	4	21	4	15	5-7, 5-10	C_L = 50 pF
T10a	$\overline{SMADS}$ valid delay	4	21	4	15	5-7, 5-10	C_L = 50 pF
T11	$\overline{ADS}$, D/$\overline{C}$, M/$\overline{IO}$, W/$\overline{R}$ float delay	4	30	4	20	5-10	Note 3
T11a	$\overline{SMADS}$ float delay	4	30	4	20	5-10	Note 3
T12	D15–D0 write data, $\overline{SUSPA}$ valid delay	7	27	7	24	5-7, 5-8 5-10	C_L = 50 pF, Note 5
T12a	D15–D0 write data hold time	2		2		5-9	
T13	D15–D0 write data, $\overline{SUSPA}$ float delay	4	22	4	17	5-10	Note 3, Note 6
T14	HDLA valid delay	4	22	4	20	5-10	C_L = 50 pF
T15	$\overline{NA}$, $\overline{SUSP}$, $\overline{FLUSH}$, $\overline{KEN}$, $\overline{A20M}$ setup time	5		5		5-6	
T16	$\overline{NA}$, $\overline{SUSP}$, $\overline{FLUSH}$, $\overline{KEN}$, $\overline{A20M}$ hold time	3		3		5-6	
T19	$\overline{READY}$ setup time	9		7		5-6	
T20	$\overline{READY}$ hold time	4		4		5-6	
T21	D15–D0 read data setup time	7		5		5-6	
T22	D15–D0 read data hold time	5		3		5-6	
T23	HOLD setup time	9		11		5-6	
T24	HOLD hold time	3		2		5-6	
T25	RESET setup time	8		5		5-5	
T26	RESET hold time	3		2		5-5	
T27	NMI, INTR setup time	6		5		5-6	Note 4
T27a	$\overline{SMI}$ setup time	6		5		5-6	Note 4
T28	NMI, INTR hold time	6		5		5-6	Note 4
T28a	$\overline{SMI}$ hold time	6		5		5-6	Note 4
T29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ setup time	6		5		5-6	Note 4
T30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ hold time	5		4		5-6	Note 4

Notes:
1) Input clock can be stopped, therefore minimum CLK2 frequency is 0 MHz.
2) These parameters are not tested. They are guaranteed by design characterization.
3) Float condition occurs when maximum output current becomes less than I_I in magnitude. Float is not 100% tested.
4) These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
5) T12 minimum time is not 100% tested.
6) $\overline{SUSPA}$ floats only in response to activation of $\overline{FLT}$. $\overline{SUSPA}$ does not float during a hold acknowledge state.

Table 5–10. AC Characteristics for TI486SLC/E-V25, V_{CC} = 3 V to 3.6 V, T_C = 0°C to 85°C

SYMBOL	PARAMETER	TI486SLC/E-V25		FIGURE	NOTES
		MIN (ns)	MAX (ns)		
T1	CLK2 period	20		5-4	Note 1
T2a	CLK2 high time	7		5-4	Note 2
T2b	CLK2 high time	4		5-4	Note 2
T3a	CLK2 low time	7		5-4	Note 2
T3b	CLK2 low time	5		5-4	Note 2
T4	CLK2 fall time		7	5-4	Note 2
T5	CLK2 rise time		7	5-4	Note 2
T6	A23–A1 valid delay	3	21	5-7, 5-10	C_L = 50 pF
T6a	SMI valid delay	3	21	5-7, 5-10	C_L = 50 pF
T7	A23–A1 float delay	4	30	5-10	Note 3
T8	BHE, BLE, LOCK valid delay	2.5	18	5-7, 5-10	C_L = 50 pF
T9	BHE, BLE, LOCK float delay	4	30	5-10	Note 3
T10	ADS, D/C, M/IO, W/R valid delay	4	19	5-7, 5-10	C_L = 50 pF
T10a	SMADS valid delay	4	19	5-7,5-10	C_L = 50 pF
T11	ADS, D/C, M/IO, W/R float delay	4	30	5-10	Note 3
T11a	SMADS float delay	4	30	5-10	Note 3
T12	D15–D0 write data, SUSPA valid delay	3.5	27	5-7, 5-8	C_L = 50 pF, Note 5
T12a	D15–D0 write data hold time	2		5-9	
T13	D15–D0 write data, SUSPAfloat delay	4	22	5-10	Note 3, Note 6
T14	HDLA valid delay	2	22	5-10	C_L = 50 pF
T15	NA, SUSP, FLUSH, KEN, A20M setup time	5		5-6	
T16	NA, SUSP, FLUSH, KEN, A20M hold time	3.5		5-6	
T19	READY setup time	9		5-6	
T20	READY hold time	4		5-6	
T21	D15–D0 read data setup time	7		5-6	
T22	D15–D0 read data hold time	5		5-6	
T23	HOLD setup time	9		5-6	
T24	HOLD hold time	3.5		5-6	
T25	RESET setup time	8		5-5	
T26	RESET hold time	3		5-5	
T27	NMI, INTR setup time	6		5-6	Note 4
T27a	SMI setup time	6		5-6	Note 4
T28	NMI, INTR hold time	6		5-6	Note 4
T28a	SMI hold time	6		5-6	Note 4
T29	PEREQ, ERROR, BUSY setup time	6		5-6	Note 4
T30	PEREQ, ERROR, BUSY hold time	5		5-6	Note 4

Notes:
1) Input clock can be stopped, therefore minimum CLK2 frequency is 0 MHz.
2) These parameters are not tested. They are guaranteed by design characterization.
3) Float condition occurs when maximum output current becomes less than I_I in magnitude. Float is not 100% tested.
4) These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
5) T12 minimum time is not 100% tested.
6) SUSPA floats only in response to activation of FLT. SUSPA does not float during a hold acknowledge state.

Table 5–11. AC Characteristics for TI486DLC/E-33 and TI486DLC/E-40
V_{CC} = 4.75 V to 5.25 V, T_C = 0°C to 85°C

SYMBOL	PARAMETER	TI486DLC/E-33		TI486DLC/E-40		FIGURE	NOTES
		MIN(ns)	MAX(ns)	MIN (ns)	MAX (ns)		
T1	CLK2 period	15		12.5		5-4	Note 1
T2a	CLK2 high time	6.25		5		5-4	Note 2
T2b	CLK2 high time	4.5		3.25		5-4	Note 2
T3a	CLK2 low time	6.25		5		5-4	Note 2
T3b	CLK2 low time	4.5		3.25		5-4	Note 2
T4	CLK2 fall time		4		4	5-4	Note 2
T5	CLK2 rise time		4		4	5-4	Note 2
T6	A31–A2 valid delay	4	15	3	12.5	5-12, 5-15	C_L = 50 pF
T6a	SMI valid delay	4	15	3	12.5	5-12, 5-15	C_L = 50 pF
T7	A31–A2 float delay	4	20	3	17	5-15	Note 3
T8	BE3 – BE0, LOCK valid delay	4	15	3	12.5	5-15, 5-15	C_L = 50 pF
T9	BE3 – BE0, LOCK float delay	4	20	3	17	5-15	Note 3
T10	ADS, D/C, M/IO, W/R valid delay	4	15	3	12.5	5-12, 5-15	C_L = 50 pF
T10a	SMADS valid delay	4	15	3	12.5	5-12, 5-15	C_L = 50 pF
T11	ADS, D/C, M/IO, W/R float delay	4	20	3	17	5-15	Note 3
T11a	SMADS float delay	4	20	3	17	5-15	Note 3
T12	D31–D0 write data, SUSPA valid delay	7	24	5	20	5-12, 5-13	C_L = 50 pF, Note 5
T12a	D31–D0 write data hold time	2		2		5-14	
T13	D31–D0 write data, SUSPA float delay	4	17	3	14.5	5-15	Note 3
T14	HDLA valid delay	4	20	3	17	5-15	C_L = 50 pF
T15	A20M, FLUSH, KEN, NA, SUSP setup time	5		5		5-11	
T16	A20M, FLUSH, KEN, NA, SUSP hold time	2		2		5-11	
T17	BS16 setup time	5		5		5-11	
T18	BS16 hold time	2		2		5-11	
T19	READY setup time	7		5		5-11	
T20	READY hold time	4		3		5-11	
T21	D31–D0 read data setup time	5		5		5-11	
T22	D31–D0 read data hold time	3		3		5-11	
T23	HOLD setup time	7		4		5-11	
T24	HOLD hold time	2		2		5-11	
T25	RESET setup time	5		4.5		5-5	
T26	RESET hold time	2		2		5-5	
T27	NMI, INTR setup time	5		5		5-11	Note 4
T27a	SMI setup time	5		5		5-11	Note 4
T28	NMI, INTR hold time	5		5		5-11	Note 4
T28a	SMI hold time	5		5		5-11	Note 4
T29	PEREQ, ERROR, BUSY setup time	5		5		5-11	Note 4
T30	PEREQ, ERROR, BUSY hold time	4		3		5-11	Note 4

Notes:
1) Input clock can be stopped, therefore minimum CLK2 frequency is 0 MHz.
2) These parameters are not tested. They are guaranteed by design characterization.
3) Float condition occurs when maximum output current becomes less than I_I in magnitude. Float is not 100% tested.
4) These following inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
5) T12 minimum time is not 100% tested.

Table 5–12. AC Characteristics for TI486DLC/E-V25 and TI486DLC/E-V33 V_{CC} = 3 V to 3.6 V, T_C = 0°C to 85°C

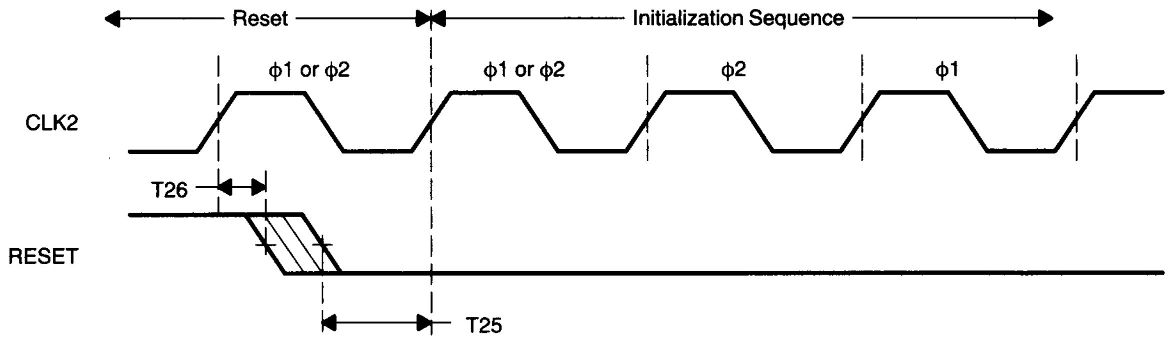
SYMBOL	PARAMETER	TI486DLC/E-V25		TI486DLC/E-V33		FIGURE	NOTES
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)		
T1	CLK2 period	20		15		5-4	Note 1
T2a	CLK2 high time	7		6.25		5-4	Note 2
T2b	CLK2 high time	4		4.5		5-4	Note 2
T3a	CLK2 low time	7		6.25		5-4	Note 2
T3b	CLK2 low time	5		4.5		5-4	Note 2
T4	CLK2 fall time		7		4	5-4	Note 2
T5	CLK2 rise time		7		4	5-4	Note 2
T6	A31–A2 valid delay	3	21	3	15	5-12, 5-15	C_L = 50 pF
T6a	$\overline{\text{SMI}}$ valid delay	3	21	3	15	5-12, 5-15	C_L = 50 pF
T7	A31–A2 float delay	4	30	4	20	5-15	Note 3
T8	$\overline{\text{BE3}}$ – $\overline{\text{BE0}}$, $\overline{\text{LOCK}}$ valid delay	2.5	18	2.5	18	5-12, 5-15	C_L = 50 pF
T9	$\overline{\text{BE3}}$ – $\overline{\text{BE0}}$, $\overline{\text{LOCK}}$ float delay	4	30	4	20	5-15	Note 3
T10	$\overline{\text{ADS}}$, D/$\overline{\text{C}}$, M/$\overline{\text{IO}}$, W/$\overline{\text{R}}$ valid delay	4	19	4	19	5-12, 5-15	C_L = 50 pF
T10a	$\overline{\text{SMADS}}$ valid delay	4	19	4	19	5-12, 5-15	C_L = 50 pF
T11	$\overline{\text{ADS}}$, D/$\overline{\text{C}}$, M/$\overline{\text{IO}}$, W/$\overline{\text{R}}$ float delay	4	30	4	20	5-15	Note 3
T11a	$\overline{\text{SMADS}}$ float delay	4	30	4	20	5-15	Note 3
T12	D31–D0 write data, $\overline{\text{SUSPA}}$ valid delay	3.5	27	3.5	24	5-12, 5-13	C_L = 50 pF, Note 5
T12a	D31–D0 write data hold time	2		2		5-14	
T13	D31–D0 write data, $\overline{\text{SUSPA}}$ float delay	4	22	4	17	5-15	Note 3
T14	HDLA valid delay	2	22	2	20	5-15	C_L = 50 pF
T15	$\overline{\text{A20M}}$, $\overline{\text{FLUSH}}$, $\overline{\text{KEN}}$, $\overline{\text{NA}}$, $\overline{\text{SUSP}}$ setup time	5		5		5-11	
T16	$\overline{\text{A20M}}$, $\overline{\text{FLUSH}}$, $\overline{\text{KEN}}$, $\overline{\text{NA}}$, $\overline{\text{SUSP}}$ hold time	3.5		3.5		5-11	
T17	$\overline{\text{BS16}}$ setup time	7		5		5-11	
T18	$\overline{\text{BS16}}$ hold time	2		2		5-11	
T19	$\overline{\text{READY}}$ setup time	9		7		5-11	
T20	$\overline{\text{READY}}$ hold time	4		4		5-11	
T21	D31–D0 read data setup time	7		7		5-11	
T22	D31–D0 read data hold time	5		4		5-11	
T23	HOLD setup time	15		12		5-11	
T24	HOLD hold time	4		4		5-11	
T25	RESET setup time	8		5		5-4	
T26	RESET hold time	3		2		5-4	
T27	$\overline{\text{NMI}}$, INTR setup time	6		5		5-10	Note 4
T27a	$\overline{\text{SMI}}$ setup time	6		5		5-10	Note 4
T28	$\overline{\text{NMI}}$, INTR hold time	6		5		5-10	Note 4
T28a	$\overline{\text{SMI}}$ hold time	6		5		5-10	Note 4
T29	PEREQ, $\overline{\text{ERROR}}$, $\overline{\text{BUSY}}$ setup time	6		5		5-10	Note 4
T30	PEREQ, $\overline{\text{ERROR}}$, $\overline{\text{BUSY}}$ hold time	5		4		5-10	Note 4

Notes:
1) Input clock can be stopped, therefore minimum CLK2 frequency is 0 MHz.
2) These parameters are not tested. They are guaranteed by design characterization.
3) Float condition occurs when maximum output current becomes less than I_l in magnitude. Float is not 100% tested.
4) These following inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
5) T12 minimum time is not 100% tested.

5.5.3 RESET Setup and Hold Timing

RESET and Hold timing for the TI486SLC/E, TI486SLC/E-V, and TI486DLC/E are illustrated in Figure 5–5.

Figure 5–5. RESET Setup and Hold Timing



5.5.4 TI486SLC/E and TI486SLC/E-V Switching Waveforms

Switching waveforms for the TI486SLC/E and TI486SLC/E-V are illustrated in Figure 5–6 through Figure 5–10.

Figure 5–6. TI486SLC/E and TI486SLC/E-V Input Signal Setup and Hold Timing

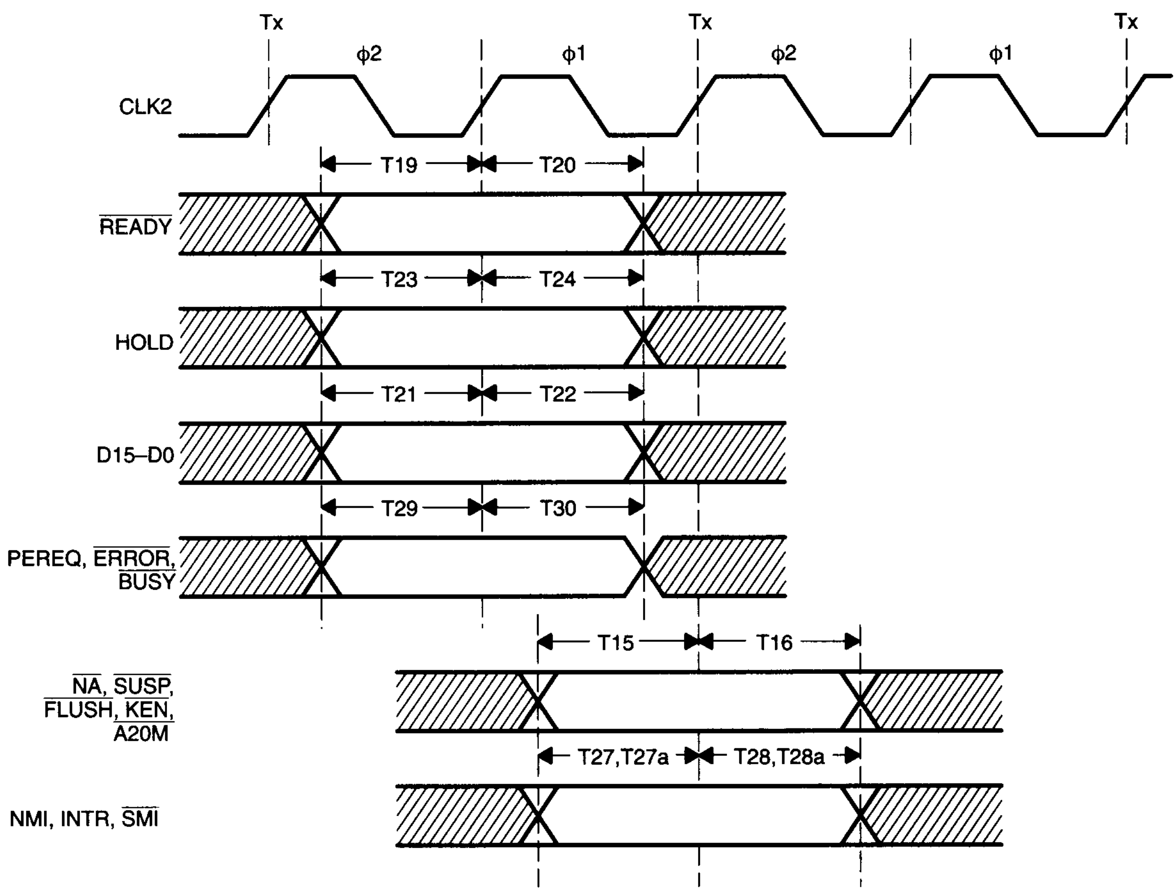


Figure 5–7. TI486SLC/E and TI486SLC/E-V Output Signal Valid Delay Timing

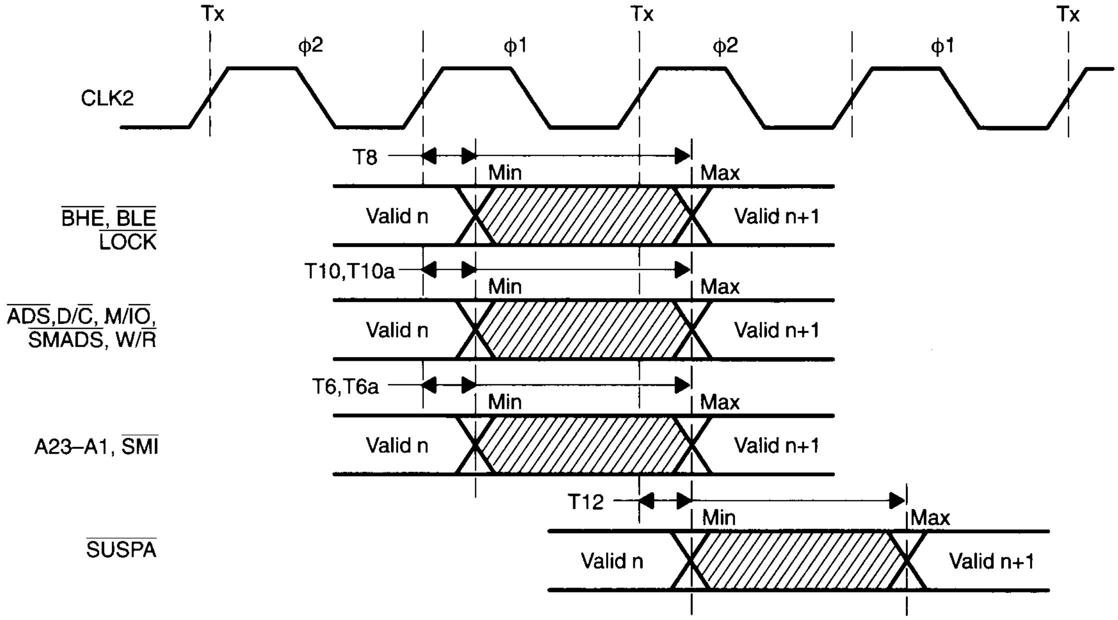


Figure 5–8. TI486SLC/E and TI486SLC/E-V Data Write Cycle Valid Delay Timing

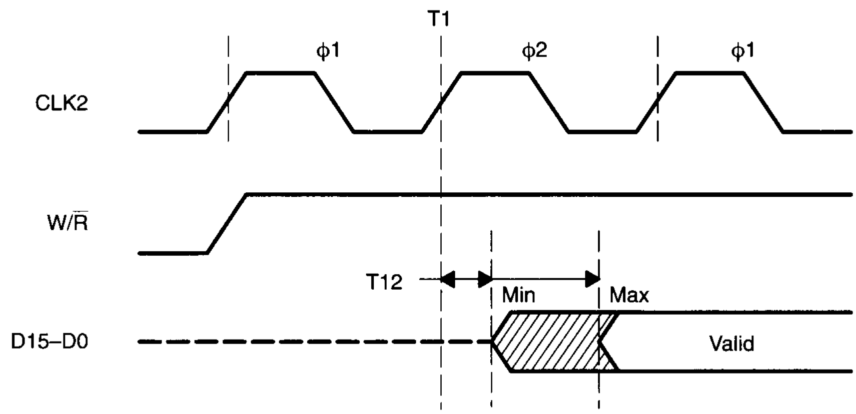


Figure 5–9. TI486SLC/E and TI486SLC/E-V Data Write Cycle Hold Timing

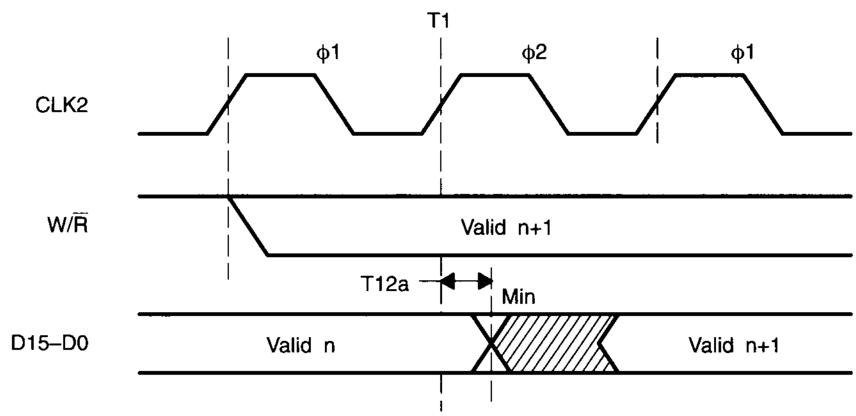
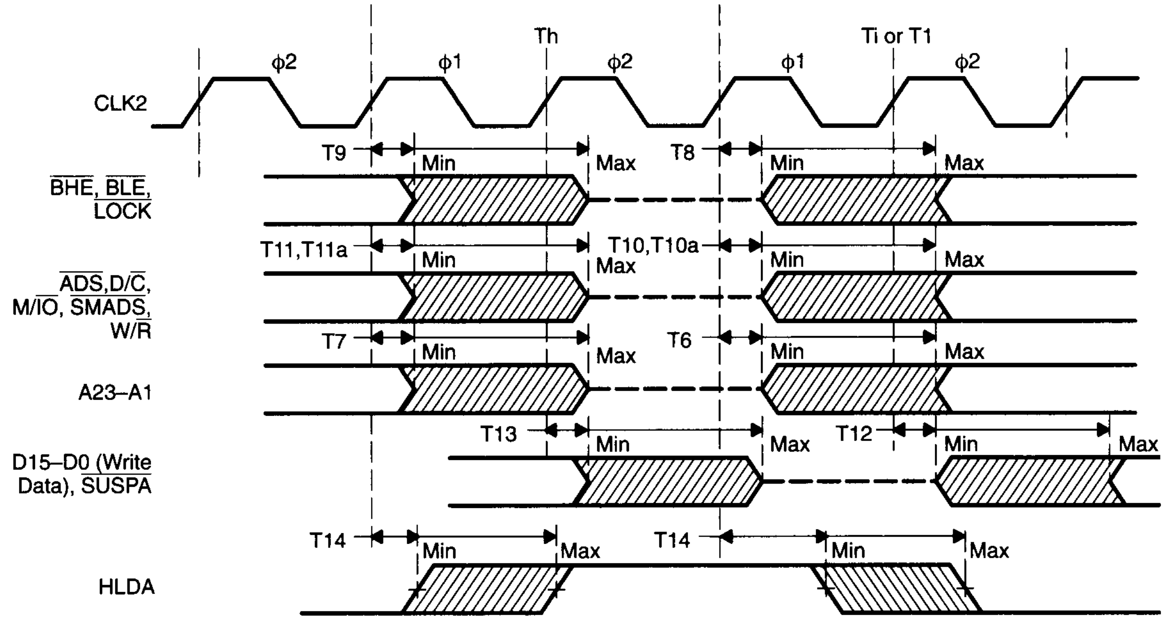


Figure 5–10. TI486SLC/E and TI486SLC/E-V Output Signal Float Delay and HLDA Valid Delay Timing



5.5.5 TI486DLC/E Switching Waveforms

Switching waveforms for the TI486DLC/E and TI486DLC/E-V are illustrated in Figure 5–11 through Figure 5–15.

Figure 5–11. TI486DLC/E and TI486DLC/E-V Input Signal Setup and Hold Timing

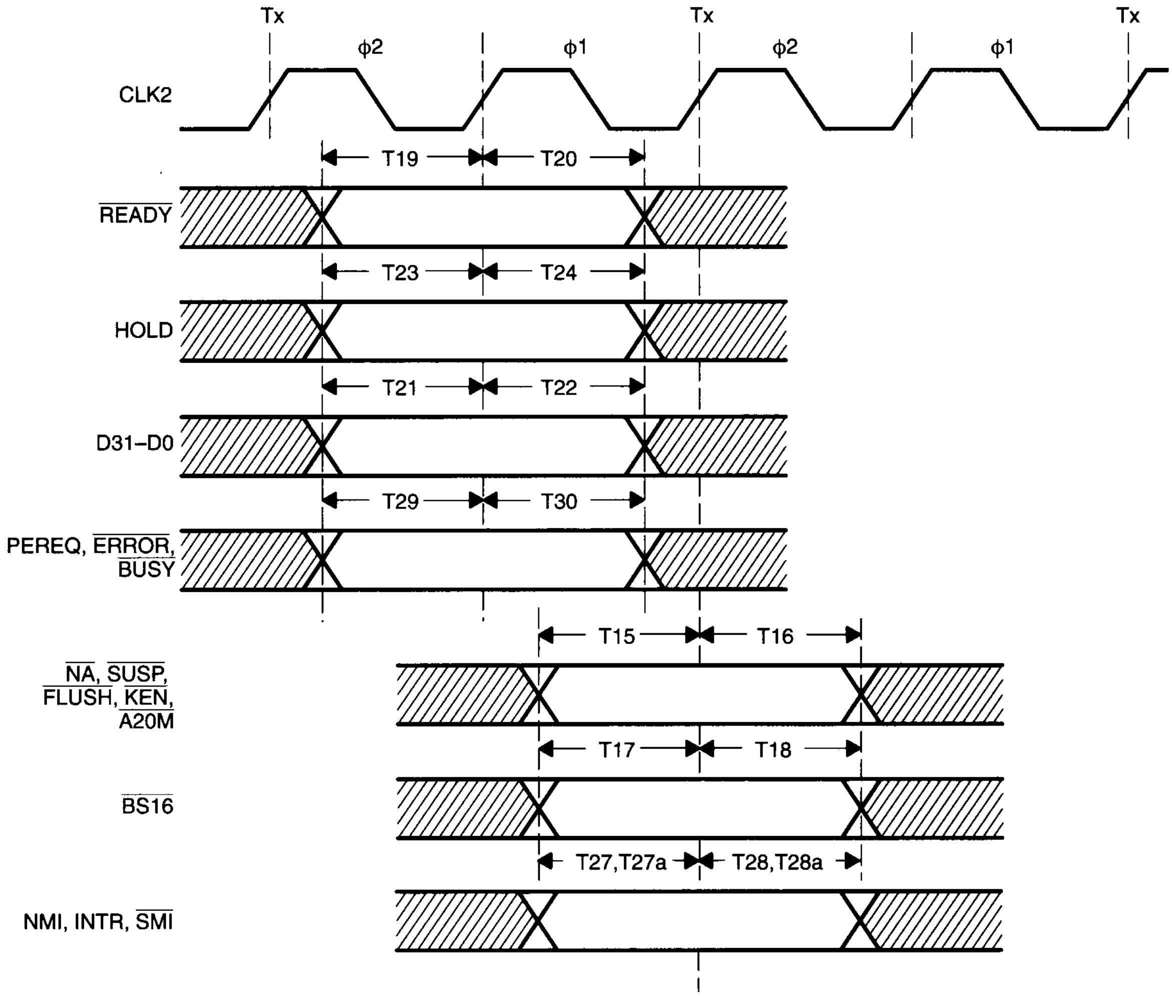


Figure 5–12. TI486DLC/E and TI486DLC/E-V Output Signal Valid Delay Timing

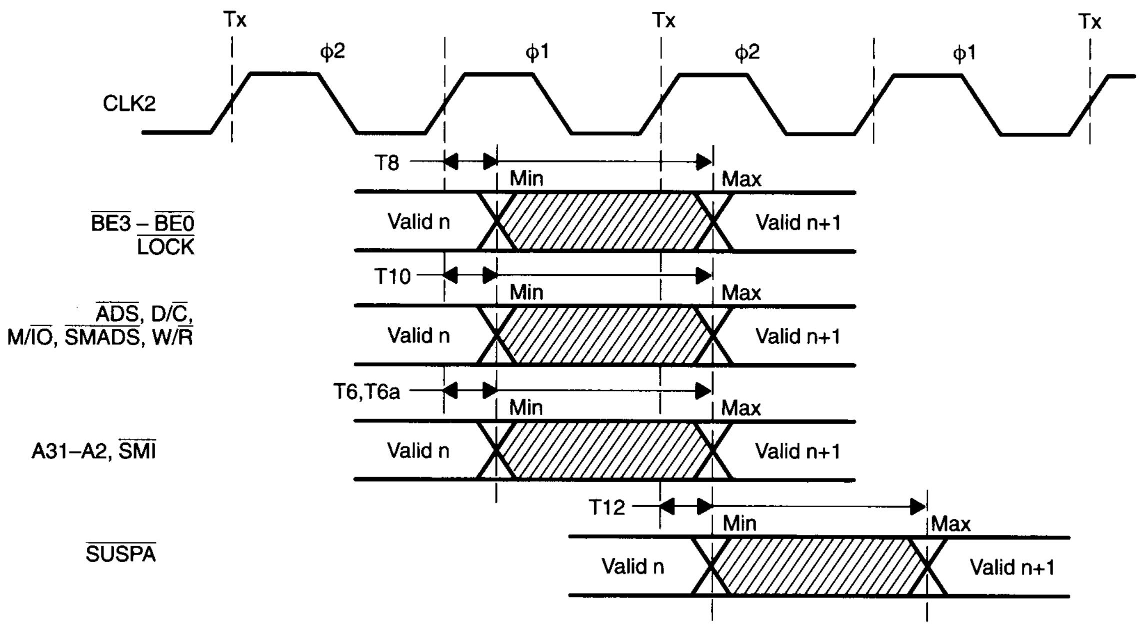


Figure 5–13. TI486DLC/E and TI486DLC/E-V Data Write Cycle Valid Delay Timing

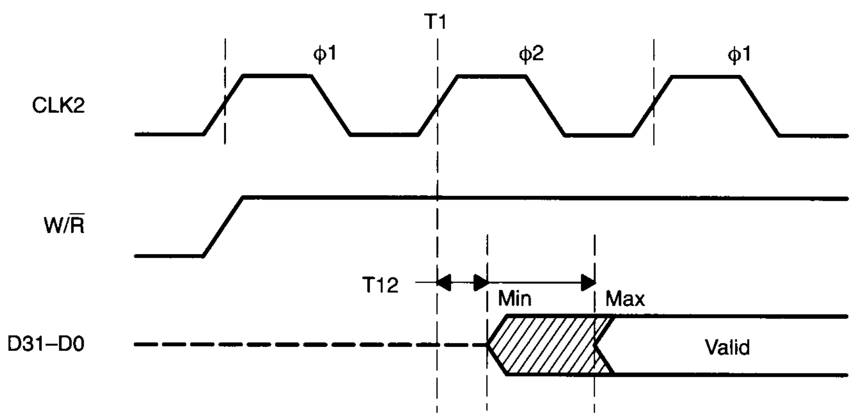


Figure 5–14. TI486DLC/E and TI486DLC/E-V Data Write Cycle Hold Timing

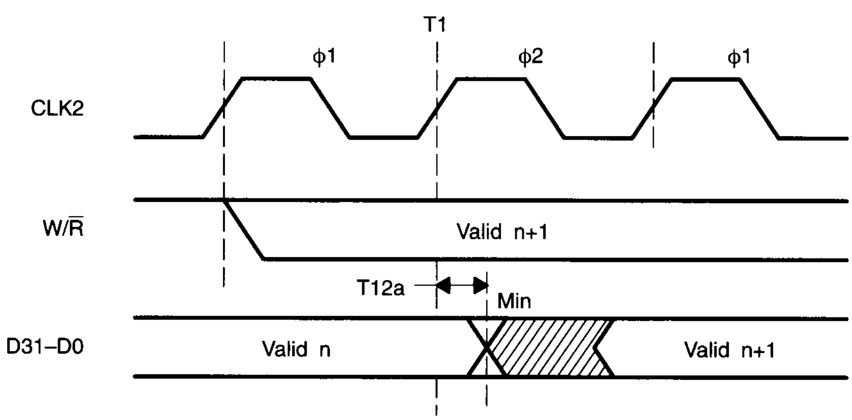


Figure 5–15. TI486DLC/E Output Signal Float Delay and HLDA Valid Delay Timing