ADVANCE INFORMATION

intel®

SERIES 2+ FLASH MEMORY CARDS
4 and 20 Megabytes

iMC004FLSP, iMC020FLSP

- **Single Power Supply Operation**
- **Automatically Reconfigures for 3.3V and 5V Systems**
- **150 ns Maximum Access Time with 10 MB/S Read Throughout**
- **High Performance Random Writes**
  - **0.85 MB/S Sustained Throughout**
  - **1 KB Burst Write @ 10 MB/S**
- **PCMCIA 2.0/JEIDA 4.1 Compatible**
- **PCMCIA Type 1 Form Factor**
- **Revolutionary Architecture**
  - **Pipelined Command Execution**
  - **Write During Erase**
  - **Series 2 Command Superset**
- **12 μA Typical Deep Powerdown**
- **State-of-the Art 0.6 μm ETOX™ IV Flash Technology**
- **1 Million Erase Cycles per Block**
- **320 Independent Lockable Blocks**

Intel's Series 2+ Flash Memory Card sets the new record for high-performance disk emulation and XIP applications in mobile PC's and dedicated equipment. Manufactured with Intel's 28F016SA 16-Mbit FlashFile™ Memory, this card takes advantage of a revolutionary architecture that provides innovative capabilities, low power operation and very high read/write performance.

The Series 2+ Card provides today's highest density, highest performance non-volatile read/write solution for solid-state storage applications. These applications are further enhanced with this product's symmetrically blocked architecture, extended MTBF, low power 3.3V operation, built-in V_{PP} generator, and multiple block-locking methods. The Series 2+ Card's dual read and write voltages allow interchange between 3.3V and 5V systems.

290491-8

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October 1993
Order Number: 290491-001

Series 2+ Flash Memory Cards

CONTENTS

SCOPE OF DOCUMENT

The documentation for Intel's Series 2+ Flash Memory Card includes this data sheet and a detailed design guide. The data sheet provides all AC and DC characteristics (including timing waveforms) and a convenient reference for the device command set and the card's integrated registers (including the 28F016SA's status registers). The design guide (order number 297373-001) provides a complete description of the methods for using the card. It also contains the full list of software algorithms and flowcharts and a section for upgrading from Intel's Series 2 Flash Memory Cards.

PRODUCT OVERVIEW

The 4 and 20 Megabyte, Series 2+ Flash Memory Cards contain a flash memory array that consists of 2 to 10 28F016SA TSOP memory devices, respectively. Each 28F016SA contains 32 distinct, individually-erasable, 64 Kbyte blocks; therefore, the cards contain 64 and 320 device blocks, respectively.

The Series 2+ Card offers additional product features to those of the Series 2 Card product family (refer to the iMC002FLSA, iMC004FLSA, iMC010FLSA, and iMC020FLSA data sheets). Some of the more notable card-level enhancements include: interchangeable operation at 3.3V or 5V and internal V_{PP} generation.

The card incorporates V_{CC} detect circuitry, referred to as SmartPower, to sense the voltage level present at the card interface. The card's control logic automatically configures its circuitry and the 28F016SA memory array accordingly. The Card Information Structure reports that the card is 3.3V or 5V compatible. The card also detects the presence of 12V on the socket V_{PP} pin and passes this supply to each 28F016SA. When 12V are unavailable, the card generates the required V_{PP} via its internal V_{PP}-generation circuitry, whether V_{CC} is 3.3V or 5V.

At the device level, internal algorithm automation allows write and block erase operations to be executed using a two-write command sequence in the same way as the 28F008SA FlashFile memory in the Series 2 Card. A superset of commands and additional performance enhancements have been added to the basic 28F008SA command-set:

- **Page buffer writes to flash** results in writes up to 4 times faster than Series 2 Cards.
- **Command queuing** permits the devices to receive new commands during the execution of the current command.
- **Automatic data writes during erase** allows the 28F016SA to perform write operations to one block of memory while performing an erase on another block.
- **Software locking of memory blocks** provides a means to selectively protect code or data within the card.
- **Erase all unlocked blocks** provides a quick and simple method to sequentially erase the blocks within a 28F016SA.

The Series 2+ Card has two means for putting its flash devices into a *Deep-Sleep* mode for reduced power consumption: 1) Issue a command to individual devices, referred to as the software-controlled *Deep-Sleep* mode. Using this approach the device will retain status register contents and finish any operation in progress: 2) Write to the card's PCMCIA-compatible Configuration and Status Register to activate a Reset-PowerDown to all devices simultaneously.

The card achieves its PCMCIA-compatible word-wide access by pairing the 28F016SA devices resulting in an accessible memory block size of 64 KWords. The card's decoding logic (contained within its ASICs) allows the system to write or read one word at a time, or one byte at a time by referencing the high or low byte. Erasure can be performed on the entire block pair (high and low device block simultaneously) or on the high or low byte portion separately. Although the 28F016SA supports byte or word-wide data access, the byte interface was utilized within the card to allow the delivery of higher performance benefits (such as the doubling of the effective page buffer size).

The Series 2+ Card's ASICs also contain the Component Management Registers that provide five control functions—Ready-Busy mode selection, software-controlled write protection, card status, voltage-control and status, and soft reset.

The memory card interface supports the Personal Computer Memory Card Industry Association (PCMCIA 2.01) and Japanese Electronics Industry Development Association (JEIDA 4.1) 68-pin card format. The Series 2+ Flash Card meets all PCMCIA/JEIDA Type 1 mechanical specifications.

SERIES 2+ ARCHITECTURE OVERVIEW

As depicted in Figure 1, the Series 2+ Card consists of three major functional elements—the 28F016SA Flash Memory array, card control logic and SmartPower circuitry. The card control logic handles the interface between the flash memory array and the host system's PCMCIA signals. The Smart Power circuitry provides the card's integrated V_{PP} generator and a means for detecting the socket's voltage levels.

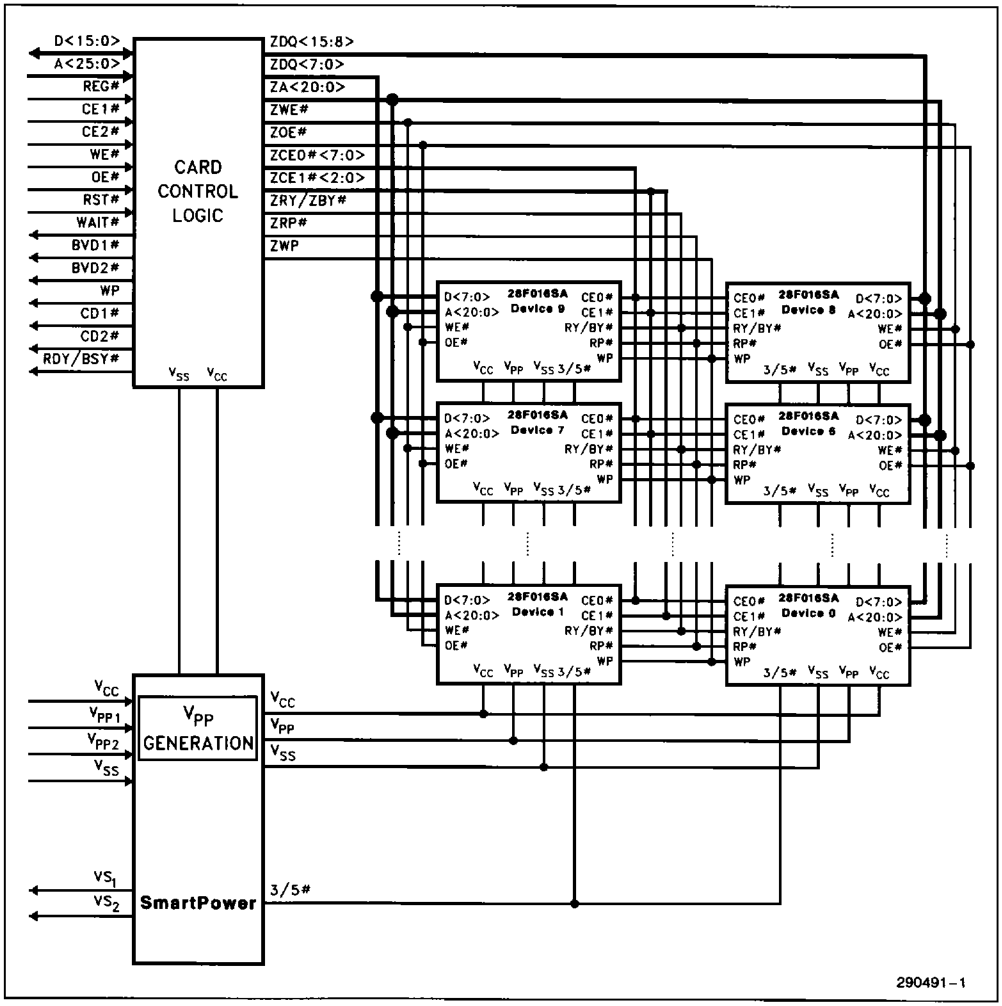


Figure 1. Series 2+ Card Block Diagram Showing Major Functional Elements Including the Card's Control Logic, Smart Power Circuitry and the 28F016SA Flash Memory Components

The Series 2+ Card signals comply with the PCMCIA specification, as shown in Table 1. Table 2 describes the functionality of these signals.

Table 1. Series 2+ Flash Memory Card Signals

Pin	Signal	I/O	Function	Active
1	GND		Ground	
2	DQ_3	I/O	Data Bit 3	
3	DQ_4	I/O	Data Bit 4	
4	DQ_5	I/O	Data Bit 5	
5	DQ_6	I/O	Data Bit 6	
6	DQ_7	I/O	Data Bit 7	
7	CE_1#	I	Card Enable 1	LOW
8	A_{10}	I	Address Bit 10	
9	OE#	I	Output Enable	LOW
10	A_{11}	I	Address Bit 11	
11	A_9	I	Address Bit 9	
12	A_8	I	Address Bit 8	
13	A_{13}	I	Address Bit 13	
14	A_{14}	I	Address Bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#		Ready-Busy	LOW
17	V_{CC}		Supply Voltage	
18	V_{PP1}		Supply Voltage	
19	A_{16}	I	Address Bit 16	
20	A_{15}	I	Address Bit 15	
21	A_{12}	I	Address Bit 12	
22	A_7	I	Address Bit 7	
23	A_6	I	Address Bit 6	
24	A_5	I	Address Bit 5	
25	A_4	I	Address Bit 4	
26	A_3	I	Address Bit 3	
27	A_2	I	Address Bit 2	
28	A_1	I	Address Bit 1	
29	A_0	I	Address Bit 0	
30	DQ_0	I/O	Data Bit 0	
31	DQ_1	I/O	Data Bit 1	
32	DQ_2	I/O	Data Bit 2	
33	WP	O	Write Protect	HIGH
34	GND		Ground	
35	GND		Ground	
36	CD_1#	O	Card Detect 1	LOW
37	DQ_{11}	I/O	Data Bit 11	
38	DQ_{12}	I/O	Data Bit 12	
39	DQ_{13}	I/O	Data Bit 13	
40	DQ_{14}	I/O	Data Bit 14	
41	DQ_{15}	I/O	Data Bit 15	
42	CE_2#	I	Card Enable 2	LOW
43	VS_1	O	Voltage Sense 1	
44	RFU		Reserved	
45	RFU		Reserved	
46	A_{17}	I	Address Bit 17	
47	A_{18}	I	Address Bit 18	
48	A_{19}	I	Address Bit 19	
49	A_{20}	I	Address Bit 20	
50	A_{21}	I	Address Bit 21	
51	V_{CC}		Supply Voltage	
52	V_{PP2}		Supply Voltage	
53	A_{22}	I	Address Bit 22	
54	A_{23}	I	Address Bit 23	
55	A_{24}	I	Address Bit 24	
56	A_{25}	I	Address Bit 25	
57	VS_2	O	Voltage Sense 2	N.C.
58	RST	I	Reset	HIGH
59	WAIT#	O	Extend Bus Cycle	LOW
60	RFU		Reserved	
61	REG#	I	Register Select	LOW
62	BVD_2	O	Batt. Volt Det 2	
63	BVD_1	O	Batt. Volt Det 1	
64	DQ_8	I/O	Data Bit 8	
65	DQ_9	I/O	Data Bit 9	
66	DQ_{10}	I/O	Data Bit 10	
67	CD_2#	O	Card Detect 2	LOW
68	GND		Ground	

Table 2. Series 2+ Flash Memory Card Signal Descriptions

Symbol	Type	Description
A_0–A_{25}	I	**ADDRESS INPUTS:** A_0 through A_{25} are address bus lines which enable direct addressing of 64 megabytes of memory on a card. A_0 is not used in word access. A_{25} is the most significant bit.
DQ_0–DQ_{15}	I/O	**DATA INPUT/OUTPUT:** DQ_0 through DQ_{15} constitute the bidirectional data bus. DQ_{15} is the most significant bit.
CE_1#, CE_2#	I	**CARD ENABLE 1, 2:** CE_1# enables even bytes, CE_2# enables odd bytes. Multiplexing A_0, CD_1# and CD_2# allows 8-bit hosts to access all data on DQ_0 through DQ_7.
OE#	I	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	I	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	O	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or write activities. A high output indicates the memory card is ready to accept accesses. A low output indicates that a device(s) in the memory card is(are) busy with internally timed activities.
CD_1#, CD_2#	O	**CARD DETECT 1, 2:** These signals provide for correct card insertion detection. They are positioned at opposite ends of the card to detect proper alignment. The signals are connected to ground internally on the memory card and will be forced low whenever a card is placed in the socket. The host socket interface circuitry shall supply 10K or larger pull-up resistors on these signal pins.
WP	O	**WRITE PROTECT:** Write Protect reflects the status of the Write-Protect switch on the memory card. WP set high = write protected, providing internal hardware write lockout to the flash array.
V_{PP1}, V_{PP2}		**WRITE/ERASE POWER SUPPLY:** (12V nominal) for erasing memory array blocks or writing data in the array. They must be 12V to perform an erase/write operation, when not using the card's integrated V_{PP} generator. These signals may be disconnected but are required for ExCA compliance.
V_{CC}		**CARD POWER SUPPLY:** (3.3V/5V nominal) for all internal circuitry.
GND	I	**GROUND** for all internal circuitry.
REG#	I	**REGISTER SELECT:** Provides access to Series 2+ Flash Memory Card registers and Card Information Structure in the Attribute Memory Plane.
RST	I	**RESET:** Active high signal from system for placing card in Power-On Default State.
WAIT#	O	**WAIT: (Extend Bus Cycle)** Used by Intel's I/O cards and is driven high.
BVD_1, BVD_2	O	**BATTERY VOLTAGE DETECT:** Upon completion of the power on reset cycle, these signals are driven high to maintain SRAM-card compatibility.
VS_1, VS_2	O	**VOLTAGE SENSE:** Notify the host socket of the card's V_{CC} requirements. VS_1 is grounded and VS_2 open indicates a 3.3V/5V card as depicted in the CIS.
RFU		**RESERVED FOR FUTURE USE.**
N.C.		**NO INTERNAL CONNECTION.** Pin may be driven or left floating.

CARD CONTROL LOGIC

The Card Control Logic, contained within two ASICs, handles the address decoding and data control for the Series 2+ Card. The card's Component Management Registers are also contained within the Card Control Logic.

ADDRESS DECODE LOGIC

At the highest level, the Address Decode section determines when to select the Common Memory (REG# = V_{IH}) or Attribute Memory (REG# = V_{IL}) Planes. Within the Attribute Memory Plane, the address decode logic determines when to select the Card Information Structure (CIS) or Component Management Registers (CMR). The CIS is contained at even-byte locations beginning at address 0000H. The CMRs are mapped at even-byte locations beginning at address 4000H as shown in Figure 2.

DATA CONTROL LOGIC

As shown in Table 3, data paths and directions are selected by the Data Control logic using REG#, A_0, WE#, OE#, CE_1#, and CE_2# as logic inputs. The Data Control logic selects any of the PCMCIA Word-Wide, Byte-Wide, and Odd-Byte modes for either Reads or Writes to Common or Attribute Memory. All accesses to the Attribute Memory Plane must be made through D_{7-0}; no valid data can be written on the high byte. Reads of D_{15-8} will yield FFH.

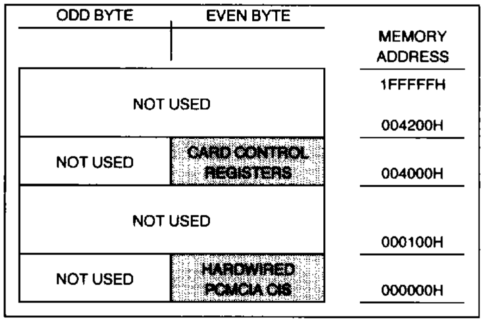


Figure 2. Attribute Memory Plane

Table 3. Data Access Mode Truth Tables

MODE	REG#	CE_2#	CE_1#	A_0	OE#	WE#	V_{PP2}	V_{PP1}	D_{15-8}	D_{7-0}
COMMON MEMORY PLANE										
STANDBY	X	V_{IH}	V_{IH}	X	X	X	V_{PPL}	V_{PPL}	HIGH-Z	HIGH-Z
BYTE-READ	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	HIGH-Z	EVEN-BYTE
	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	HIGH-Z	ODD-BYTE
WORD-READ	V_{IH}	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	ODD-BYTE	EVEN-BYTE
ODDBYTE READ	V_{IH}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	ODD-BYTE	HIGH-Z
BYTE WRITE	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	XXX	V_{PPH}	XXX	EVEN-BYTE
	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPH}	XXX	XXX	ODD-BYTE
WORD-WRITE	V_{IH}	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPH}	ODD-BYTE	EVEN-BYTE
ODDBYTE WRITE	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	V_{PPH}	V_{PPL}	ODD-BYTE	XXX
ATTRIBUTE MEMORY PLANE										
STANDBY	X	V_{IH}	V_{IH}	X	X	X	V_{PPL}	V_{PPL}	HIGH-Z	HIGH-Z
BYTE-READ	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	HIGH-Z	EVEN-BYTE
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	HIGH-Z	FFH
WORD-READ	V_{IL}	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	FFH	EVEN-BYTE
ODDBYTE READ	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{PPL}	V_{PPL}	FFH	HIGH-Z
BYTE WRITE	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{PPL}	V_{PPL}	XXX	EVEN-BYTE
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{PPL}	V_{PPL}	XXX	XXX
WORD-WRITE	V_{IL}	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	V_{PPL}	V_{PPL}	XXX	EVEN-BYTE
ODDBYTE WRITE	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	V_{PPL}	V_{PPL}	XXX	XXX

COMPONENT MANAGEMENT REGISTERS

The Component Management Registers (CMRs) are classified into two categories: those defined by PCMCIA R2.0 and those included by Intel to enhance the interface between the host system and the card's flash memory array. The CMRs provide five control functions—Ready-Busy Mode selection, Voltage Control, Software-controlled Write Protection, Card Status, and Soft Reset.

Card Register Tables

4000H—Configuration Option Register (PCMCIA)

SRESET	CONFIGURATION INDEX						
7	6	5	4	3	2	1	0

BIT 7 SOFT RESET
1 = Reset to Power On State
0 = End Reset Cycle

BITS 6–0
- Driven Low

Default: 02H

4002H—Configuration and Status Register (PCMCIA)

RESERVED*					PwrDwn	RESERVED*	
7	6	5	4	3	2	1	0

BIT 2 POWER DOWN
1 = Force All Devices Into Deep Sleep via the Device's RP# Pin. All Device Register Contents are Lost.
0 = Power Up

Default: 00H

4100H—Card Status Register (Intel—READ ONLY)

RESERVED*		SRESET	CMWP	PwrDwn	CISWP	WP	RDY/BSY#
7	6	5	4	3	2	1	0

BIT 5 SOFT RESET
- Mirrors the SRESET Bit (7) of the Configuration Option Register.
1 = RESET

BIT 4 COMMON MEMORY WP
- Indicates the Write Protect Status of the Common Memory Plane, Minus the CMCIS.

BIT 3 POWER DOWN
- Reflects the PwrDwn Bit (2) of the Configuration and Status Register.
1 = POWER DOWN

BIT 2 COMMON MEMORY CIS WP
- Indicates the Write Protect Status of the Common Memory CIS.
1 = WRITE PROTECTED

BIT 1 WRITE PROTECT SWITCH
- Reports the Status of the Card's Mechanical Write Protect Switch.
1 = WRITE PROTECT SWITCH ON

BIT 0 READY/BUSY#
- Mirrors the Card's RDY/BSY# Pin
1 = READY

Default: 1H or 3H

4104H—Write Protection Register (Intel)

RESERVED*					BLKEN	CMWP	CISWP
7	6	5	4	3	2	1	0

BIT 2 BLOCK LOCKING ENABLE
1 = Enable Independent 28F016SA Block Locking.
0 = All Blocks Unlocked.

BIT 1 COMMON MEMORY WP
1 = Force Common Memory, Minus the CMCIS, to Write Protected Status.
0 = WriteProtect According to Independent 27F016S Block Locking.

BIT 0 COMMON MEMORY CIS WP
1 = Force Only the Common Memory CIS Into Write Protected Status.
0 = Write Protected According to Independent 28F016SA Block Locking.

Default: 04H

410CH—Voltage Control Register (Intel)

V_{CC} LVL	RESERVED*					V_{PP} VAL	V_{PP} GEN
7	6	5	4	3	2	1	0

BIT 7 V_{CC} LEVEL
1 = Host Supplying 3.3V.
0 = Host Supplying 5V.

BIT 1 V_{PP} VALID
1 = V_{PP} Between 11.4V and 12.6V
0 = V_{PP} Invalid.

BIT 0 V_{PP} GENERATION
1 = Turn on Integrated V_{PP} Generator
0 = Turn off Integrated V_{PP} Generator

Default: 82H or 02H

4140H—Ready/Busy Mode Register (Intel)

RESERVED*						RACK	MODE
7	6	5	4	3	2	1	0

BIT 1 READY ACKNOWLEDGE
- Clear to Set up RDY/BSY# Pin, Then Clear After Each Becomes Ready to Acknowledge Transition.

BIT 0 RDY/BSY# MODE
1 = High Performance Mode
0 = PCMCIA Level Mode

Default: 00H

NOTE:
*Reserved bits should be zero (low) to insure future compatability.

SMART POWER

The Smart Power circuitry generates and monitors the card's programming voltage. When a host system does not provide a V_{PP} supply, the card's integrated generator can be switched on via the card's Voltage Control Register. The Smart Power circuitry also detects the host system's V_{CC} level (3.3V or 5V) and configures the card's flash memory devices accordingly (using the 28F016SA 3/5# pin as shown in Figure 1).

DEVICE COMMAND SET

The 28F016SA-based Series 2+ Command Set increases functionality over earlier 28F008-based designs while maintaining backwards compatibility. The extended 28F016SA command set supports many new features to improve programmability and write performance such as: page buffered writing, individual block-locking, multiple RDY/BSY# configurations and device level queuing capabilities. The following pages list the Series 2+ command set and Bus Cycle Operations overview.

Series 2+ Command Set

Code (H)	Series 2-Compatible Mode
00	Invalid/Reserved
10	Byte Write
20	Single Block Erase
40	Byte Write
50	Clear Status Register
70	Read Compatible Status Register
90	Intelligent Identifier
B0	Erase Suspend
D0	Erase Confirm/Resume
FF	Read Array

Code (H)	Series 2+ Performance Enhancement
08	Page Buffer Write to Flash
71	Read Extended Status Registers
72	Page Buffer Swap
74	Single Load to Page Buffer
75	Read Page Buffer
77	Lock Block
80	Abort
96	RY/BY# Reconfiguration
97	Lock-Status Upload
A7	Erase All Unlocked Blocks
E0	Sequential Load to Page Buffer
F0	Sleep

Command Bus Cycle Definitions (28F008SA-Compatible Mode)

Command	First Bus Cycle				Second Bus Cycle				Notes
	R/W	Adrs.	Data		R/W	Adrs.	Data		
			x8	x16			x8	x16	
Read Array	W	DA	FFH	FFFFH	R	DA	AD	AD	
Intelligent Identifier	W	DA	90H	9090H	R	IA	ID	ID	
Read CSR	W	DA	70H	7070H	R	DA	CSRD	CSRD	1
Clear Status Register	W	DA	50H	5050H					2
Word/Byte Write§	W	WA	40H	4040H	W	WA	WD	WD	
Word/Byte Write (Alternate)§	W	WA	10H	1010H	W	WA	WD	WD	
Block Erase/Confirm§	W	BA	20H	2020H	W	BA	D0H	D0D0h	
Erase Suspend/Resume	W	DA	B0H	B0B0H	W	DA	D0H	D0D0h	

ADDRESSES:
DA = Device Address
BA = Block Address
IA = Identifier Address
WA = Write Address

DATA:
AD = Array Data
CSRD = CSR Data
ID = Identifier Data
WD = Write Data

§ = Queueable Commands

NOTES:
1. The CSR is automatically available after the device enters Data Write, Erase or Suspend operations.
2. This command clears CSR.3, CSR.4 and CSR.5. Also clears GSR.5 and BSR.5 and BSR.2 bits.

Command Bus Cycle Definitions (28F016SA Superset Mode)

Command	First Bus Cycle				Second Bus Cycle				Third Bus Cycle				Notes
	R/W	Adrs.	Data		R/W	Adrs.	Data		R/W	Adrs.	Data		
			x8	x16			x8	x16			x8	x16	
PAGE BUFFER CONTROL													
Read Page Buffer	W	DA	75H	7575H	R	PA	PD	PDPD					
Page Buffer Swap	W	DA	72H	7272H									1
Single Load to Page Buffer	W	DA	74H	7474H	R	PA	PD	PDPD					
Sequential Load to Page Buffer	W	DA	E0H	E0E0H	W	DA	BCL		W	DA	BCH		2, 3
Page Buffer Write to Flash Array§	W	DA	0CH	0C0CH	W	A0	BC(L,H)		W	WA	BC(H,L)		2, 3, 4
READY/BUSY CONFIGURATION													
RY/BY# Pulse-On-Erase§	W	DA	96H	9696H	W	DA	03H	0303H					5
RY/BY# Pulse-On-Write§	W	DA	96H	9696H	W	DA	02H	0202H					5
RY/BY# Enable§	W	DA	96H	9696H	W	DA	01H	0101H					5
RY/BY# Disable§	W	DA	96H	9696H	W	DA	04H	0404H					5
WRITE PROTECTION AND DEVICE STATUS													
Lock Block/Confirm§	W	DA	77H	7777H	W	BA	D0H	D0D0H					
Upload Status Bits/Confirm§	W	DA	97H	9797H	W	DA	D0H	D0D0H					6
ADDITIONAL FUNCTIONS													
Read Extended Registers	W	DA	71H	7171H	R	RA	GSRD/BSRD						7
Erase All Unlocked Blocks/Confirm§	W	DA	A7H	A7A7H	W	DA	D0H	D0D0H					
Sleep	W	DA	F0H	F0F0H									
Abort	W	DA	80H	8080H									

ADDRESSES:
DA = Device Address
BA = Block Address
IA = Identifier Address
PA = Page Buffer Address
RA = Extended Register Address
WA = Write Address
X = Don't Care

DATA:
AD = Array Data
CSRD = CSR Data
G/BSRD = GSR/BSR Data
ID = Identifier Data
WD = Write Data
PD = Page Buffer Data

DATA COUNTS:
WC(L,H) = Word Count (Low, High)
BC(L,H) = Byte Count (Low, High)
WD(L,H) = Write Data (Low, High)

§ = Queueable Commands

NOTES:
1. This command allows the user to swap between available page buffers (0 or 1).
2. BCH/WCH must be at 00H for this product because of the 256-byte Page Buffer size AND to avoid writing the Page Buffer contents into more than one 256-byte segment within an array block. They are simply shown for Page Buffer expandability.
3. Page Address and Page Data (whose count is given in cycles 2 and 3) are supplied starting in the 4th cycle (not shown).
4. A0 is automatically complemented to load the second byte of data.
5. These commands reconfigure RY/BY# output to one of two pulse modes, or they enable and disable the RY/BY# function.
6. Upon device power-up, all BSR lock bits are locked. The Lock Status Upload command must be written to reflect the actual lock bit status.
7. RA can be the GSR address or any BSR address.

DEVICE STATUS REGISTERS

Each 28F016SA has three types of status registers: the Compatible Status Register, the Global Status Register and the Block Status Register. The Compatible Status register is identical to the 28F008SA Status Register. The Global Status Register provides queue and page buffer information about each device. Each block within the device has a Block Status Register assigned to it. The BSR contains the Block-Locking Status and other information specific to the block being addressed.

Compatible Status Register (CSR)

WSMS	ESS	ES	DWS	VPPS	RSRVD	RSRVD	RSRVD
7	6	5	4	3	2	1	0

CSR.7 WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

CSR.6 ERASE SUSPEND STATUS
1 = Erase Suspended
0 = Erase in Progress/ Completed

CSR.5 ERASE STATUS
1 = Error in Block Erasure
0 = Successful Block Erasure

CSR.4 DATA-WRITE STATUS
1 = Error in Data Write
0 = Data Write Successful

CSR.3 V_{PP} STATUS
1 = V_{PP} Low Detected, Operation Aborted
0 = V_{PP} OK

CSR.2-0
Reserved

Default: 80H

Global Status Register (GSR)

WSMS	OSS	DOS	DSS	QS	PBAS	PBS	PBSS
7	6	5	4	3	2	1	0

GSR.7 WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

GSR.6 OPERATION SUSPEND STATUS
1 = Operation Suspended
0 = Operation in Progress/ Completed

GSR.5 DEVICE OPERATION STATUS
1 = Operation Unsuccessful
0 = Operation Successful or Running

GSR.4 DEVICE SLEEP/ Status
1 = Device in Sleep
0 = Device Not in Sleep

GSR.3 QUEUE STATUS
1 = Queue Full
0 = Queue Available

GSR.2 PAGE BUFFER AVAILABLE STATUS
1 = One or Two Buffers Available
0 = No Page Buffer Available

GSR.1 PAGE BUFFER STATUS
1 = Selected Page Buffer Ready
0 = Selected Page Buffer Busy

GSR.0 PAGE BUFFER SELECT STATUS
1 = Page Buffer 1 Selected
0 = Page Buffer 0 Selected

Default: 8EH

Block Status Register (BSR)

BS	BLS	BOS	BOAS	QS	VPPS	R	R
7	6	5	4	3	2	1	0

BSR.7 BLOCK STATUS
1 = Ready
0 = Busy

BSR.6 BLOCK-LOCK STATUS
1 = Block Unlocked
0 = Block Locked

BSR.5 BLOCK OPERATION STATUS
1 = Operation Unsuccessful
0 = Operation Successful or Running

BSR.4 BLOCK OPERATION ABORT STATUS
1 = Operation Aborted
0 = Operation Not Aborted

BSR.3 QUEUE STATUS
1 = Queue Full
0 = Queue Available

BSR.2 V_{PP} STATUS
1 = V_{PP} Low Detect
0 = V_{PP} OK

BSR.1–0 RESERVED

Default: C0H

PCMCIA CARD INFORMATION STRUCTURE

The Card Information Structure begins at address 0000000H of the card's Attribute Memory Plane. It contains a variable-length chain of data blocks (tuples) that conform to a basic format (Table 4). The CIS of the Series 2+ Flash Memory Card is found in Table 5.

Table 4. PCMCIA Tuple Format

BYTES	DATA
0	**TUPLE CODE:** CISTPL_xxx. The tuple code 0FFh indicates no more tuples in the list.
1	**TUPLE LINK:** TPL_LINK. Link to the next tuple in the list. This can be viewed as the number of additional bytes in tuple, excluding this byte. If the link field is zero, the tuple body is empty. If the link field contains 0FFh, this tuple is the last tuple in the list.
2–n	Bytes specific to this tuple.

Table 5. Series 2+ Tuples

Address	Value	Description
00H	01H	**CISTPL DEVICE**
02H	04H	TPL_LINK
04H	57H	FLASH
06H	2AH 32H	200 ns 250 ns
08H	0EH 4EH	CARD SIZE 4 MB 20 MB
0AH	FFH	END OF DEVICE
0CH	1CH	**CISTPL_DEVICE_OC**
0EH	05H	TPL_LINK
10H	02H	OTHER CONDITIONS—3 V_{CC}
12H	57H	FLASH
14H	32H	250 ns
16H	0EH 4EH	CARD SIZE 4 MB 20 MB
18H	FFH	END OF DEVICE
1AH	17H	**CISTPL_DEVICE_A**
1CH	04H	TPL_LINK
1EH	1FH	ROM
20H	22H	150 ns
22H	01H	2 Kb
24H	FFH	END OF DEVICE
26H	1DH	**CISTPL_DEVICE_OA**
28H	05H	TPL_LINK
2AH	02H	OTHER CONDITIONS—3 V_{CC}
2CH	17H	ROM
2EH	2AH	200 ns
30H	01H	2 Kb
32H	FFH	END OF DEVICE
34H	18H	**CISTPL_JEDEC_C**
36H	02H	TPL_LINK
38H	89H	INTEL J-ID
3AH	A0H	28F016 J-ID
3CH	00H	Null Control Tuple

Table 5. Series 2+ Tuples (Continued)

Address	Value	Description
3EH	15H	**CISTPL VERS 1**
40H	39H	TPL_LINK
42H	04H	TPLLV1_MAJOR
44H	01H	TPLLV1_MINOR
		TPLLV1_INFO
46H	49H	I
48H	6EH	n
4AH	74H	t
4CH	65H	e
4EH	6CH	l
50H	00H	END TEXT
52H	53H	S
54H	32H	2
56H	45H	E
58H	34H	4 MB
	32H	20 MB
5AH	20H	4 MB
	30H	20 MB
5CH	53H	S
	20H	SPACE
5EH	57H	W
	20H	SPACE
60H	00H	ENDTEXT
62H	43H	C
64H	4FH	O
66H	50H	P
68H	59H	Y
6AH	52H	R
6CH	49H	I
6EH	47H	G
70H	48H	H
72H	54H	T
74H	20H	SPACE
76H	49H	I
78H	6EH	n
7AH	74H	t
7CH	65H	e
7EH	6CH	l
80H	20H	SPACE
82H	43H	C
84H	4FH	O
86H	52H	R
88H	50H	P
8AH	4FH	O
8CH	52H	R
8EH	41H	A
90H	54H	T
92H	49H	I
94H	4FH	O
96H	4EH	N
98H	20H	SPACE
9AH	31H	1
9CH	39H	9
9EH	39H	9
A0H	33H	3
A2H	20H	SPACE
A4H	47H	G
A6H	4CH	L
A8H	41H	A
AAH	44H	D
ACH	45H	E
AEH	4BH	K
B0H	00H	END TEXT
B2H	FFH	END OF LIST
B4H	1AH	**CISTPL_CONF**
B6H	05H	TUPL_LINK
B8H	01H	TPCC_SZ
BAH	04H	TPCC_LAST
BCH	00H	TPCC_RADR
BEH	40H	TPCC_RADR

Table 5. Series 2+ Tuples (Continued)

Address	Value	Description
C0H	03H	TPCC_RMSK
C2H	00H	NULL CONTROL TUPLE
C4H	1BH	**CISTPL_CFTABLE_ENTRY**
C6H	08H	TPL_LINK
C8H	01H	**TPCE_INDEX (01H)**
CAH	01H	TPCE_FS (V_{CC} ONLY)
CCH	79H	TPCE_PD V_{CC} PARAMETER SELECTION BYTE
CEH	55H	V_{CC} NOMINAL VOLTAGE 5V ±5%
D0H	53H	I_{CC} STATIC 500 µA
D2H	1EH	I_{CC} AVERAGE 150 mA
D4H	1EH	I_{CC} PEAK 150 mA
D6H	1BH	I_{CC} PWRDWN 200 µA
D8H	1BH	CISTPL_CFTABLE_ENTRY
DAH	0FH	TPL_LINK
DCH	02H	**TPCE_INDEX (02H)**
DEH	02H	TPCE_FS (V_{CC} AND V_{PP})
E0H	79H	TPCE_PD V_{CC} PARAMETER SELECTION BYTE
E2H	55H	V_{CC} NOMINAL VOLTAGE 5V ±5%
E4H	2BH	I_{CC} STATIC 250 µA
E6H	06H	I_{CC} AVERAGE 100 mA
E8H	06H	I_{CC} PEAK 100 mA
EAH	52H	I_{CC} PWRDWN 50 µA
ECH	79H	TPCE_PD V_{PP} PARAMETER SELECTION BYTE
EEH	8EH	12.0V ±5%
F0H	7DH	NC OK ON STANDBY & PWD
F2H	53H	I_{PP} STATIC 500 µA
F4H	25H	I_{PP} AVERAGE 20 mA
F6H	25H	I_{PP} PEAK 20 mA
F8H	52H	I_{PP} PWRDWN 50 µA
FAH	1BH	CISTPL_CFTABLE_ENTRY
FCH	09H	TPL_LINK
FEH	03H	**TPCE_INDEX (03H)**
100H	01H	TPCE_FS (V_{CC} ONLY)
102H	79H	TPCE_PD V_{CC} PARAMETER SELECTION BYTE
104H	B5H	V_{CC} = 3.3V
106H	1EH	EXTENSION BYTE
108H	04H	I_{CC} STATIC 1 mA
10AH	1EH	I_{CC} AVERAGE 150 mA
10CH	1EH	I_{CC} PEAK 150 mA
10EH	53H	I_{CC} PWRDWN 500 µA
110H	1BH	CISTPL_CFTABLE_ENTRY
112H	10H	TPL_LINK
114H	04H	**TPCE_INDEX (04H)**
116H	02H	TPCE_FS (V_{CC} AND V_{PP})
118H	79H	TPCE_PD V_{CC} PARAMETER SELECTION BYTE
11AH	B5H	V_{CC} = 3.3V
11CH	1EH	EXTENSION BYTE
11EH	2BH	I_{CC} STATIC 250 µA
120H	06H	I_{CC} AVERAGE 100 mA
122H	06H	I_{CC} PEAK 100 mA
124H	52H	I_{CC} PWRDWN 50 µA
126H	79H	TPCE_PD V_{PP} PARAMETER SELECTION BYTE
128H	8EH	12.0V ±5%
12AH	7DH	NC OK ON STANDBY & PWD
12CH	53H	I_{PP} STATIC 500 µA
12EH	25H	I_{PP} AVERAGE 20 mA
130H	25H	I_{PP} PEAK 20 mA
132H	1BH	I_{PP} PWRDWN 150 µA
134H	00H	NULL CONTROL TUPLE
136H	00H	NULL CONTROL TUPLE
138H	1EH	**CISTPL DEVICEGEO**
13AH	06H	TPL_LINK
13CH	02H	DGTPL_BUS
13EH	11H	DGTPL_EBS
140H	01H	DGTPL_RBS
142H	01H	DGTPL_WBS

Table 5. Series 2+ Tuples (Continued)

Address	Value	Description
144H	01H	DGTPL_PART=1
146H	01H	FLASH DEVICE INTERLEAVE
148H	20H	**CISTPL MANFID**
14AH	04H	TPL_LINK (04H)
		TPLMID_MANF
14CH	89H	LSB
14EH	00H	MSB
150H	11H	4 MB—200 ns
	41H	20 MB—200 ns
	10H	4 MB—250 ns
	40H	20 MB—250 ns
152H	83H	TPLMID_CARD MSB
	84H	TPLMID_CARD MSB
154H	21H	CISTPL_FUNCID
156H	02H	TPL_LINK
158H	01H	TPLFID_FUNCTION (MEMORY)
15AH	00H	TPLFID_SYSINIT (NONE)
15CH	FFH	**CISTPL_END**
	00H	INVALID ECIS ADDRESS (15EH-1FEH)

SYSTEM DESIGN CONSIDERATIONS

POWER SUPPLY DECOUPLING

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby, active and transient current peaks which are produced by rising and falling edges of $CE_1\#$ and $CE_2\#$. The capacitive and inductive loads on the card and internal flash memory device pairs determine the magnitudes of these peaks.

Three-line control and proper decoupling capacitor selection suppress transient voltage peaks. Series 2+ Cards contain on-card ceramic decoupling capacitors connected between V_{CC} and GND, and between V_{PP1}/V_{PP2} and GND.

The card connector should also have a 4.7 µF electrolytic capacitor between V_{CC} and GND, as well as between V_{PP1}/V_{PP2} and GND. The bulk capacitors overcome voltage slumps caused by printed-circuit-board trace inductance, and supply charge to the smaller capacitors as needed.

POWER UP/DOWN PROTECTION

The PCMCIA/JEIDA specified socket properly sequences the power supplies and control signals to the flash memory card via shorter and longer pins. This assures that hot insertion and removal will not result in card damage or data loss.

Each device in the card is designed to offer protection against accidental erasure or writing, caused by spurious system-level signals that may exist during power transitions. The card will power up into the read state.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and $CE_1\#$ must be low for a command write, driving either to V_{IH} will inhibit writes. With its control register architecture, alteration of device contents only occurs after successful completion of the two-step command sequences. While these precautions are sufficient for most applications, an alternative approach would allow V_{CC} to reach its steady state value before raising V_{PP1}/V_{PP2} above V_{CC} + 2.0V. In addition, upon powering down, V_{PP1}/V_{PP2} should be below V_{CC} + 2.0V before lowering V_{CC}.

NOTE:
The Integrated V_{PP} generator defaults to the power off condition after reset and system power up.

HOT INSERTION/REMOVAL

The capability to remove or insert PC cards while the system is powered on (i.e., hot insertion/removal) requires careful design techniques on the system and card levels. To design for this capability consider card over-voltage stress, system power droop and control line stability.

OPERATION SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .... 0°C to +60°C(1)
During Erase/Write .... 0°C to +60°C
Storage Temperature.......... −30°C to +70°C(2)
Voltage on Any Pin with
Respect to Ground ... −2.0V to $+V_{CC}$ + 2.0V(2)
$V_{PP}1/V_{PP}2$ Supply Voltage with
Respect to Ground
during Erase/Write .... −2.0V to +14.0V(2, 3)
V_{CC} Supply Voltage with
Respect to Ground .... −0.5V to +6.0V

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum D.C. input voltage is −0.5V. During transitions, inputs may undershoot to 2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum D.C. input voltage on V_{PP1}/V_{PP2} may overshoot to +14.0V for periods less than 20 ns.

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
$V_{CC3.3}$	V_{CC} Supply Voltage (5%)	3.0	3.6	V
V_{CC5}	V_{CC} Supply Voltage (5%)	4.75	5.25	V

SERIES 2+ DC CHARACTERISTICS, GENERAL

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1, 3	±1	±20	μA	$V_{CC} = V_{CC}$ MAX $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1	±1	±20	μA	$V_{CC} = V_{CC}$ MAX $V_{OUT} = V_{CC}$ or GND
V_{IL}	Input Low Voltage	1	−0.5	0.8	V	Min = −0.3V for 3.3V V_{CC}
V_{IH}	Input High Voltage	1	$0.7V_{CC}$	V_{CC} +0.3	V	Max = V_{CC} +0.5V for 5V V_{CC}
V_{OL}	Output Low Voltage	1		0.4	V	Max = 0.45V for 5V w/I_{OH} = −2.0mA
V_{OH1}	Output High Voltage (@3.3V)	1	2.4		V	
V_{OH2}	Output High Voltage (@5.0V)	1	$0.85V_{CC}$		V	I_{OH} = −2.5mA
V_{PPL}	V_{PP} during Read Only Operations	1, 2	0.0	6.5	V	
V_{PPH}	V_{PP} during Read/Write Operations	1	11.4	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage	1	2.0		V	

NOTES:
1. Values are the same for byte and word wide modes and for all card densities.
2. Block Erases/Data Writes are inhibited when V_{PP} and V_{PPL} are not guaranteed in the range between V_{PPH} and V_{PPL}.
3. Exceptions: With V_{IN} = GND, the leakage on CE_1#, CE_2#, REG#, OE# and WE# will be ≤500 μA due to internal pull up resistors and, with $V_{IN} = V_{CC}$, RST leakage will be ≤500 μA due to internal pull-down resistors.

SERIES 2+ DC CHARACTERISTICS(1) V_{CC} = 5V, V_{PP} = 12V

Symbol	Parameters	Density (MBytes)	Notes	x8 Mode		x16 Mode		Units	Test Conditions
				Typ	Max	Typ	Max		
I_{CCR}	V_{CC} Read Current	4, 20	2, 3		85		120	mA	V_{CC} = V_{CC} MAX t_{CYCLE} = 150ns
I_{CCW}	V_{CC} Write Current	4, 20	2, 3		85		120	mA	Data Write in Progress
I_{CCE}	V_{CC} Erase Current	4, 20	2, 3		75		100	mA	Block (Pair) Erase in Progress
I_{CCSL}	V_{CC} Sleep Current	4		12	20	12	20	µA	
		20		20	60	20	60	µA	
I_{CCS}	V_{CC} Standby Current	4, 20	2, 3	61	115	170	210	µA	V_{CC} = V_{CC} MAX Control Signals = V_{IH}
I_{PPW}	V_{PP} Write Current (V_{PP} = V_{PPH})	4, 20	2, 3	7	12	14	24	mA	Data Write in Progress
I_{PPE}	V_{PP} Erase Current (V_{PP} = V_{PPH})	4, 20	2, 3	5	10	10	20	mA	Block (Pair) Erase in Progress
I_{PPSL}	V_{PP} Sleep Current	4		0		0		µA	V_{PP} = 0V
		20		0		0		µA	
I_{PPS_1}	V_{PP} Standby or Read Current ($V_{PP} \leq V_{CC}$)	4	2, 3	0		0		µA	V_{PP} = 0V
		20		0		0		µA	

NOTES:

1. All currents are RMS values unless otherwise specified. Typical V_{CC} = 5V, V_{PP} = 12V, T = 25°C.
2. Two devices active in word mode, one device active in byte mode.
3. Currents are not added in for devices not accessed or in sleep mode.

SERIES 2+ DC CHARACTERISTICS, CMOS(1) V_{CC} = 5V, V_{PP} = 0V**

Symbol	Parameters	Density (MBytes)	Notes	x8 Mode		x16 Mode		Units	Test Conditions
				Typ	Max	Typ	Max		
I_{CCR}	V_{CC}Read Current	4, 20	2, 3, 4		85		120	mA	V_{CC} = V_{CC} MAX t_{CYCLE} = 200ns
I_{CCW}	V_{CC} Write Current	4, 20	2, 3, 5		119		188	mA	Data Write in Progress
I_{CCE}	V_{CC} Erase Current	4, 20	2, 3, 5		104		157	mA	Block Erase in Progress
I_{CCSL}	V_{CC} Sleep Current	4	4		20		20	µA	
		20			60		60	µA	
I_{CCS}	V_{CC} Standby Current	4, 20	3, 4		640		750	µA	V_{CC} = V_{CC} MAX Control Signals = V_{IH}

** I_{PP} specs not included because all I_{PP} is derived from I_{CC} via the internal V_{PP} Generation Circuitry.

NOTES:

1. All currents are RMS values unless otherwise specified. Typical V_{CC} = 3.3V, V_{PP} = 12V, T = 25°C.
2. Two devices active in word mode, one device active in byte mode.
3. Currents are not added in for devices not accessed or in sleep mode.
4. V_{PP} Generation Circuitry turned off.
5. V_{PP} Generation Circuitry turned on.

SERIES 2+ DC CHARACTERISTICS(1) V_{CC} = 3.3V, V_{PP} = 12V

Symbol	Parameters	Density (MBytes)	Notes	x8 Mode		x16 Mode		Units	Test Conditions
				Typ	Max	Typ	Max		
I_{CCR}	V_{CC}Read Current	4, 20	2, 3		44		64	mA	V_{CC} = V_{CC} MAX t_{CYCLE} = 200ns
I_{CCW}	V_{CC} Write Current	4, 20	2, 3		36		48	mA	Data Write in Progress
I_{CCE}	V_{CC} Erase Current	4, 20	2, 3		36		48	mA	Block (Pair) Erase in Progress
I_{CCSL}	V_{CC} Sleep Current	4			20		20	µA	
		20			60		60	µA	
I_{CCS}	V_{CC} Standby Current	4, 20	2, 3		115		210	µA	V_{CC} = V_{CC} MAX Control Signals = V_{IH}
I_{PPW}	V_{PP} Write Current (V_{PP} = V_{PPH})	4, 20	2, 3	10	15	20	30	mA	Data Write in Progress
I_{PPE}	V_{PP} Erase Current (V_{PP} = V_{PPH})	4, 20	2, 3	6	12	12	22	mA	Block (Pair) Erase in Progress
I_{PPSL}	V_{PP} Sleep Current	4		0		0		µA	V_{PP} = 0V
		20		0		0		µA	
I_{PPS_1}	V_{PP} Standby or Read Current	4	2,3	0		0		µA	V_{PP} = 0V
		20		0		0		µA	

NOTES:

1. All currents are RMS values unless otherwise specified. Typical V_{CC} = 3.3V, V_{PP} = 12V, T = 25°C.
2. Two devices active in word mode, one device active in byte mode.
3. Currents are not added in for devices not accessed or in sleep mode.

SERIES 2+ DC CHARACTERISTICS(1) V_{CC} = 3.3V, V_{PP} = 0V**

Symbol	Parameters	Density (MBytes)	Notes	x8 Mode		x16 Mode		Units	Test Conditions
				Typ	Max	Typ	Max		
I_{CCR}	V_{CC} Read Current	4, 20	2, 3, 4		44		64	mA	V_{CC} = V_{CC} MAX t_{CYCLE} = 200ns
I_{CCW}	V_{CC} Write Current	4, 20	2, 3, 5		100		177	mA	Data Write in Progress
I_{CCE}	V_{CC} Erase Current	4, 20	2, 3, 5		79		134	mA	Block (Pair) Erase in Progress
I_{CCSL}	V_{CC} Sleep Current	4	4		12		20	µA	
		20			20		60	µA	
I_{CCS}	V_{CC} Standby Current	4, 20	3, 4		115		210	µA	V_{CC} = V_{CC} MAX Control Signals = V_{IH}

** I_{PP} specs not included because all I_{PP} is derived from I_{CC} via the internal V_{PP} Generation Circuitry.

NOTES:

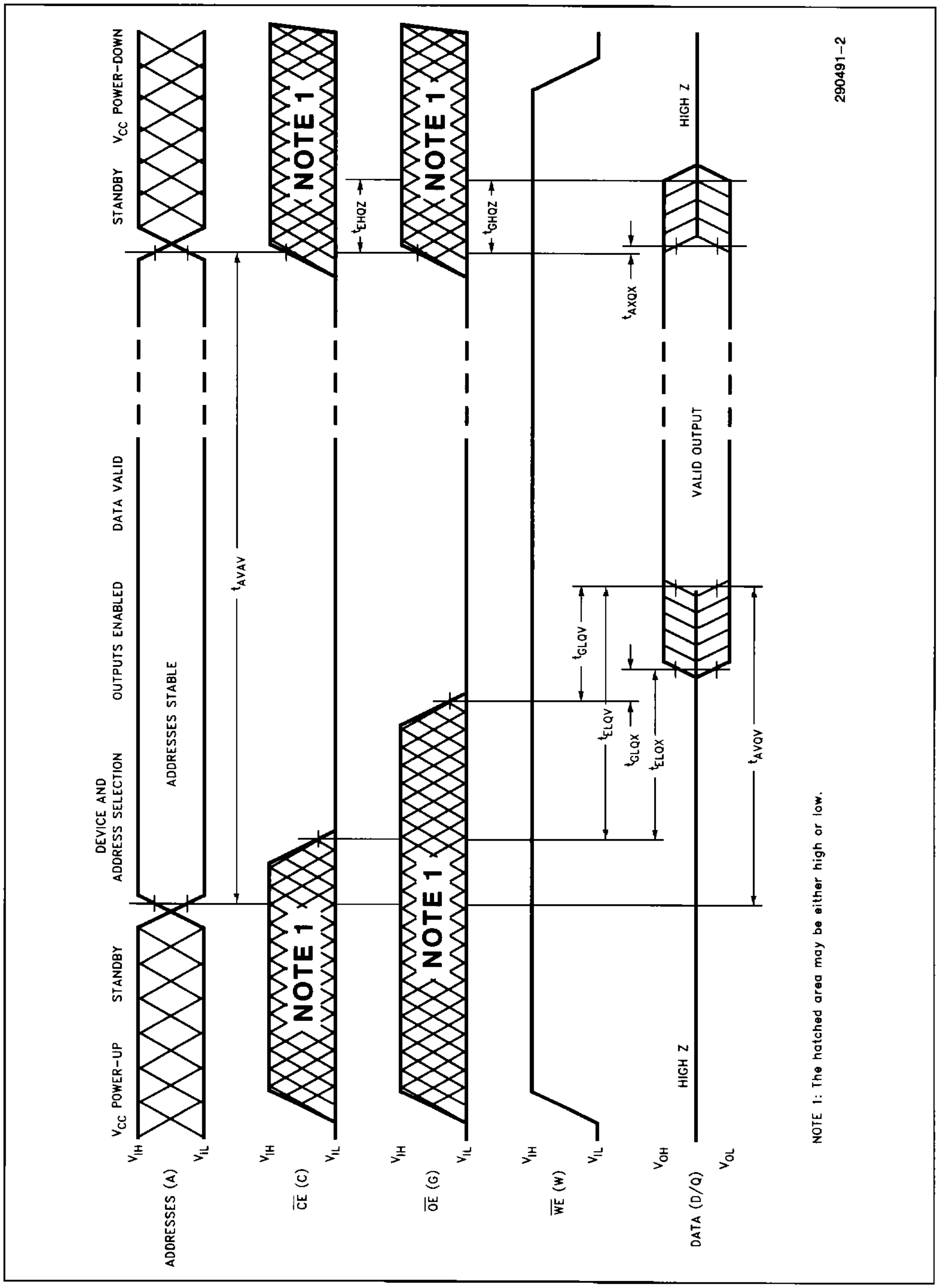
1. All currents are RMS values unless otherwise specified. Typical V_{CC} = 3.3V, V_{PP} = 12V, T = 25°C.
2. Two devices active in word mode, one device active in byte mode.
3. Currents are not added in for devices not accessed or in sleep mode.
4. V_{PP} Generation Circuitry turned off.
5. V_{PP} Generation Circuitry turned on.

AC CHARACTERISTICS

AC Timing Diagrams and characteristics are guaranteed to meet or exceed PCMCIA Release 2.01 specifications. No delay occurs when switching between the Common and Attribute Memory Planes.

COMMON AND ATTRIBUTE MEMORY Read-Only Operations

Symbol		Parameter	Notes	200 ns		250 ns		Units
JEDEC	PCMCIA			Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time		200		250		ns
t_{AVQV}	t_a (A)	Address Access Time			200		250	ns
t_{ELQV}	t_a (CE)	Card Enable Access Time			200		250	ns
t_{GLQV}	t_a (OE)	Output Enable Access Time			100		125	ns
t_{EHQX}	t_{dis} (CE)	Output Disable Time from CE#			90		100	ns
t_{GHQZ}	t_{dis} (OE)	Output Disable Time from OE#			90		100	ns
t_{GLQX}	t_{en} (CE)	Output Enable Time From CE#		5		5		ns
t_{ELQX}	t_{en} (OE)	Output Enable Time from OE#		5		5		ns
t_{PHQV}		Powerdown Recovery to Output Delay. V_{CC} = 5V			530		530	ns
		Powerdown Recovery to Output Delay. V_{CC} = 3.3V			670		670	ns
	t_{su} (V_{CC})	CE Setup Time on Powerup		0		0		ms



NOTE 1: The hatched area may be either high or low.

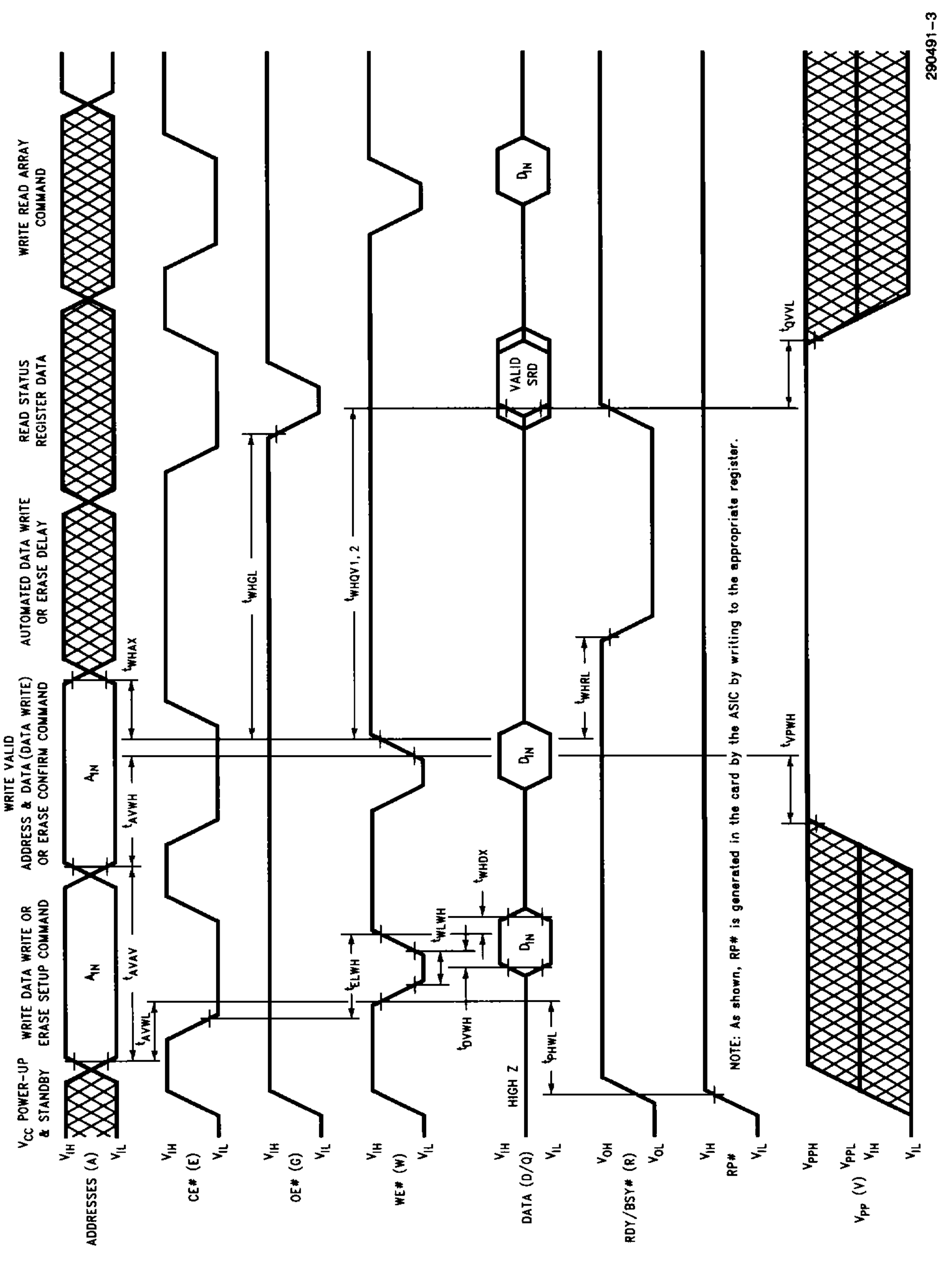
Figure 16. AC Waveform for Read Operations

COMMON AND ATTRIBUTE MEMORY Write Operations(1)

Symbol		Parameter	Notes	200 ns		250 ns		Units
JEDEC	PCMCIA			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time		200		250		ns
t_{WLWH}	t_w (WE)	Write Pulse Width		120		150		ns
t_{AVWL}	t_{su} (A)	Address Setup Time		20		30		ns
t_{AVWH}	t_{su} (A-WEH)	Address Setup Time for WE#		140		180		ns
t_{VPWH}	t_{vps}	V_{PP} Setup to WE# Going High		100		100		ns
t_{ELWH}	t_{su} (CE-WEH)	Card Enable Setup Time for WE#		140		180		ns
t_{DVWH}	t_{su} (D-WEH)	Data Setup Time for WE#		60		80		ns
t_{WHDX}	t_n (D)	Data Hold Time		30		30		ns
t_{WHAX}	t_{rec} (WE)	Write Recover Time		30		30		ns
t_{WHRL}		WE# High to RDY/BSY#			140		140	ns
t_{WHQV1}		Duration of Data Write Operation			6		6	μs
t_{WHQV2}		Duration of Block Erase Operation		0.3		0.3		sec
t_{QVVL}		V_{PP} Hold from Operation Complete		0		0		ns
t_{WHGL}	t_h (OE-WE)	Write Recovery Before Read		10		10		ns
t_{PHWL}		Powerdown Recovery to WE# Going Low		1		1		us

NOTE:

1. Read timing charateristics during erase and data write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only operations.



NOTE: As shown, RP# is generated in the card by the ASIC by writing to the appropriate register.

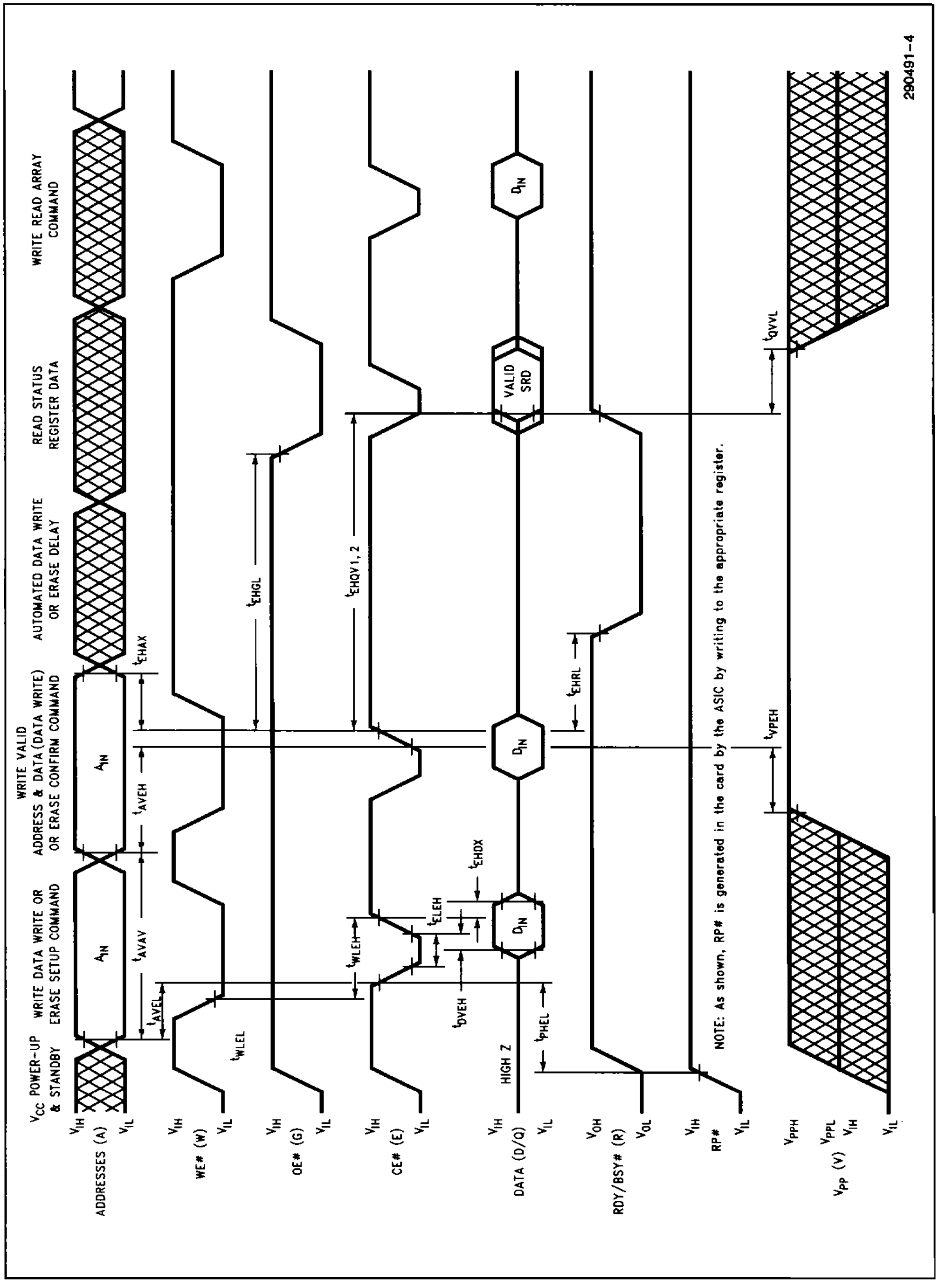
Figure 17. AC Waveform for Write Operations

COMMON AND ATTRIBUTE MEMORY CE#-Controlled Write Operations(1)

Symbol		Parameter	Notes	200 ns		250 ns		Units
JEDEC	PCMCIA			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time		200		250		ns
t_{ELEH}	t_w (WE)	Chip Enable Pulse Width		120		150		ns
t_{AVEL}	t_{su} (A)	Address Setup Time		20		20		ns
t_{AVEH}	t_{su} (A-WEH)	Address Setup Time for CE#		140		180		ns
t_{VPEH}	t_{vps}	V_{PP} Setup to CE# Going High		100		100		ns
t_{WLEH}	t_{su} (CE-WEH)	Write Enable Setup Time for CE#		140		180		ns
t_{DVEH}	t_{su} (D-WEH)	Data Setup Time for CE#		60		80		ns
t_{EHDX}	t_H (D)	Data Hold Time		30		30		ns
t_{EHAX}	t_{rec} (WE)	Write Recover Time		30		30		ns
t_{EHRL}		CE# High to RDY/BSY#			140		140	ns
t_{EHQV1}		Duration of Data Write Operation			9		9	µs
t_{EHQV2}		Duration of Block Erase Operation		0.3		0.3		sec
t_{QVVL}		V_{PP} Hold from Operation Complete		0		0		ns
t_{EHGL}	t_h (OE-WE)	Write Recovery Before Read		10		10		ns
t_{PHEL}		Powerdown Recovery to CE# Going Low		1		1		µs

NOTE:

1. Read timing characteristics during erase and data write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only operations.



NOTE: As shown, RP# is generated in the card by the ASIC by writing to the appropriate register.

Figure 18. Alternate AC Waveform for Write Operations

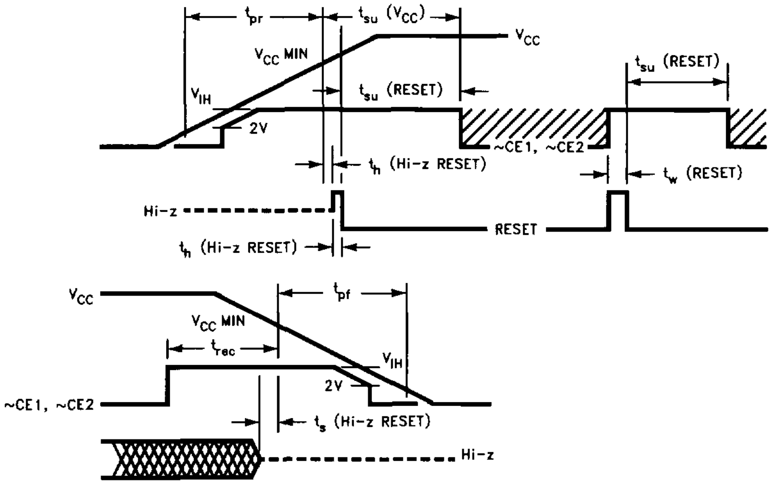
POWER-UP/POWER-DOWN

Symbol	Parameter	Notes	Min	Max	Units
PCMCIA					
V_i (CE)	CE# Signal Level (0V < V_{CC} < 2.0V)	1	0	ViMAX	V
	CE# Signal Level (2.0V < V_{CC} < V_{IH})	1	$V_{CC} - 0.1$	ViMAX	V
	CE# Signal Level (V_{IH} < V_{CC})	1	V_{IH}	ViMAX	V
t_{su} (V_{CC})	CE# Setup Time		20		ms
t_{su} (RESET)	CE# Setup Time		20		ms
t_{rec} (V_{CC})	CE# Recover Time		1.0		µs
t_{pr}	V_{CC} Rising Time	2	0.1	300	ms
t_{pf}	V_{CC} Falling Time	2	3.0	300	ms
t_w (RESET)	RESET Width		10		µs
t_h (Hi-Z Reset)	RESET Width		1		ms
t_s (Hi-Z Reset)	RESET Width		0		ms

NOTES:

1. V_{iMAX} means Absolute Maximum Voltage for input in the period of 0V < V_{CC} < 2.0V, V_i (CE#) is only 0V ~ V_{iMAX}
2. The t_{pr} and t_{pf} are defined as "linear waveforms" in the period of 10% to 90% or vice-versa. Even if the waveform is not a "linear waveform", its rising and falling time must meet this specification.

Power-Up/Down Timing for Systems Supporting RESET

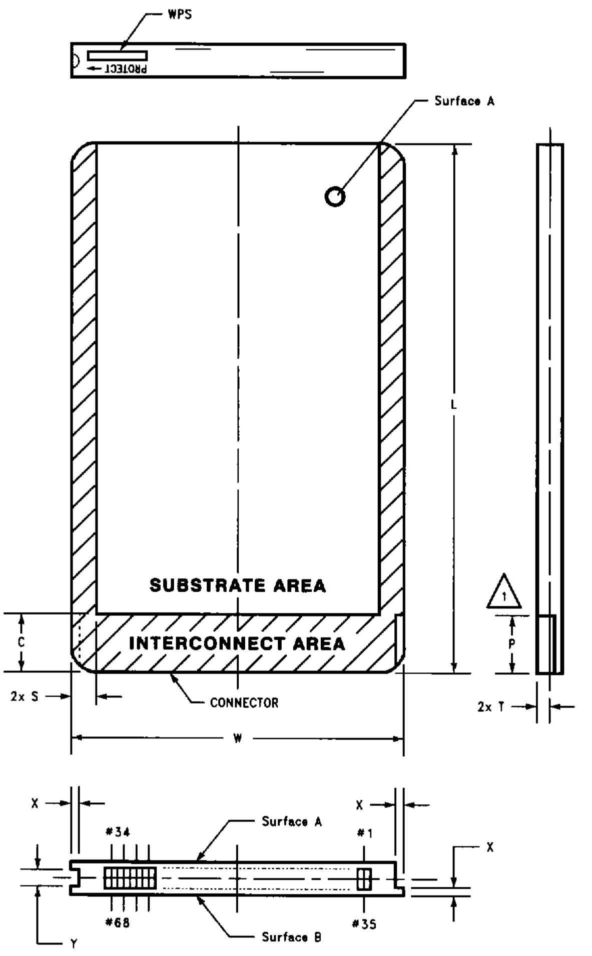


290491-5

CAPACITANCE $T_A = 25°C, f = 1.0\ MHz$

Symbol	Pins	Typ	4MB	Units
			Max	
C_{IN}	A_0	15	30	pF
C_{IN}	Address/Control	10	20	pF
C_{IN}	V_{CC}, V_{PP}	2	2	µF
C_{OUT}	Output	10	20	pF

PACKAGING



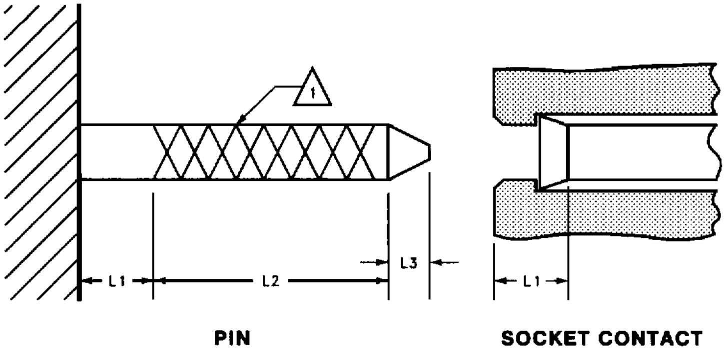
C MIN	L ± 0.008	P MIN △1	S MIN	T △2	W ± 0.004	X ± 0.002	Y ± 0.002
0.294 (10.0)	3.370 (85.60)	0.394 (10.0)	0.118 (3.0)	0.065 (1.65)	2.126 (54.0)	0.039 (1.00)	0.063 (1.60)

△1 POLARIZATION KEY LENGTH.

△2 INTERCONNECT AREA TOLERANCE = ±0.002
SUBSTRATE AREA TOLERANCE = ±0.004

3 MILLIMETERS ARE IN PARENTHESIS().

290491–6



△1 PIN/SOCKET CONTACT AREA

2. MILLIMETERS ARE IN PARENTHESIS ()

290491-7

ORDERING INFORMATION

iMC020FLSP,SBXXXXX

WHERE:

i = INTEL
MC = MEMORY CARD
020 = DENSITY IN MEGABYTES (004,020 AVAILABLE)
FL = FLASH TECHNOLOGY
S = BLOCKED ARCHITECTURE
P = PERFORMANCE
SBXXXXX = CUSTOMER IDENTIFIER

ADDITIONAL INFORMATION

References

Available Documentation

Document	Order Number
SERIES 2 FLASH MEMORY CARD Data Sheet	290434
SERIES 2+ Flash Memory Card User's Manual	297373
28F016SA 16 Mbit (1Mbit x 16, 2Mbit x 8) FlashFile™ Memory Data Sheet	290489
28F008SA 8 Mb (1Mb x 8) FlashFile™ Memory Data Sheet	290429
AP-357 Power Supply Solutions for Flash Memory	292092
AP-362 Implementing Mobile PC Designs Using High Density FlashFile™ Components	292097
AP-377 The 28F016SA Software Drivers	292126
AP-378 Enhanced Features of the 28F016SA	292127
ER-31 The 28F016SA FlashFile™ Memory	294015
ER-33 ETOX™ IV Flash Memory Technology	294016