ECG® Semiconductors

ECG937, ECG937M

JFET Input Op Amplifier

Features

- Wider bandwidth decompensated (A_{Vmin} = 6)
- Low input bias current — 30 pA
- Low input offset current — 3.0 pA
- Low input offset voltage — 1.0 mV
- Temperature compensation of input offset voltage — 3.0 μV/°C
- Low input noise current — 0.01 pA/√Hz
- High input impedance — $10^{12}\Omega$
- High common-mode rejection ratio — 100 dB
- High DC voltage gain — 106 dB

This internally compensated operational amplifier incorporates highly matched JFET devices on the same chip with standard bipolar transistors. The JFET device enhances the input characteristics of the operational amplifier by more than an order of magnitude over conventional amplifiers.

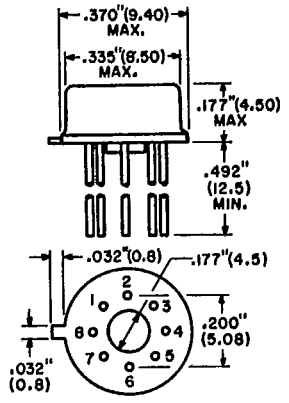
This op amp combines the low current characterisitics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also, nulling the offset voltages does not degrade the drift or common mode rejection.

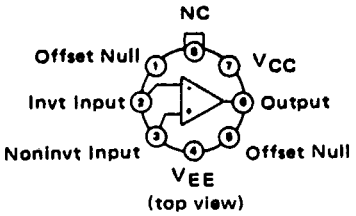
The device is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Applications

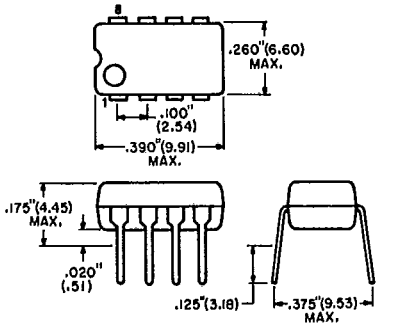
- Sample and hold circuits
- High impedance buffers
- Fast D/A and A/D converters
- Precision high-speed integrators
- Wideband, low noise, low drift amplifiers

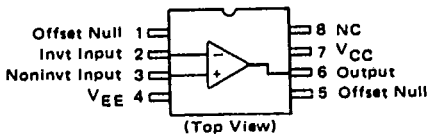
ECG937





ECG937M





Maximum Ratings

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range(Note 1)	V_{IDR}	±16	V
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Metal Package Plastic Package	T_{opg}	 115 100	°C
Storage Temperature Range Metal Package Plastic Package	T_{stg}	 −65 to +150 −55 to +125	°C

Note 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

Electrical Characteristics (V_{CC} = 15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} (Note 2) unless otherwise noted)

DC Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0) (T_A = 25°C) (Over Temperature)	V_{IO}	 -- --	 3.0 --	 10 13	mV
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)	$\Delta V_{IO}/\Delta T$	--	5.0	--	μV/°C
Change in Average TC with V_{IO} Adjust (R_S = 50 Ω) (Note 3)	$\Delta TC/\Delta V_{IO}$	--	0.5	--	μV/°C per mV
Input Offset Current (V_{CM} = 0) (Note 4) (T_{opg} = 25°C) (T_{opg}<T_{high}) (Note 2)	I_{IO}	 -- --	 3.0 --	 50 2.0	 pA nA
Input Bias Current (V_{CM} = 0) (Note 4) (T_{opg} = 25°C) (T_{opg}<T_{high}) (Note 2)	I_{IB}	 -- --	 30 --	 200 8.0	 pA nA
Input Resistance (T_{opg} = 25°C)	r_i	--	10^{12}	--	Ω
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k, V_{CC} = 15 V, V_{EE} = −15 V) (T_A = 25°C) (Over Temperature)	A_{VOL}	 25 15	 200 --	 -- --	V/mV
Output Voltage Swing (V_{CC} = 15 V, V_{EE} = −15 V, R_L = 10 kΩ) (V_{CC} = 15 V, V_{EE} = −15 V, R_L = 2 kΩ)	V_O	 ±12 ±10	 ±13 ±12	 -- --	V
Input Common-Mode Voltage Range (V_{CC} = 15 V, V_{EE} = −15 V)	V_{ICR}	±10	±15.1 −12.0	--	V
Common-Mode Rejection Ratio	CMRR	80	100	--	dB
Supply Voltage Rejection Ratio (Note 5)	PSRR	80	100	--	dB
Supply Current (T_A = 25°C, V_{CC} = 15 V, V_{EE} = −15 V)	I_D	--	5.0	10	mA

AC Characteristic (T_A = 25°C)	Symbol	Min	Typ	Max	Unit
Slew Rate (Note 6) (A_V = 5)	SR	30	50	--	V/μs
Gain-Bandwidth Product	BWp	--	20	--	MHz
Settling Time to 0.01% (Note 6)	t_s	--	1.5	--	μs
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 100 Hz) (R_S = 100 Ω, f = 1000 Hz)	en	-- --	15 12	-- --	nV/√Hz
Equivalent Input Noise Current (f = 100 Hz) (f = 1000 Hz)	in	-- --	0.01 0.01	-- --	pA/√Hz
Input Capacitance	Ci	--	3.0	--	pF

Notes

(1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

(2) T_{low} = 0°C
T_{high} = +70°C

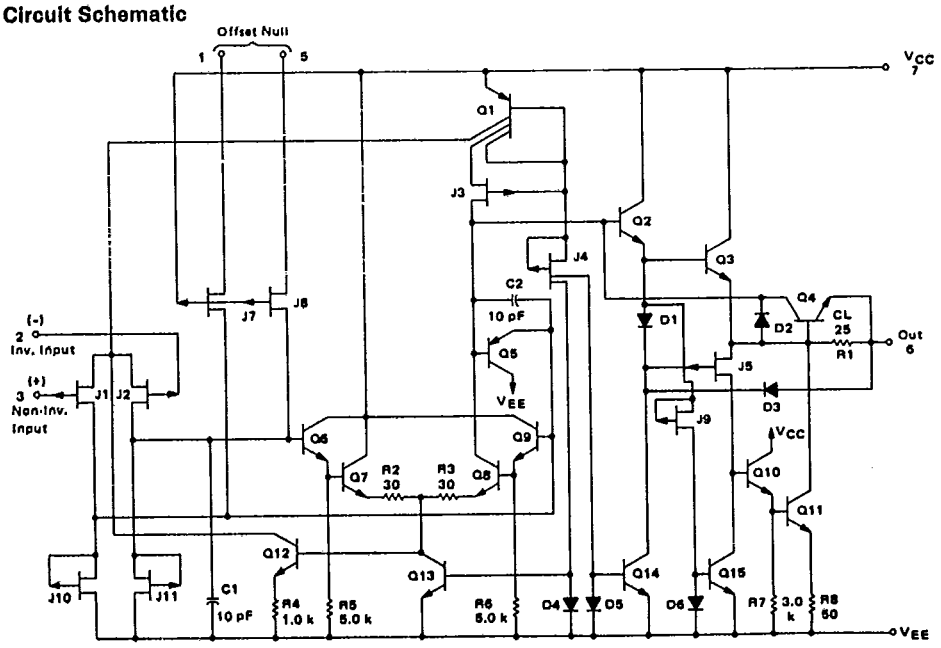
(3) The temperature coefficient of the adjusted input offset voltage changes only a small amount of (0.5 μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

(4) The input bias currents approximately double for every 10°C rise in junction temperature, T_{opg}. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(5) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

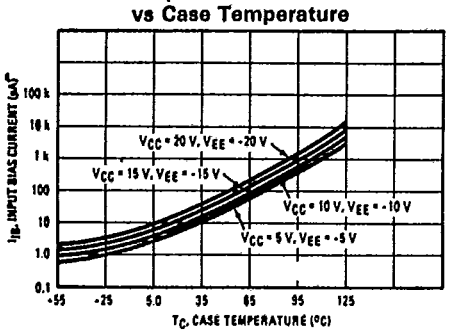
(6) A_V = −5.0, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

Circuit Schematic

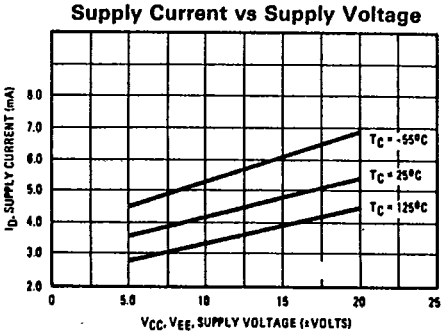


Typical DC Performance Characteristics

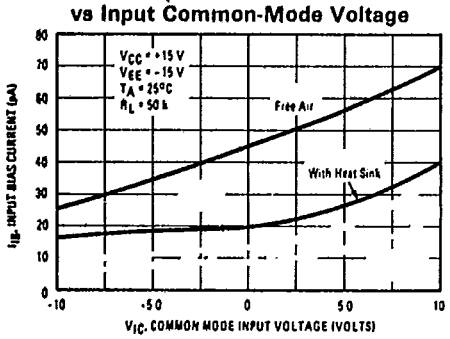
Input Bias Current vs Case Temperature



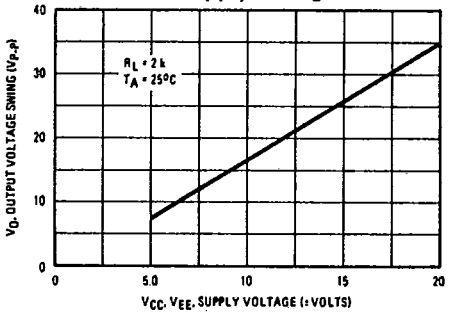
Supply Current vs Supply Voltage



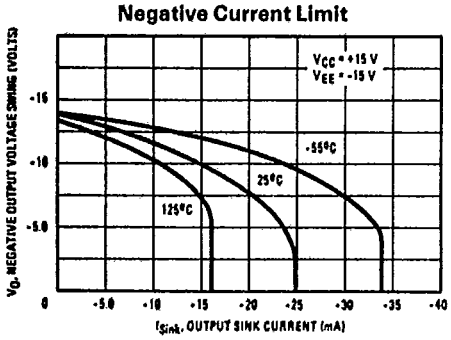
Input Bias Current vs Input Common-Mode Voltage



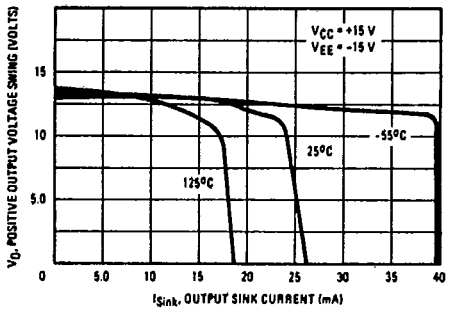
Output Voltage Swing vs Supply Voltage



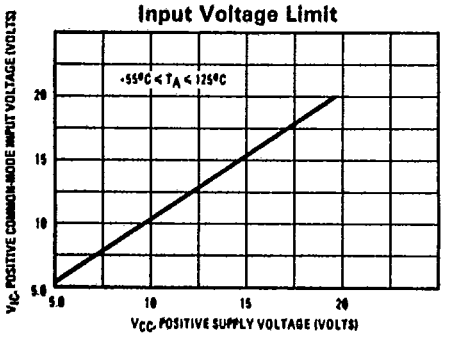
Negative Current Limit



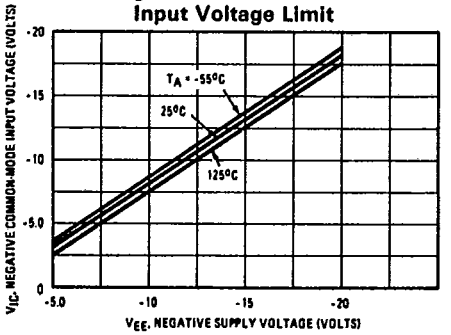
Positive Current Limit



Positive Common-Mode Input Voltage Limit

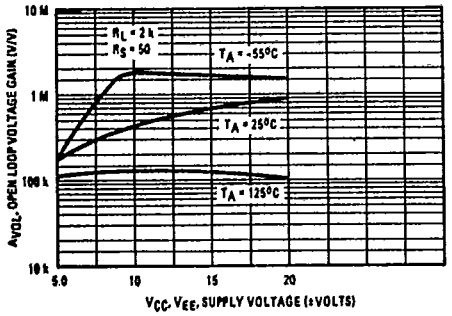


Negative Common-Mode Input Voltage Limit

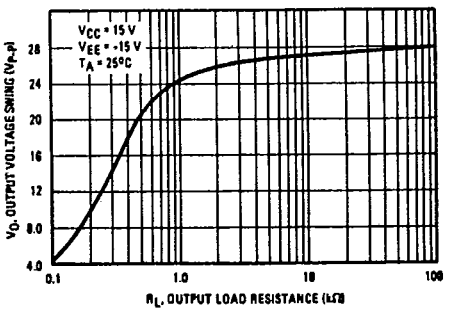


Typical DC Performance Characteristics (Cont.)

Open Loop Voltage Gain

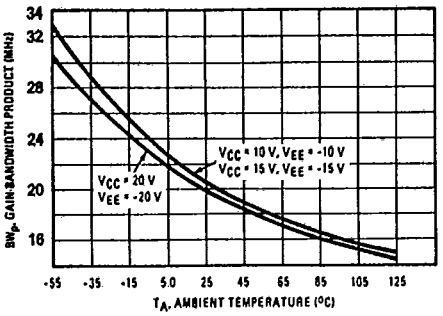


Output Voltage Swing vs Load Resistance

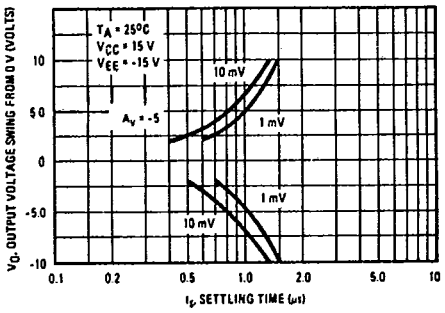


Typical AC Performance Characteristics

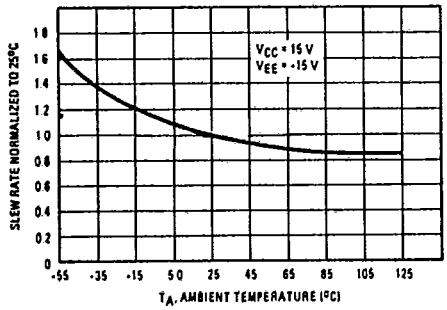
Gain Bandwidth Product



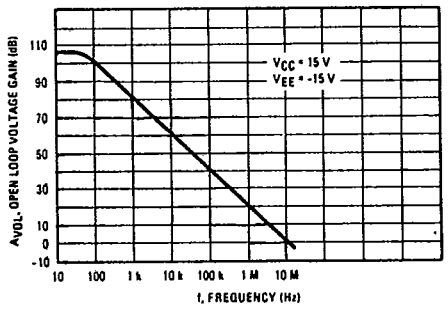
Inverter Settling Time



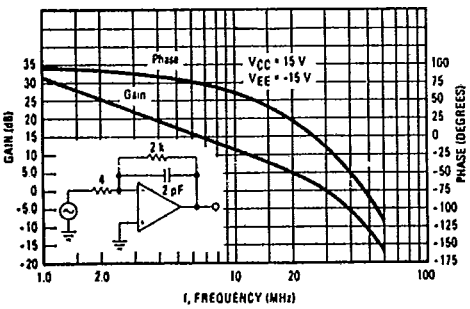
Normalized Slew Rate



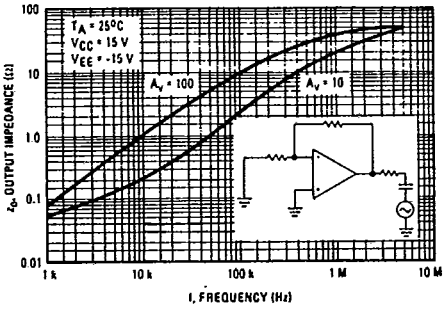
Open Loop Frequency Response



Bode Plot

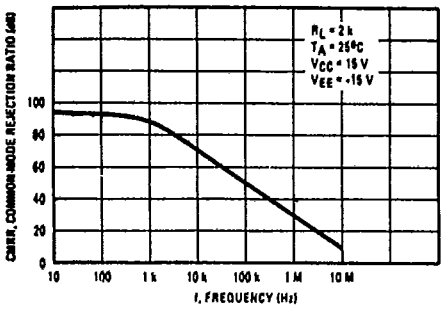


Output Impedance

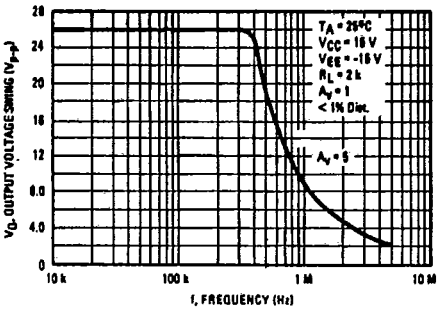


Typical AC Performance Characteristics (Cont.)

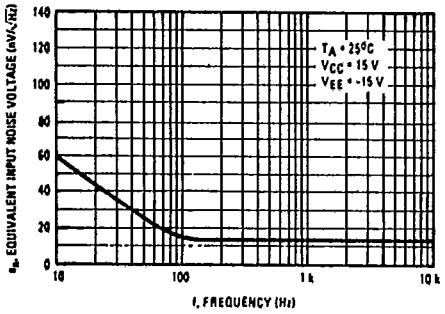
Common-Mode Rejection Ratio



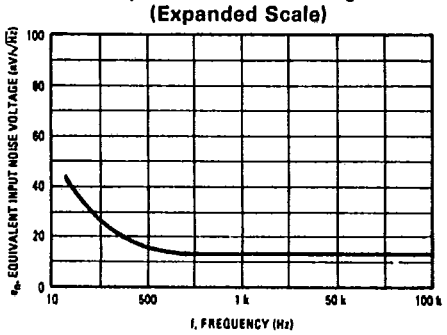
Undistorted Output Voltage Swing



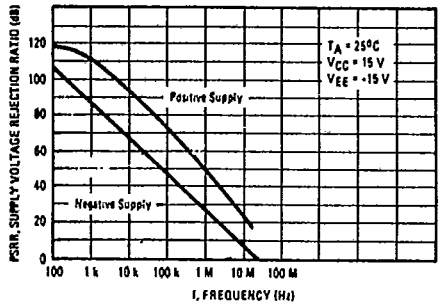
Equivalent Noise Voltage



Equivalent Noise Voltage (Expanded Scale)

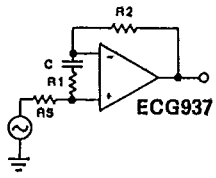


Power Supply Voltage Rejection Ratio



Typical Circuit Applications

Non-Inverting Unity Gain Operation



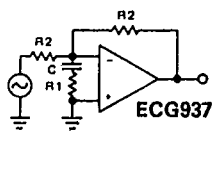
$R1C \geq \frac{1}{(2\pi)(5\ MHz)}$

$R1 = \frac{R2 + R_S}{4}$

$A_{V(DC)} = 1$

$f_{-3dB} \approx 5\ MHz$

Inverting Unity Gain



$R1C \geq \frac{1}{(2\pi)(5\ MHz)}$

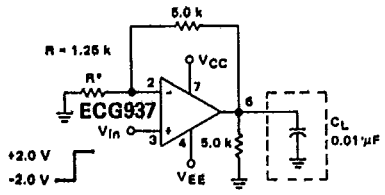
$R1 = \frac{R2}{4}$

$A_{V(DC)} = -1$

$f_{-3dB} \approx 5\ MHz$

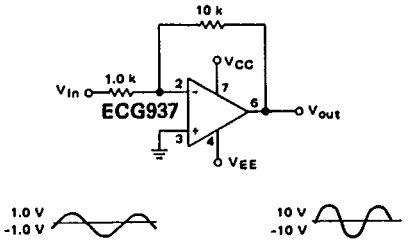
Typical Circuit Applications (Cont.)

Driving Capacitive Loads



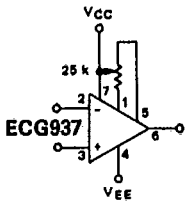
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.
$C_{L(max)} \approx 0.01\ \mu F$.
Overshoot < 20%
Settling time (t_s) ≈ 5.0 µs

Large Power Bandwidth Amplifier



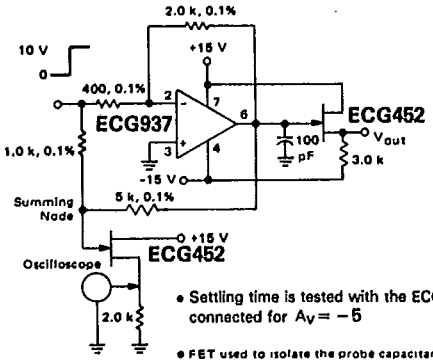
For distortion < 1% and a 20 Vp-p V_{Out} swing, power bandwidth is: 500 kHz.

Input Offset Voltage Adjustment



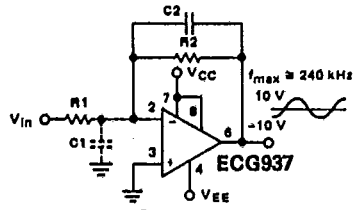
- V_{IO} is adjusted with a 25 k potentiometer
- The potentiometer wiper is connected to V_{CC}
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 µV/°C/mV of adjustment.
- Typical overall drift: 5.0 µV/°C ±(0.5 µV/°C/mV of adjustment.)

Settling Time Test Circuit



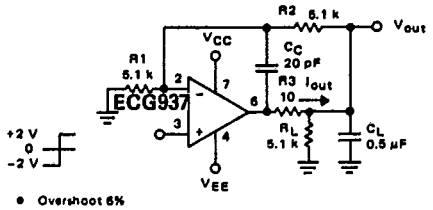
- Settling time is tested with the ECG937 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10 V step

Wide BW, Low Noise, Low Drift Amplifier



- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \approx 240\ kHz$
- Parasitic input capacitance (C1≅3 pF plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2≅R1C1.

Isolating Large Capacitive Loads

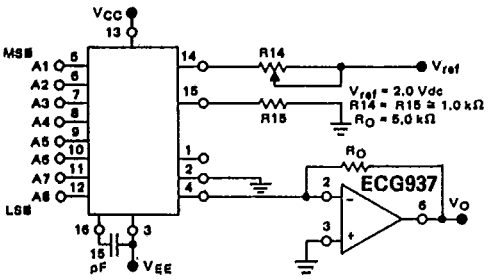


- Overshoot 6%
- $t_s = 10\ \mu s$
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \geq \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

Typical Circuit Applications (Cont.)

8-Bit D/A with Output Current to Voltage Conversion



Theoretical V_O

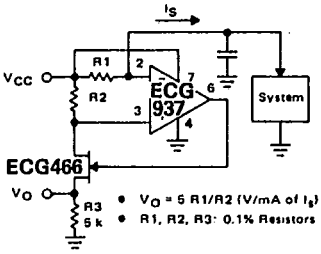
$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O to that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2V}{1k}(5\,k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

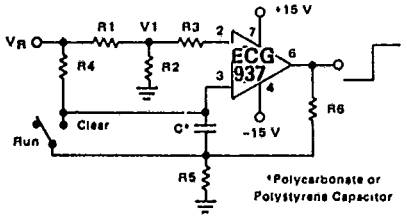
$$= 10\,V\left[\frac{255}{256}\right] = 9.961\,V$$

Precision Current Monitor



- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% Resistors

Long Interval RC Timer



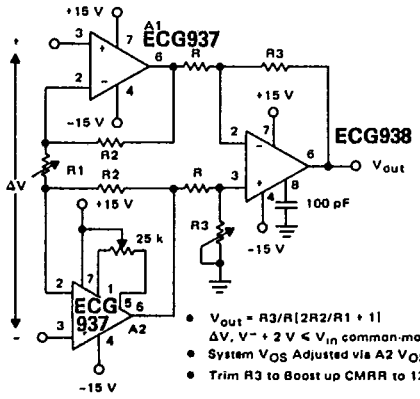
Time (t) = R4C$\ln(V_R/V_R - V_t)$, $R_3 = R_4$, $R_5 = 0.1$ R6
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer

V_R = 10 V C = 1 μF R3 = R4 = 144 M

R6 = 20 k R5 = 2 k R1 = R2 = 1 k

High Impedance, Low Drift Instrumentation Amplifier



- V_{out} = R3/R[2R2/R1 + 1]
  ΔV, V^- + 2 V ≤ V_{in} common-mode ≤ V^+
- System V_{OS} Adjusted via A2 V_{OS} Adjust
- Trim R3 to Boost up CMRR to 120 dB